Mott DAQ Timing

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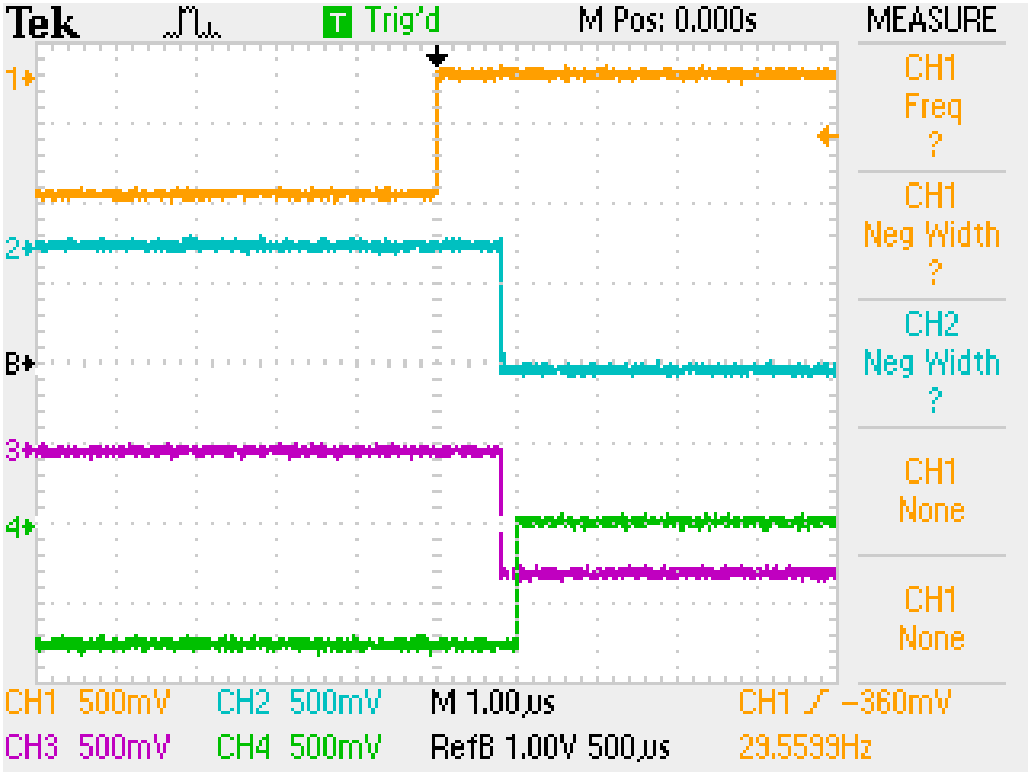
Helicity Signals Timing

T_Settle starts 1.0 µs earlier than all other helicity signals



T_Settle

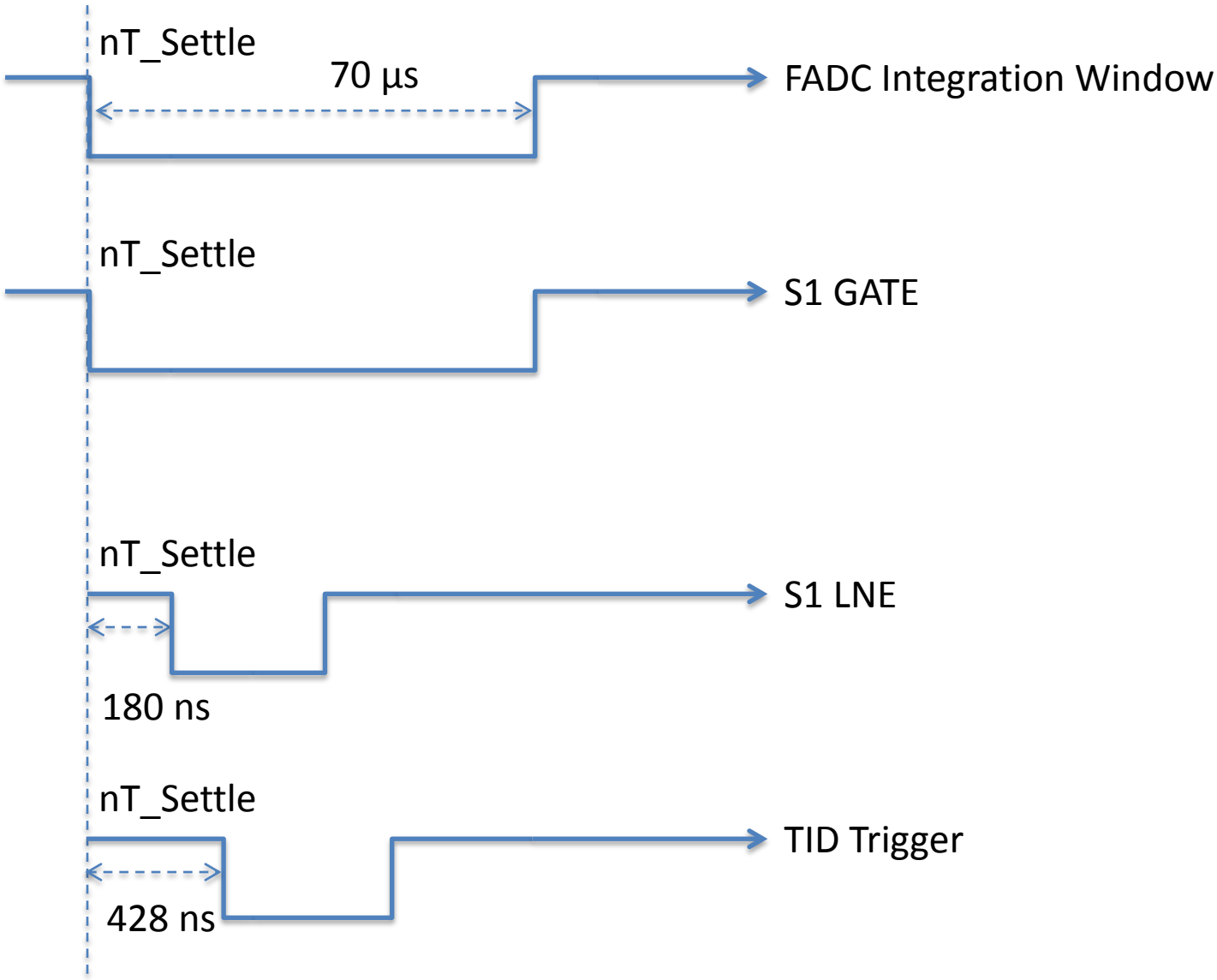
Pair -Sync

Pattern-Sync

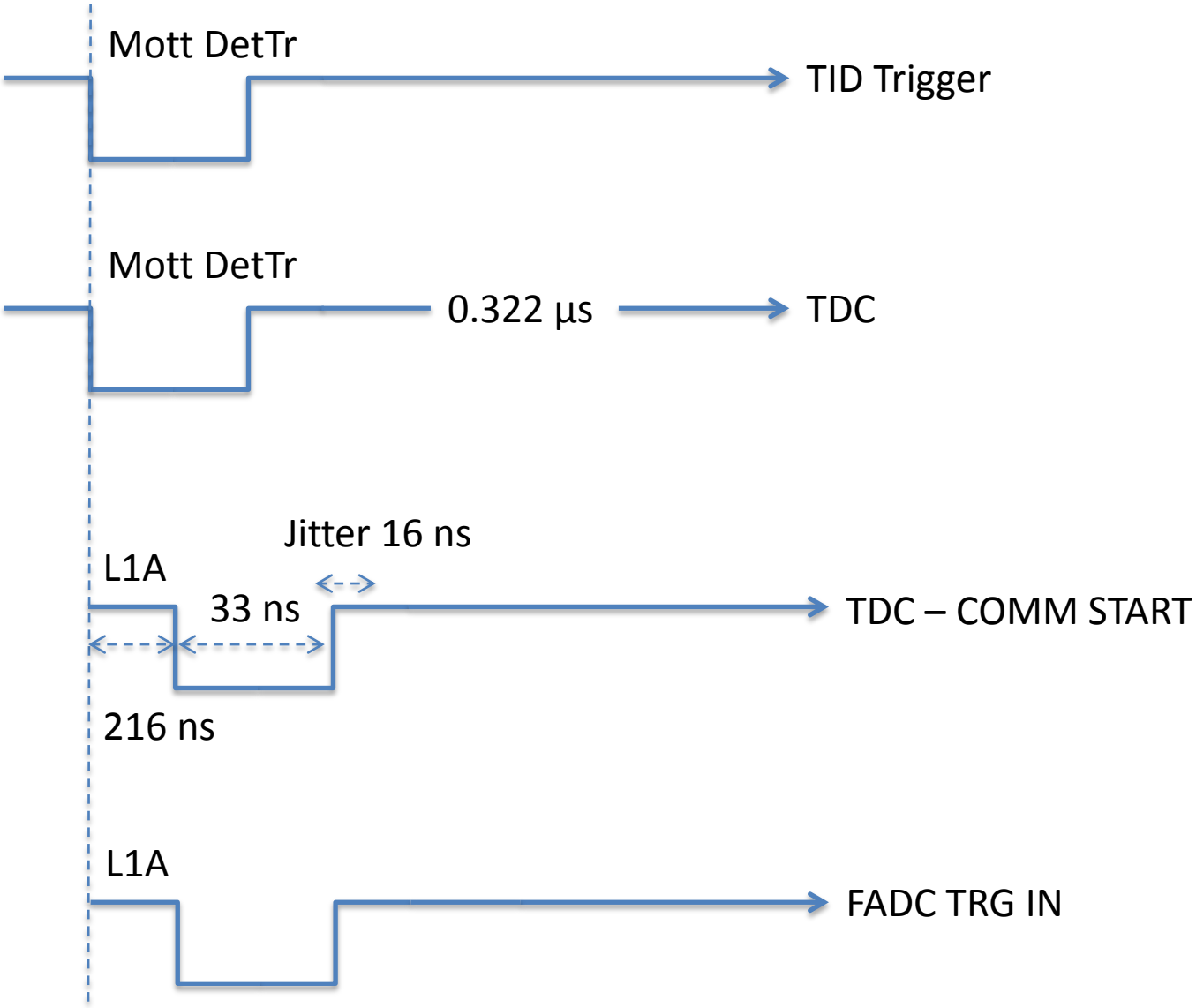
Delayed Helicity

ΔT(nT_Settle - PairSync) = 0.94 µs
ΔT(nT_Settle - PatSync) = 1.1 µs
ΔT(nT_Settle - Delayed Hel) = 0.95 µs

Scalers / FADC_Int



Mott Signals



Busy Delays

All the measurements were done using the configuration (or control readout list “crl”) files used during the data taking.

TOT Busy (µs)	Mode	Channels
47.6 – 52.4	FADC Int	At 30 and 960 Hz
214	Mott Sample	

Busy Delays

The evaluation of the busy signal for each single piece was done starting from the configuration files used during the data taking. To evaluate each contribution all the other boards were removed from “trigger” session of the crl file. ONLY the correspondent board was read.

Busy (us)	Module	Mode	
106	FADC	Mott Sample	16 channels and 500 samples
83	FADC	Mott Sample	16 channels and 148 samples
25 – 26	FADC	FADC_Int	16 channels
14.8 – 17.4	TDC		
31 – 32	Scalers (S1+S2)		Both boards together
11.8 – 13.2	Scaler S1		Only Scaler S1
8.8 – 9.9	All environment		NO readout of any board

Delays & Signals

Signal	Delay	Width	Jitter
S1 LNE = nT_Settle delayed	180 ns	70 µs	
TID Trigger = nT_Settle delayed	428 ns	70 µs	
TDC Mott Detector Trigger	322 ns		
L1A – Detector Trigger	216 ns	33 ns	16 ns
121 kHz Clock	8.16 µs		

Signal	Amplitude	Width
TTL detector signals in S2	+5 V	20 ns
NIM detector signals in S1	-0.7 V	20 ns