**Requirements of SCAM for 4-Laser Operations**

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**Contact J. Grames**

[**grames@jlab.org**](mailto:grames@jlab.org)

**Introduction**

The SCAM (Service Building Catch All Module) is a programmable interface to the Laser Macropulse chassis to select the desired laser beam modes. The previous SCAM module supported 3-laser operation and both polarized and thermionic sources. This version supports 4-laser operation and only a polarized source.

**Functional Description**

Laser control is partitioned in 5 ways: Master, Laser A, Laser B, Laser C and Laser D. The Master partition limits the accessible modes of the individual Lasers (A, B, C, D).

Each partition allows 5 beam modes of user selected laser operation, where the User mode is the highest order.

1. Beam Off Mode
2. Pulsed Viewer Mode
3. Pulsed Tune Mode
4. Continuous Wave Mode
5. User Mode

All macropulse modes are triggered with respect to the Beam Sync marker pulse. The Beam Sync marker pulse may be generated in one of two User selected methods:

* *Input Line Sync* – A line sync module that detects zero crossing of one phase of site power provides the SCAM with an Input Line Sync pulse. The SCAM delays the Beam Sync marker pulse by a User defined Beam Sync Delay after input Line Sync of value of 0-16,000 us in 10 us increments after Input Line Sync. Drive signals to all lasers use this same timing value.
* *Free Run Sync* – An internal 20 MHz clock of the SCAM module self-generates an internal Free Run Sync pulse. In this mode the User may set the frequency within the range 40-200 Hz in 0.1 Hz increments (corresponds to period Tperiod 25.0-33.3 milliseconds). The SCAM delays the Beam Sync marker pulse by a User defined Beam Sync Delay value of 0-16,000 us in 10 us increments after Free Run Sync. Drive signals to all lasers use this same timing value.

Beam modes are defined:

1. *Beam Off Mode*

In this mode the user can individually turn off the beam any Laser. The user can turn off all Lasers by setting the Master to Beam Off.

1. *Pulsed Viewer Mode*

In this mode the user can individually set any Laser to Viewer mode, provided the Master mode is of equal or higher order. Lasers of higher order than the Master mode will automatically be set to the Master mode. The Viewer mode macro-pulse structure (Fig. 1) has one ON pulse. This pulse is delayed from Beam Sync by a User defined value of 340-360 us in 0.2 us increments and with a User defined pulse width of 0.2-10 us in 0.1 us increments.

1. *Pulsed Tune Mode*

In this mode the user can individually set any Laser to Tune mode, provided the Master mode is of equal or higher order. Lasers of higher order than the Master mode will automatically be set to the Master mode.

The Tune mode macro-pulse structure (Fig. 1) has two ON pulses. The first time period is triggered at Beam Sync with a User defined pulse width of 100–250 us in 10.0 us increments. This “ON” time is individually selectable for each drive output.

The second time period is delayed from Beam Sync with a User defined value of 340-360 us in 0.2 us increments. Drive signals to all lasers use this same timing value.

The third time period is a User defined “ON” pulse width of 0.2-10 us in 0.1 us increments. Drive signals to all lasers use this same timing value.

1. *Continuous Wave Mode*

In this mode the user can set individually any Laser to Continuous mode, provided the Master mode is of equal or higher order. There is no macro-pulse structure; the beam is always ON. This mode of operation may be implemented in both Line-Sync and Free-run modes.

1. *User Modes*

In this mode the user can set individually any Laser to a User mode, provided the Master mode is of equal or higher order. The SCAM will generate the same pulse structure for all lasers.

The following User modes are defined:

* + *User Mode 1 – Variable Duty Factor*

In this mode the user can individually set any Laser to User Mode 1, provided the Master mode is of equal or higher order. The SCAM will generate the same macro-pulse timing structure for all lasers. In this mode a single beam ON macropulse will be generated start time Tstart to end time Tend relative to Beam Sync (see Fig. 2). The two constraints are that both Tstart and Tend are at least 500 us less than the Beam Sync period and that Tstart is at least 1 us earlier than Tend. The step size for Tstart and Tend is 0.1 us.

**I/O Interface**

In order to provide the above functionality and requisite CEBAF safety features the SCAM will have the following interfaces.

1. Line Sync Input
2. Beam Sync Output
3. Pre-Trigger Output
4. Beam Mode Outputs
5. VME bus I/O
6. FSD/VL Limit Input

We define the interfaces below. For clarity a timing diagram is shown in Fig. 1 and an interface diagram is shown in Fig. 3. The text “x4” refers to four independent channels for Laser A, B, C, D.

1. *Line Sync Input*

The SCAM will receive on fiber from Line Sync Module the Line Sync Input derived from the zero crossing of wall plug AC line. A copy of Line Sync Input will be provided on TTL and Fiber.

1. *Beam Sync Output*

The Beam-sync pulse is user defined starting at Line-sync to a maximum time of 16.666ms in 0.1 us steps with a fixed pulse width of 354us. The Beam Sync Output pulse will be provided on both TTL and Fiber.

1. *User-Trigger Output*

The User-Trigger pulse is user defined starting at Line-sync to a maximum time of 16.666ms in 0.1 us steps with a user defined pulse width 1-500 us in 0.1 us steps. The User-Trigger Output will be provided on both TTL and Fiber.

1. *Beam Mode Outputs*

The SCAM will provide drive signals (x4) by fiber to the Laser Macropulse chassis enabling the Beam modes of laser operation.

1. *VME Bus I/O*

The SCAM will have a 16-bit wide VME bus interface. The user will access control and status registers through this interface in order to select the modes of the SCAM. The SCAM will contain registers identifying the current code revision (MM/DD/YY).

1. *FSD/VL Limit Input*

The SCAM has an input that can monitor an FSD-type input (5Mhz square wave) that can force all Beam Mode outputs to Viewer-limited mode in the absence of the signal. The SCAM provides both live and latched status for EPICS readback. This function can be enabled/disabled via a bit in the ACC control register.

**Registers and Bit Assignments**

Registers are accesible via the 16-bit VME interface.

1. Code Revision Registers (by Revision Date)
2. Accelerator Control/Status Register
3. Hall A Tune-Mode Modulation Register
4. Hall B Tune-Mode Modulation Register
5. Hall C Tune-Mode Modulation Register
6. Hall D Tune-Mode Modulation Register
7. All Halls Tune-Mode Delay Register
8. All Halls Tune-Mode Marker & VL Pulse
9. Frequency Period Register
10. Trigger Delay Register
11. Pre-trigger Pulse Width Register
12. Post-trigger Pulse to Beam-Sync Output Delay

Registers are defined in more detail below. Note that some register widths exceed the 16-bit word width. For clarity a timing diagram is shown in Fig. 1 and an interface diagram is shown in Fig. 2. The text “x4” refers to four independent channels for Laser A, B, C, D.

1. *Code Revision Regisers*

Revison “Month” – Base Address + 0, Read-only, Even Byte

Two four-bit nibbles containing the month of the most recent code update.

Format – Decimal

Revison “Day” – Base Address + 0, Read-only, Odd Byte

Two four-bit nibbles containing the day of the month of the most recent code update.

Format – Decimal

Revison “Year” – Base Address + 1, Read-only, Even Byte

Two four-bit nibbles containing the last two digits of the year of the most recent code update.

Format – Decimal

1. *Accelerator Control/Status Register*

Control/Status – Base Address + 1, Various R/W, Odd Byte

Bit-0 – Line-Sync Active. A HI bit indicates that the input Line-Sync signal is active.

Format – Binary, Read-only

Bit-1 – ACC FSD/VL Limit Status. Real-time status of the ACC FSD/VL Limit input. A HI bit indicates that the signal is present.

Format – Binary, Read-only

Bit-2 – Latched FSD/VL Limit Status. A HI bit indicates that a fault occurred on the input signal. This also forces the ACC and all Halls Beam Modes to drop to VL Mode if in a higher mode and this feature is enabled. Reading of the register clears the fault bit.

Format – Binary, Read-only

Bit-3 – FSD/VL Limit mask bit. Default state is LO which enables the FSD/VL Limit feature noted above.

Format – Binary, Read-only

Bit-4 – Sync-Select. A LO bit sets all output timing signals referenced to the 60Hz Line-Sync input. A HI bit sets the SCAM to Free-Run mode; all timing and output signals are referenced to the Frequency Period Register.

Format – Binary, R/W

Bits-5, 6 – ACC Mode Control/Status. Two-bits that determine the operating mode of the SCAM and the laser drive signals. Note that no Hall is permitted to operate at a higher mode than the ACC. These operating modes (R/W) are:

Mode-0 – Viewer-Limited Mode (00)

Mode-1 – Tune-Mode (01)

Mode-2 – CW Mode (10)

Mode-3 – User Mode (11)

Format – Binary, R/W

Bit-7 – ACC “GO” Bit. A HI bit permits any of the above operating modes and allows the individual Hall “GO” bits to be set. Clearing this bit also clears all Hall “GO” bits.

Format – Binary, R/W

1. *Hall A Tune-Mode Modulation Register*

Base Address + 2, WORD addressing

Hall A “GO” (bit 15) is set HI to enable output to the Hall A laser. The bit is automatically cleared if the ACC “GO” bit is cleared.

Hall A Mode (bits 14-13) determines the mode of the hall operation (see ACC Modes). The mode is permitted to operate only in a mode lower or equal to the ACC mode. This feature is implemented in firmware.

Hall A beam modulation timing count value (bits 12-0) from 100us to 250us in 10us increments. The minimum and maximum range of operation is established in firmware. LSB value is 50ns.

Format – Binary, R/W

1. *Hall B Tune-Mode Modulation Register*

Base Address + 3, WORD addressing

Hall B “GO” (bit 15) is set HI to enable output to the Hall B laser. The bit is automatically cleared if the ACC “GO” bit is cleared.

Hall B Mode (bits 14-13) determines the mode of the hall operation (see ACC Modes). The mode is permitted to operate only in a mode lower or equal to the ACC mode. This feature is implemented in firmware.

Hall B beam modulation timing count value (bits 12-0) from 100us to 250us in 10us increments. The minimum and maximum range of operation is established in firmware. LSB value is 50ns.

Format – Binary, R/W

1. *Hall C Tune-Mode Modulation Register*

Base Address + 4, WORD addressing

Hall C “GO” (bit 15) is set HI to enable output to the Hall C laser. The bit is automatically cleared if the ACC “GO” bit is cleared.

Hall C Mode (bits 14-13) determines the mode of the hall operation (see ACC Modes). The mode is permitted to operate only in a mode lower or equal to the ACC mode. This feature is implemented in firmware.

Hall C beam modulation timing count value (bits 12-0) from 100us to 250us in 10us increments. The minimum and maximum range of operation is established in firmware. LSB value is 50ns.

Format – Binary, R/W

1. *Hall D Tune-Mode Modulation Register*

Base Address + 5, WORD addressing

Hall D “GO” (bit 15) is set HI to enable output to the Hall D

cleared.

Hall D Mode (bits 14-13) determines the mode of the hall operation (see ACC Modes). The mode is permitted to operate only in a mode lower or equal to the ACC mode. This feature is implemented in firmware.

Hall D beam modulation timing count value (bits 12-0) from 100us to 250us in 10us increments. The minimum and maximum range of operation is established in firmware. LSB value is 50ns.

Format – Binary, R/W

1. *All Halls VL Delay Register*

Base Address + 6, WORD addressing, 12-bits used (11-0)

Timing count value for delay of the VL-mode marker pulse from 0us to 360us in .2us increments. The minimum and

maximum range of operation is established in firmware. LSB value is 50ns. Bits 15-13 are unused.

Format – Binary, R/W

1. *All Halls VL-Mode Marker Register*

Base Address + 7, WORD addressing, 9-bits used (8-0)

Timing count value of the pulse width in Viewer-limited mode operation only. The pulse width is variable from .2us to 10us in .1us increments. The minimum and maximum range of operation is established in firmware. LSB value is 50ns. Bits 15-9 are unused.

Format – Binary, R/W

1. *All Halls Tune Delay Register*

Base Address + 8, WORD addressing, 12-bits used (11-0)

Timing count value for delay of the Tune-mode marker pulse from 90us to 110us in .2us increments. The minimum and maximum range of operation is established in firmware. LSB value is 50ns. Note that EPICS should display this as 340-360us (250us + delay register value). Bits 15-12 are unused.

Format – Binary, R/W

1. *All Halls Tune-Mode Marker Register*

Base Address + 9, WORD addressing, 9-bits used (8-0)

Timing count value of the pulse width in Tune-mode operation only. The pulse width is variable from .2us to 10us in .1us increments. The minimum and maximum range of operation is established in firmware. LSB value is 50ns. Bits 15-9 are unused.

Format – Binary, R/W

1. *Frequency Period Register*

Base Address + 10, Base Address + 11, WORD addressing, 19-bits used

Timing count value of the frequency period when operating in Free-Run mode. Bits 2-0 of Base Address + 10 register are the counter MSB’s; bits 15-3 are unused.

Bits 15-0 of Base Address + 11 are the remaining LSB counter bits. The count value is variable from a period of 40-200Hz in .1Hz increments. The minimum and maximum range of operation is established in firmware. LSB value is 50ns.

Format – Binary, R/W

1. *User Trigger Delay Register*

Base Address + 12, Base Address + 13, WORD addressing, 18-bits used

Timing count value of the delay from Line-Sync (when in Line-Sync mode) to the User-trigger Pulse or the timing count value of the delay from start of new frequency period (when in Free-Run mode) to the User-trigger Pulse. If the Trigger Delay count value is zero, the User-trigger output occurs immediately at Line-Sync input or the start of the new frequency period. The count value is variable from 0 to 16.666ms in 10us increments. The maximum value is limited in firmware. LSB value is 50ns.

Format – Binary, R/W

1. *Beam-Sync Trigger Delay Register*

Base Address + 14, Base Address +15, WORD addressing, 18-bits used

Timing count value of the delay from Line-Sync (when in Line-Sync mode) to the Beam-Sync Pulse or the timing count value of the delay from start of new frequency period (when in Free-Run mode) to the Beam-Sync Pulse. The count value is variable from 0 to 16.666ms in 10us increments. The maximum value is limited in firmware. LSB value is 50ns.

Format – Binary, R/W

1. *User-mode T-Start Time Register*

Base Address + 16, Base Address + 17, WORD addressing, 18-bits used

Timing count value of the CW start-time after Line-Sync begins when operating in User mode. Bits 2-0 of Base Address + 16 register are the counter MSB’s; bits 15-3 are unused.

Bits 15-0 of Base Address + 17 are the remaining LSB counter bits. The count value is variable from a period of no delay after Line-Sync begins to 1us before T-End Time in .1us increments. The minimum and maximum range of operation is established in firmware. LSB hardware value is 50ns.

Format – Binary, R/W

1. *User-mode T-Stop Register*

Base Address + 18, Base Address + 19, WORD addressing, 18-bits used

Timing count value of the CW end-time after LINE-SYNC begins when operating in User mode. Bits 2-0 of Base Address + 18 register are the counter MSB’s; bits 15-3 are unused.

Bits 15-0 of Base Address + 19 are the remaining LSB counter bits. The count value is variable in .1us increments from a minimum period of 1us after LINE-SYNC begins to a maximum period of 500us before the next LINE-SYNC tyically occurs. The minimum and maximum values are limited in firmware. LSB hardware value is 50ns.

Format – Binary, R/W

1. *Pre-Trigger Pulse Width Register*

Base Address + 20, WORD addressing, 14-bits used

Timing count value of the Pre-Trigger Pulse Width. The count value is variable from 1us to 500us in 100ns increments. The minimum and maximum values are limited in firmware. LSB value is 50ns.

Format – Binary, R/W

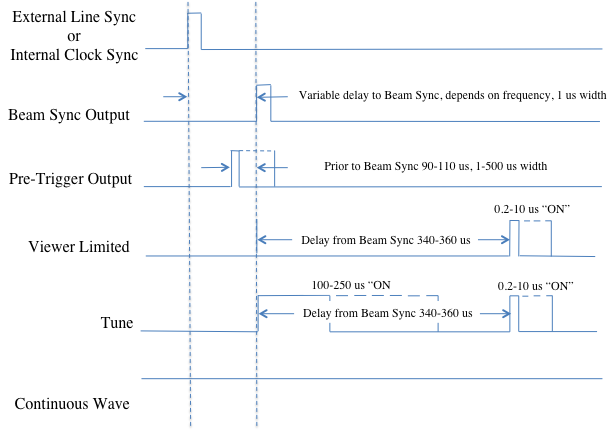


Fig. 1. The SCAM Line Sync input, Digital outputs (Pre-Trigger, Beam Sync) and standard laser control signals (Viewer, Tune, Continuous) are shown. Note that all beam and diagnostic time is time stable relative to the Beam Sync Output pulse.

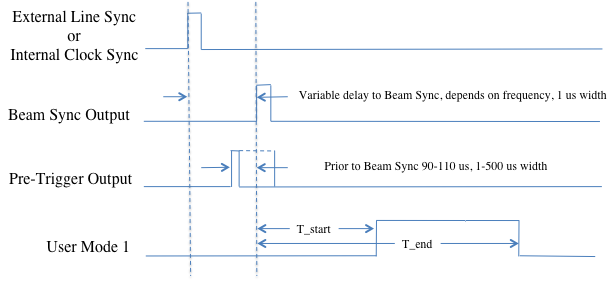


Fig. 2. The SCAM Line Sync input, Digital outputs (Pre-Trigger, Beam Sync) and user laser control signal (User#1) are shown. Note that all beam and diagnostic time is time stable relative to the Beam Sync Output pulse.

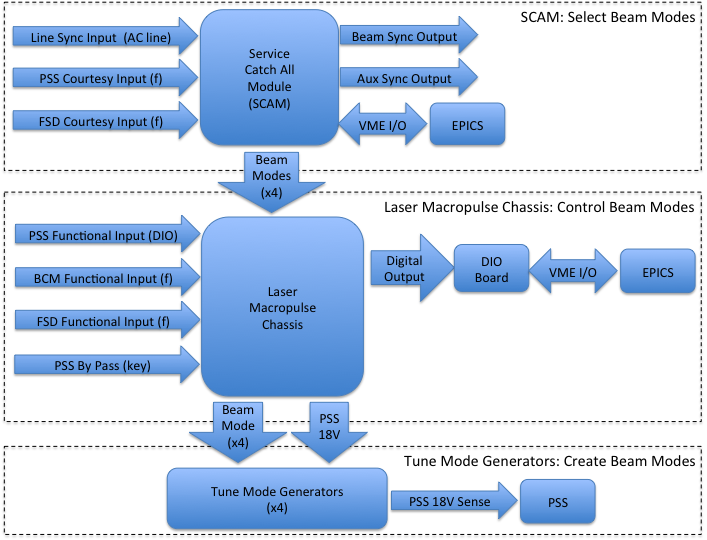


Fig. 3. Shown is the interface diagram of the SCAM, Laser Macropulse Chassis and Tune Mode Generators along with I/O dependencies and interface to the EPICS control system.