Helicity Decoder Board

Prevents mis-identification of real helicity of some of events in counting mode – needed with 2 kHz MOLLER Helicity Reversal

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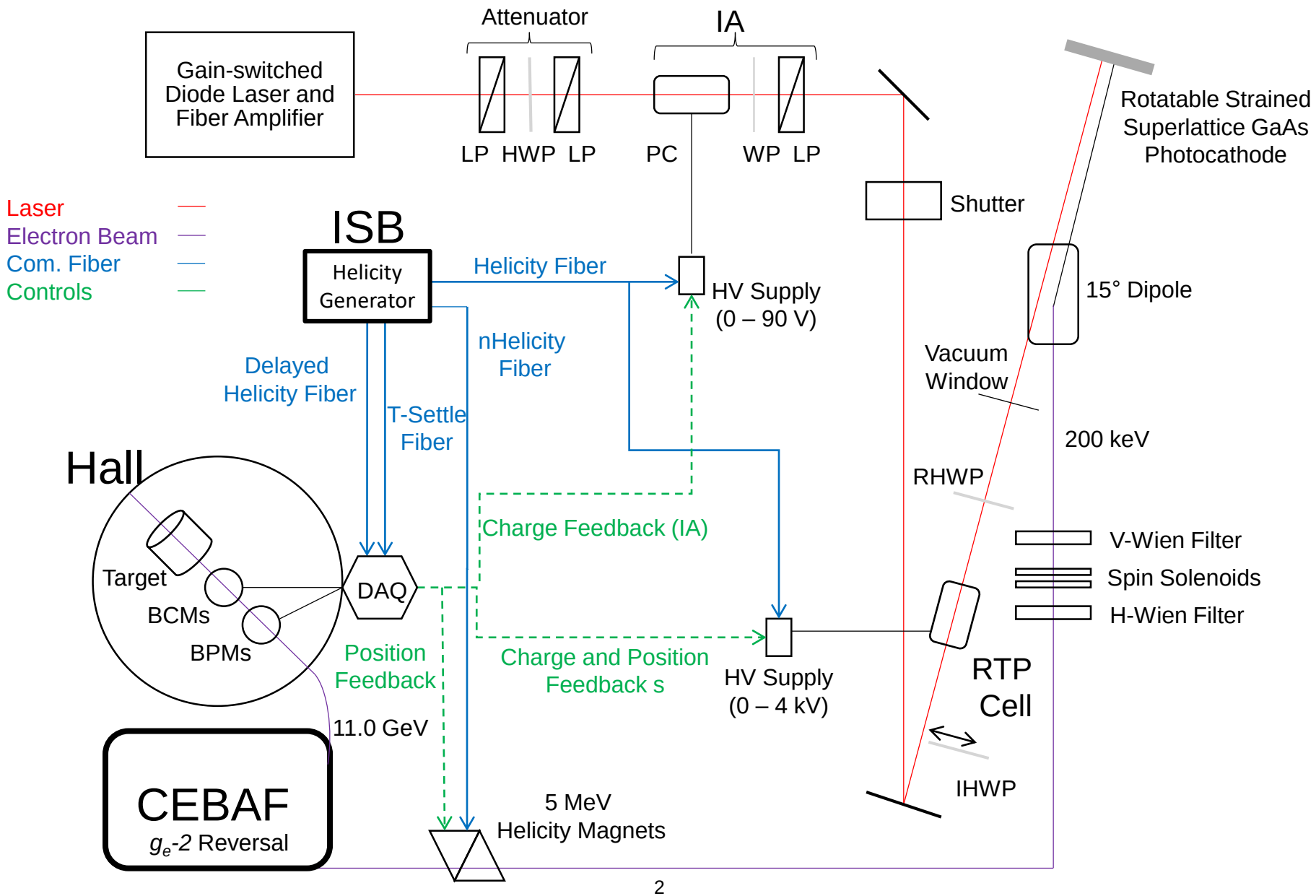
CEBAF Helicity Controls



Helicity Generator Signals to DAQ – What user gets

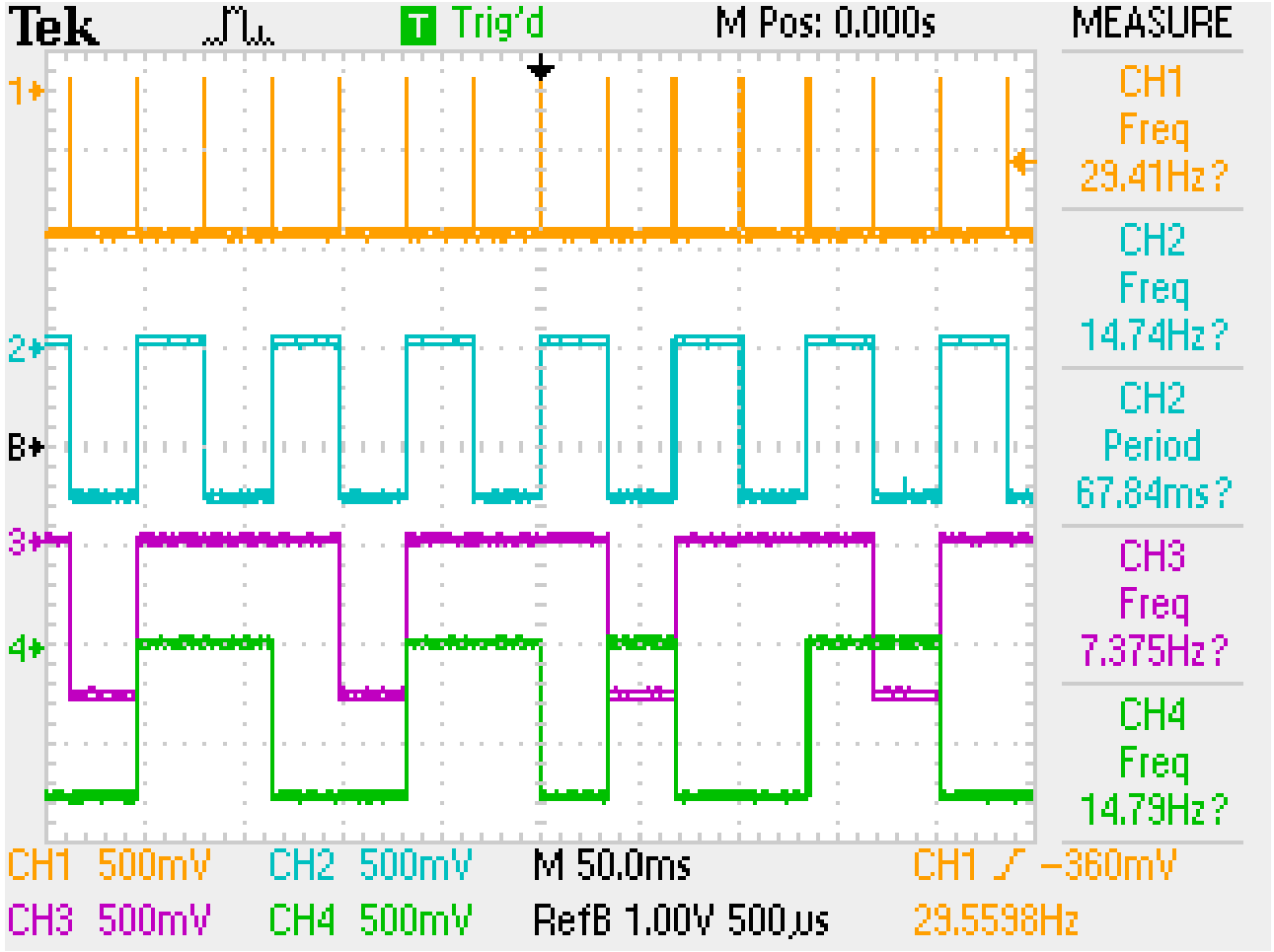
- Example:
  Quarter Pattern
  - +--+ or
  - -++-

T_Settle or T_Stable

Pair Sync

Helicity Pattern

Reported or Delayed Helicity



Helicity Generator Signals – Real time signals

T_Settle or T_Stable

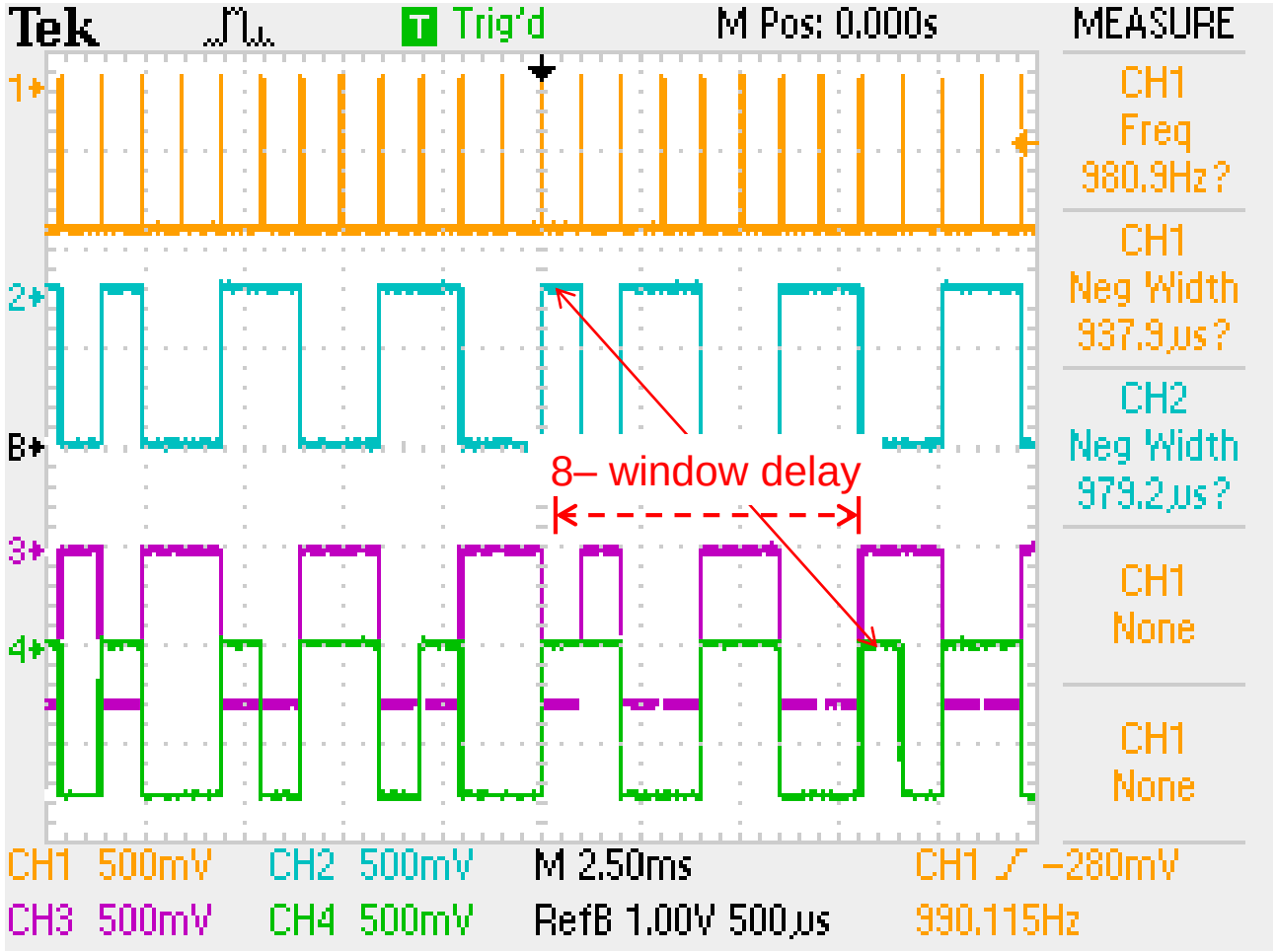
To Pockels Cell (Real Time)

Helicity Flip

To Helicity Magnets (Real Time)

nHelicity Flip

Reported or Delayed Helicity



Helicity Decoder Board

- MOLLER fast helicity reversal (1920 Hz, 10 µsec settle time, 64-window pattern, 128-window delay) could cause mis-identification of real helicity of some of events in counting mode (these are random events), diluting measured asymmetry
- Board to be developed by: MOLLER collaboration (Ohio University), Jefferson Lab Fast Electronics Group and Accelerator Division
- Will be used by data acquisition systems running in counting mode: Hall B, Hall C, Møller Polarimeters and Mott Polarimeter in CEBAF Injector
- **Board will not reconstruct real helicity or real 30-Bit Shift Register**
- Board has four input signals: T_Settle, Delayed Helicity, Helicity Pattern, and Pair Sync
- For each counting event:
  - Now: Delayed Helicity and Pattern are recorded in Rings of helicity-gated SIS3801 Scaler. Offline analysis then attempts to construct real helicity, a complicated process due to delay and randomness of events.
  - New Board: board will keep records of helicities spanning last 30 patterns – to be able to construct 30-bit shift register seed of pseudo-random helicity generator – and position within pattern. And for each event, these records are read along with event. Offline analysis (anytime>n-patterns) will calculate real helicity using helicity predictor. Will be able to correctly identify helicity of every event.

Electron Beam Travel Time

- With 10 μs T_Settle time, travel time from photocathode (Pockels Cell) to Hall target becomes relevant. Also, time it takes for helicity board signals to propagate to Laser Hut and to Halls.

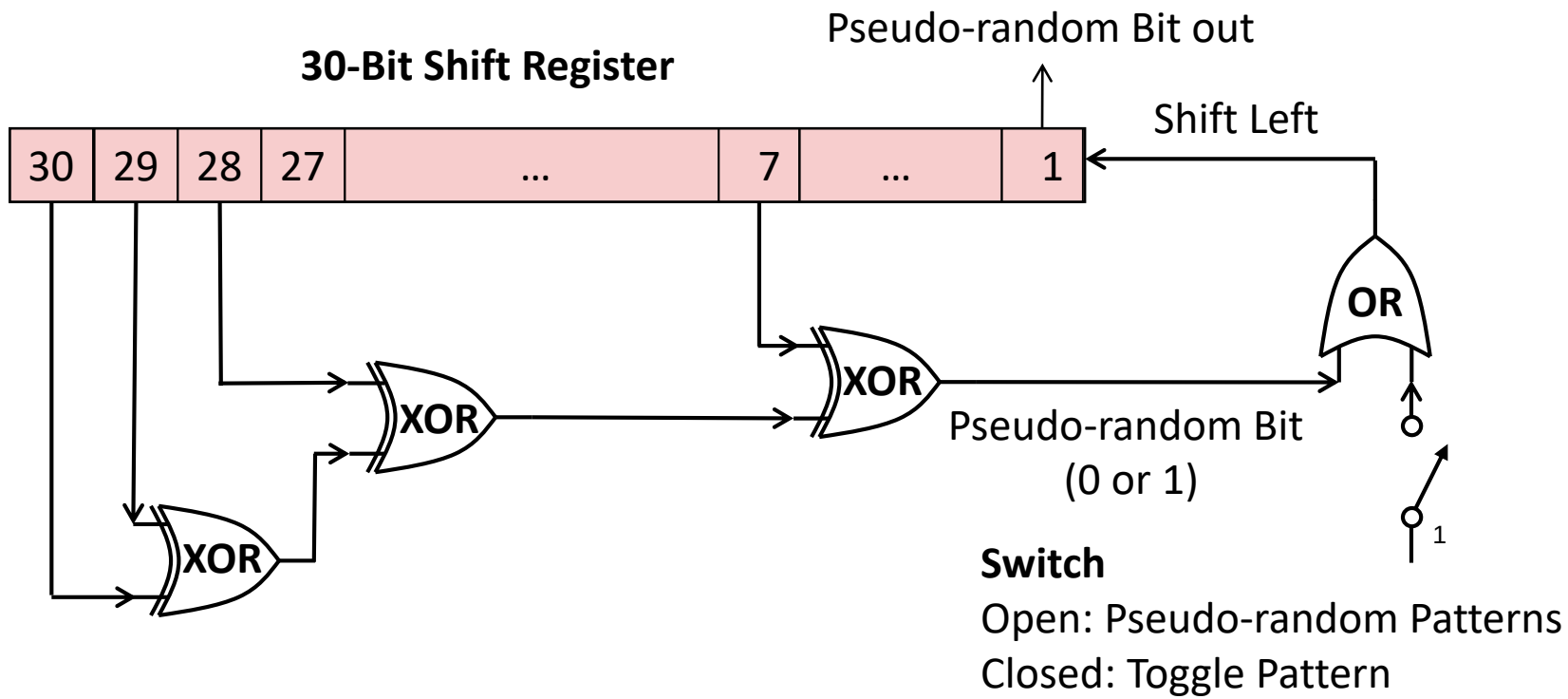
- It takes beam about 4.3 μs per pass to reach Hall.

- Fiber length from Injector Service Building (ISB) IN01B05 to Hall C was measured to be 1705 ft using “20 MHz Clock” fiber. With n=1.45, it takes 2.5 μs for helicity signals to travel in fibers to Hall.

  - All these travel times will be accounted for in this new Helicity Decoder Board such that recorded events have correct helicity at Physics Interaction Time

Pseudo-Radom Helicity Generator

- Determines helicity at start of pattern
- Use 30-bit Shift Register
- It is Pseudorandom, not “Random” because it is deterministic, once a sequence of 30 helicity states is known, next states can be predicted, and it repeats its cycle.
- For any initial seed, there are $2^{30} – 1 =$ 1,073,741,823 (maximal length) random bits before sequence repeats, 50 days for 1000 Hz helicity reversal rate and a Quartet.



Decoder Board I/O and Features

- Input:
  1. T_Settle
  2. Delayed Helicity
  3. Helicity Pattern
  4. Pair Sync

  } NIM or Fiber, programmable

  5. External 250 MHz FADC Clock (ECL) – Board has 250 MHz internal clock
  6. Trigger and Sync Signals
- Output:
  1. Four NIM helicity outputs (T_Settle, Delayed, Pattern and Pair) after common delay for timing check
  2. 20 Data words for each trigger event
- Add programable common delay (0-30 μs) for input helicity signals:
  - To fix time delays due to beam travel time and helicity signal distribution to Hall
  - Will be measured for each board in a specific DAQ
  - Will sync helicity of beam at Physics Interaction Time in Hall

Scheme Outline

➢New scheme to readout delayed helicity for Physics Event Trigger:

- Running in background in Helicity Decoder Board:
  - On Pattern Start:
    1. Increment pattern counter
    2. Grab delayed (or reported) helicity
    3. Push onto running Helicity Seed (**32 bits**)
    4. Clear pattern phase counter
  - On T_Settle Transition:
    1. Increment pattern phase counter
    2. Increment T_Settle counter

Analysis will use last two delayed helicity windows to check 30-bit Shift Register

- Then, when a physics event triggers DAQ, report Data Word of:
  1. Current seed value – to find true helicity for first window in pattern
  2. Counter of pattern phase
  3. Counters of pattern and T_Settle
  4. Status of T_Settle at time of trigger – to be used to veto event
  5. Event Polarity: XOR of delayed helicity and delayed helicity on Pattern Start

Analysis – Realtime on Crate, Online, Offline

- Use seed value to construct 30-Bit Shift Register – use first 30 bits

- Note: No 1,0 vs 0,1 symmetry, *i.e.*, these two registers generate different helicity sequence:
  a. 11010001111001010101010100011001
  b. 00101110000110101010101011100110

- Predict last 30 bits to confirm valid data – generate delayed helicity shift register
- Predict n-patterns (e.g., two patterns for 8-window delay with Quartet Pattern)
- No realtime prediction on crate level, prediction can happen in analysis after event buffering and/or event transfer from crate
- Use Pattern Phase Counter to find real helicity
- Use status of T_Settle at time of trigger to accept or veto event

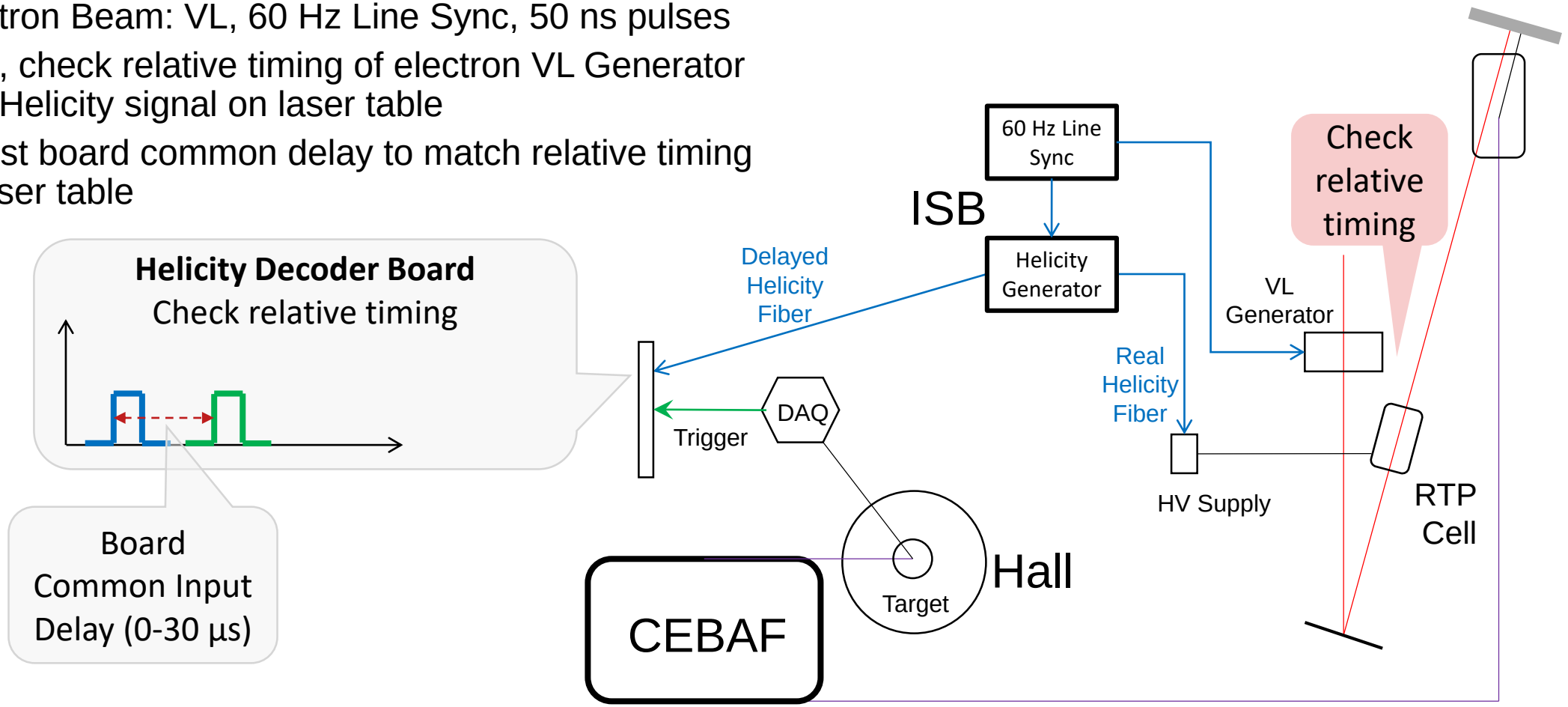
Cross-Check

- For cross-check, Decoder Board will report data words that have same info as Rings of helicity-gated SIS3801 Scaler:
  1. Latched delayed helicity for this event
  2. Latched pattern sync for this event
  3. Latched T_Settle for this event
  4. Time of trigger since start of T_Settle
  5. Time of trigger since end of T_Settle
  6. Duration of previous complete T_Settle interval
  7. Duration of previous complete inverse T_Settle interval
  8. Last 32 windows of Pattern Sync (Delayed Helicity at start of Pattern)
  9. Last 32 windows of Pair Sync
  10. Last 32 windows of Delayed Helicity
  11. Time of trigger since last trigger

- Board will continuously check:
  1. **Delayed helicity at start of Pattern is as expected from 30-bit Shift Register**
  2. No three consecutive delayed helicity signals are same
  3. No two Pair Sync signals are same

Board Programmable Common Delay

- How to set input common time delay:
  - Helicity Board: 60 Hz Line Sync
  - Electron Beam: VL, 60 Hz Line Sync, 50 ns pulses
  - First, check relative timing of electron VL Generator and Helicity signal on laser table
  - Adjust board common delay to match relative timing at laser table



Required No. of Boards – 20 Boards

- Number of boards (20):
  - Accelerator: CEBAF Mott, UITF Mott, Spare
  - Hall A: Moller Pol, Compton Pol, HRS1, HRS2, 2-Spares
  - Hall B: Moller Pol, CLAS, Spare
  - Hall C: Moller Pol, Compton Pol, HMS, SHMS, 2-Spares
  - Hall D: HD, Spare