# Digital Beam Charge Processor

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# Beam Instrumentation Challenge

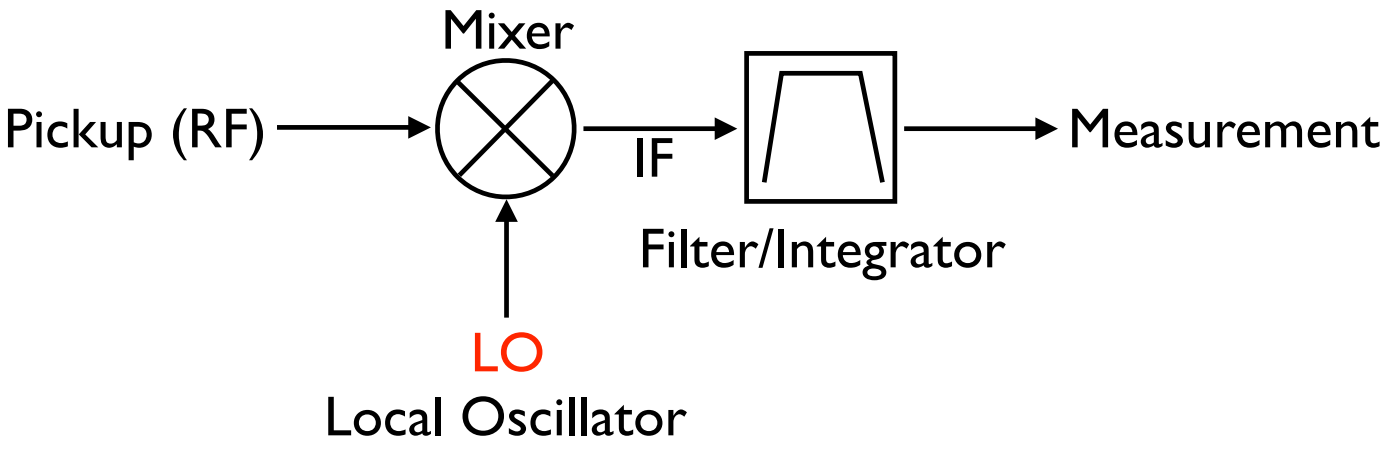
- MOLLER science goals require precision measurement of (false) beam-induced asymmetries
  - Rapid flips of the longitudinal polarization of electrons (2 kHz helicity flip rate)
  - Beam charge asymmetry measurement with 10ppm resolution ($\sigma_Q/Q<14$ ppm)
  - Current state of the art (Qweak): ~65ppm for 1 kHz pulse pair rate
  - Limitation (most likely): LO amplitude and phase noise
- New idea to address outstanding beam instrumentation issues for MOLLER:
  - High-resolution, fully digital beam charge monitor
- LDRD at LBNL (FY18 and FY19)

# Beam Instrumentation Challenge

| Parameter | Jitter requirement | Achieved | Resolution requirement | Achieved |
|---|---|---|---|---|
| Charge | $< 1000$ ppm | 500 ppm | $< 10$ ppm | 65 ppm |
| Energy | $< 108$ ppm | 6.5 ppm | | |
| Position | $< 47$ $\mu$m | 48 $\mu$m | $< 3$ $\mu$m | 2.4 $\mu$m |
| Angle | $< 4.7$ $\mu$rad | 1.4 $\mu$rad | | |

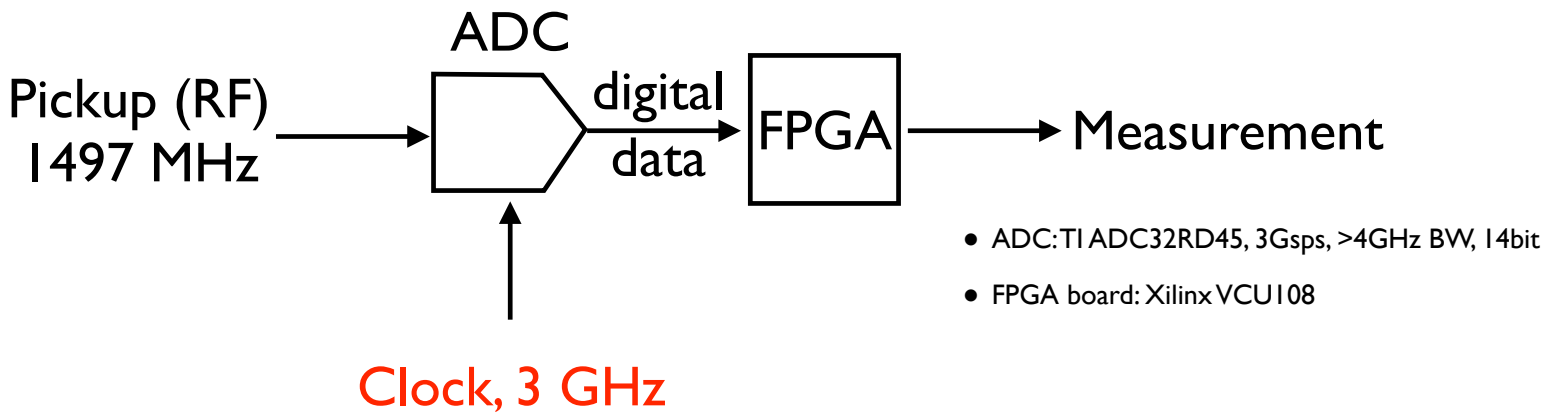
# Beam Charge Monitor

- Measure (monitor) electron beam charge on a pulse-pair basis
- Pick up 1497 MHz RF signal from BCM cavity
  - Expect ~-5 dBm signal for 60 $\mu$A current (check)
- Single pulse duration: 0.5 ms
- Requirement: Pulse-pair charge asymmetry measurement uncertainty <10 ppm; $\sigma_Q/Q<14$ ppm
- Traditional method: cavity/stripline induction
  +RF mixing (down conversion)




- Resolution limited by the amplitude and phase fluctuation of LO

# New approach: digital RF receiver




- High sampling rate (>~3Gsps) and high dynamic range (>10bits) ADCs that are capable of direct RF sampling
- Amplitude fluctuation of LO doesn't contribute. Phase noise is small; modest contribution to the final uncertainly
- Filtering and decimation done digitally in FPGA
- Output: decimated data stream, integrated in 0.5 msec windows in FPGA or offline

# Noise Budget

- Digitizer (white) noise

$$\frac{\sigma_Q}{Q} = 2^{-\mathrm{ENOB}+3/2} \cdot \frac{1}{\sqrt{f_s \Delta T}} \rightarrow \text{ENOB} > 8 \text{ bits}$$

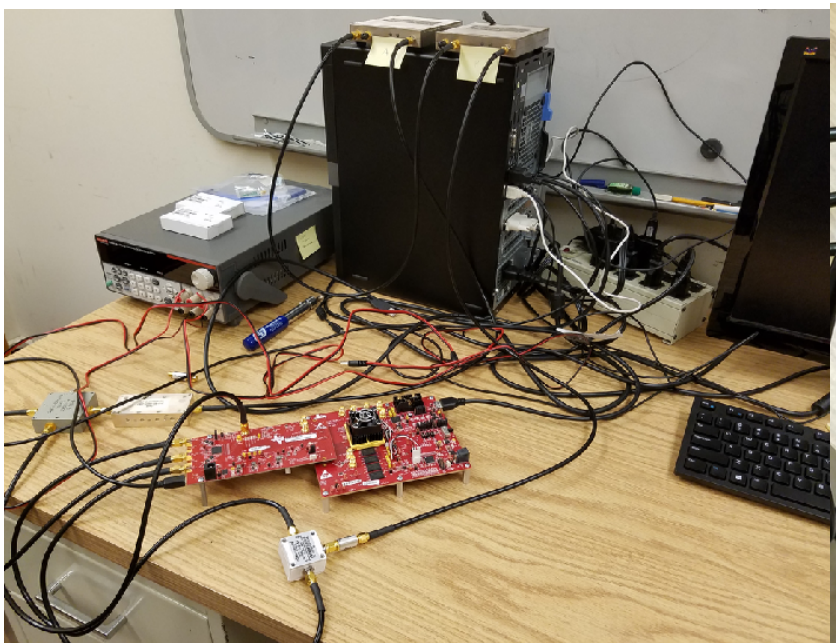
- Thermal noise: -130 dB @ 2 kHz for beam signal of -12 dBm → $\sigma_Q/Q$ ~ 0.3 ppm
- Phase noise (uncorrelated time jitter, though mindful of 1/f contributions):

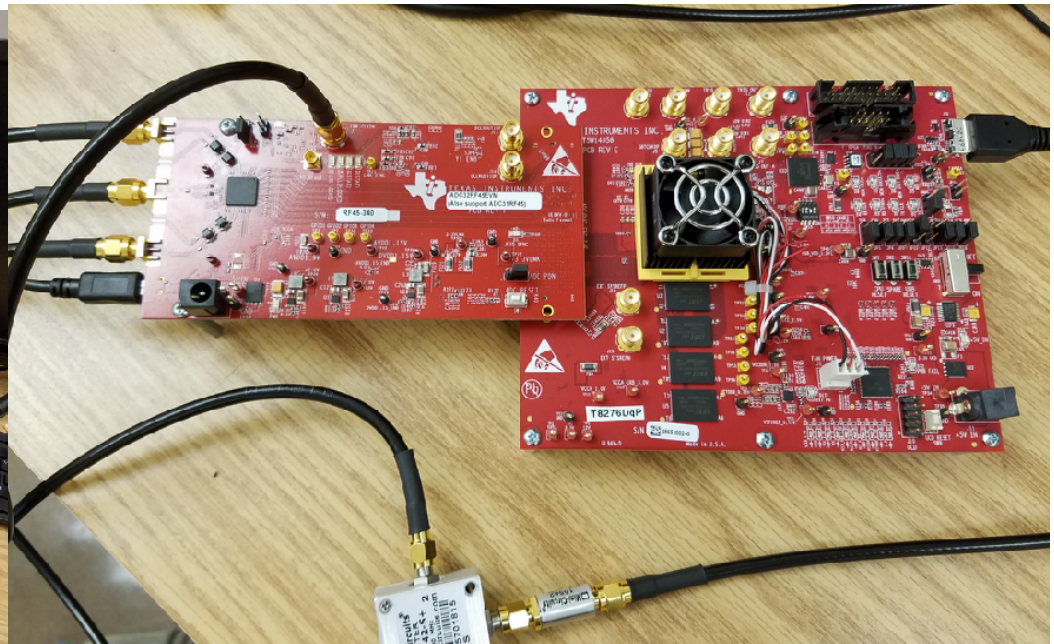
$$\frac{\sigma_Q}{Q} \sim \frac{\pi f \sigma_t}{\sqrt{f_s \Delta T}} \rightarrow \sigma_t < 3.6 \text{ psec}$$

- Spec of $\sigma_Q/Q$<14 ppm achievable with currently available hardware

# BCM Digital Receiver Prototype

- LDRD at LBNL
  - FY18: prototyping, bench tests
  - FY19: full hardware/firmware implementation, beam tests
- Prototype based in TI ADC32RD45 evaluation board and ADC capture card; stream raw data to disk (~200 msec → 2 GB)
  - 14-bit ADC but limited to 12 bits by JESD204B interface with capture card
- Offline analysis (DDC, averaging, asymmetry analysis)





# RF Clock

- ERA Instruments ERASynth+: software-configurable, low-jitter RF generator; oven-controlled oscillator
- Use two phase-locked generators
  - 3 GHz clock
  - RF signal (<1.5 GHz)
  - Split signal between 2 input channels of the ADC (typically 11 dBm/channel)

# RF clock: phase noise

## Adequate for 10 ppm resolution

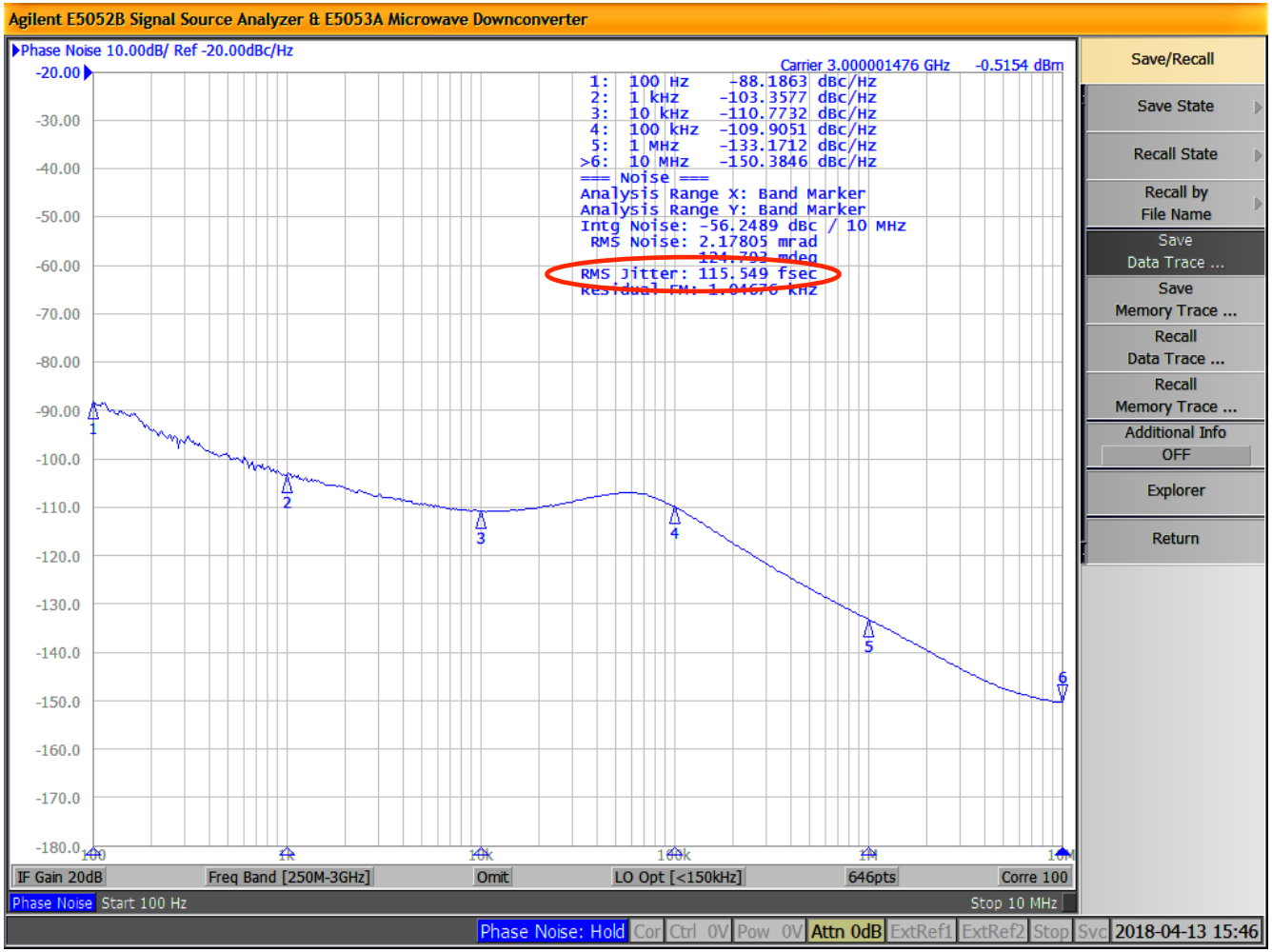
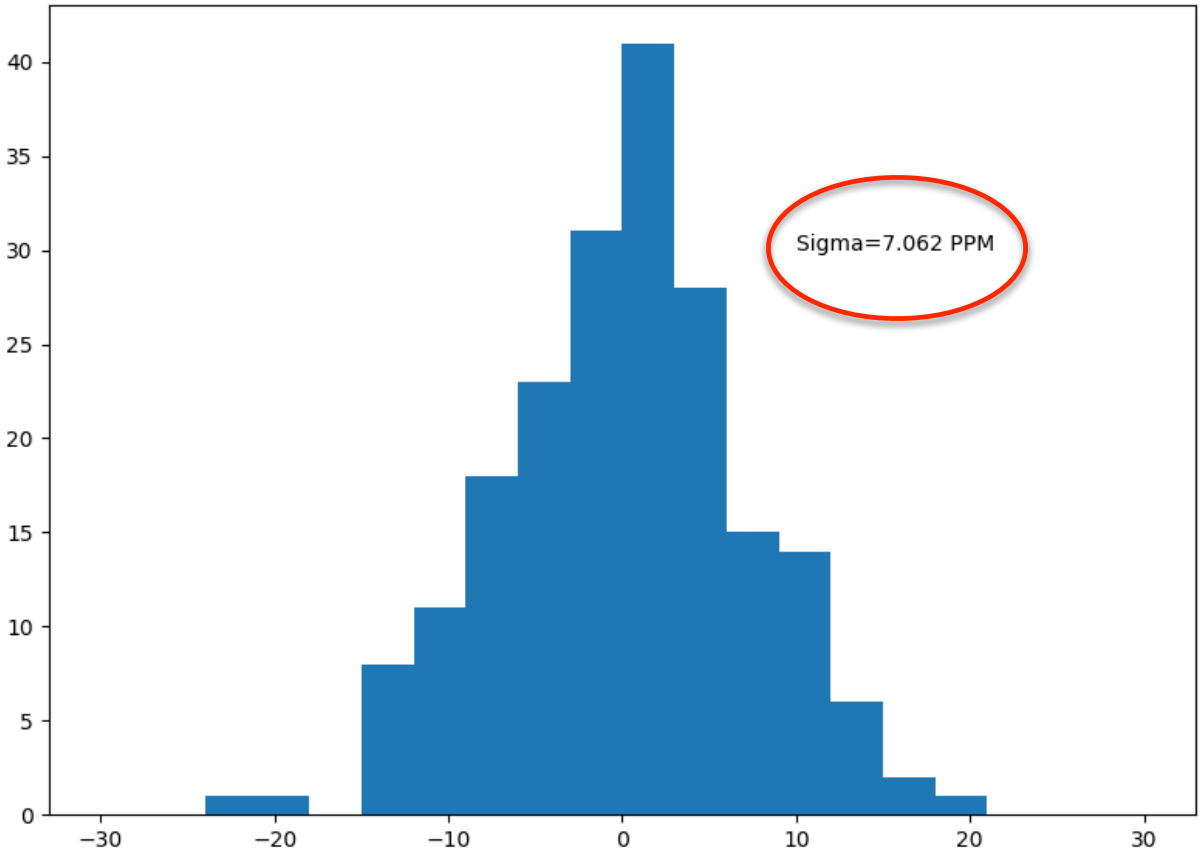


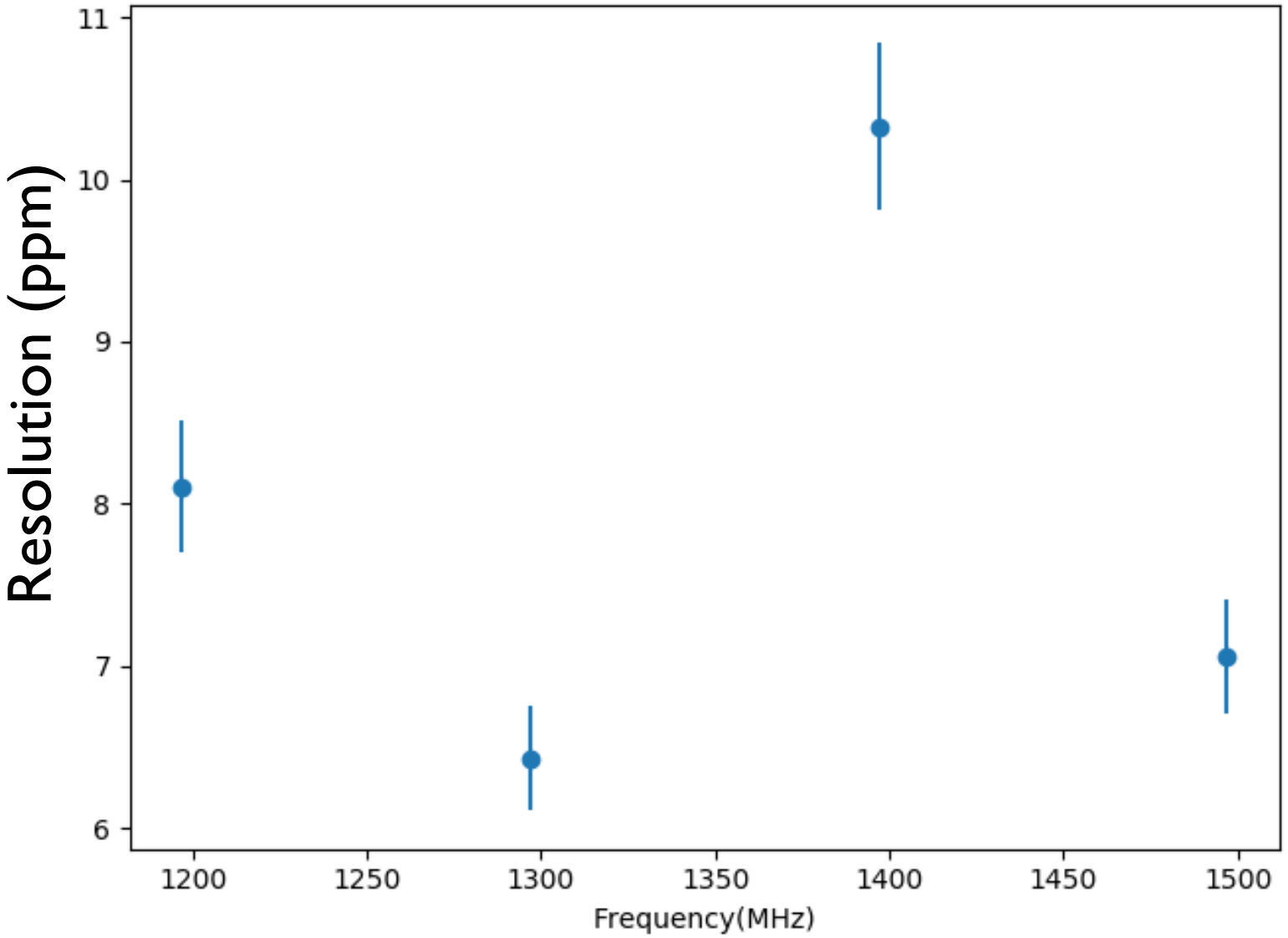

Figure 27: ERASynth+ Phase Noise Performance at 3 GHz RF Output

# Performance

Asymmetry difference (ppm), 1 kHz pairs
1497 MHz, +9 dBm input signal
3000 Msps, 12 bit digitizer



# Performance



# Next Steps

- Build a real chassis
  - 4-channel unit (2 independent ADC boards, 2 channels each)
  - Basic RF front end (amplifier/attenuator, bandpass)
  - Built-in clock (ERASynth+), phase locked to external reference (TBD)
  - Readout into single FGPA board (VCU108) for DSP, stream decimated data out
  - Hardware should be ready in ~month, firmware development ~1-2 months
- Evaluate performance on the bench; ready for beam tests in early 2019

# Questions for this group

- When (and where) to schedule beam test
  - Dedicated vs parasitic
  - Available hardware (BCMs)
  - Expected signal power (beam current)
  - Interface to the accelerator clock distrubution
    - Frequency, phase noise of the clock ?
- Interfaces to the parity/Hall A DAQ
  - Clocks, helicity windows, data stream synchronization ?
  - Hardware interfaces (copper vs optical ?)

# Backup