16 Channel Ethernet Flash 250 MHz Analog to Digital Converter (EFADC250-16)

General Description:

The EFADC250-16 collects and processes data from sixteen 12-bit ADC input channels. It sums ADC samples from 4 groups of 4 ADC channels in each group. When the sum is greater than a user programmable threshold and in coincidence (coincident matrix) with other group(s) or itself, the firmware sums N user programmable samples (Integrating Window width) for each ADC channel of the coincident groups and sends the sums either with samples (Sample Mode) or without the samples (Sum Mode) to the host computer via Ethernet in as a stand-alone device. All parameters for pulse processing such as pulse width, sample window, coincident matrix, etc. are programmable through Ethernet. Firmware can be updated either through Ethernet or directly with a Xilinx USB JTAG cable.

Front Panel

Hardware Specifications:

External Power Supplies:
+5 V +/- 2% 8 Amp
+12V +/- 2% 1 Amp
-12V +/- 2% 1Amp
Analog to Digital Converters:
16 ADC (AD9230BCPZ-250) Channels
12 bits resolution
ADC sampling rate: 250 MSample/Sec.
Input Voltage Range: 0…-2V; 0…+2V; +1…-1.
Front panel Lemo input jacks
Fiber optic Input Output[I/O]:
Support either wire or QSFP+ iSR4 (AFBR-79EIDZ) Pluggable, Parallel Fiber-Optics Module
2 6.6 GHz Xilinx GTP Transceivers
1 250 MHz Clock I/O
1 1MHz I/O
Ethernet: Micrel KSZ9021GQ Gigabits Ethernet Transceiver with GMII/MII support
Display: 2 Lines, 16 characters per line LCD
FPGA: Two Xilinx Artix XC7A200T

Firmware Specifications:

Operates stand-alone or with Ethernet Trigger Supervisor (ETS):
Automatically switches between the 2 modes
In stand-alone mode, configuration and data output is through Ethernet.
Inn ETS mode, configuration and data output is through Fiber I/O.
ETS mode takes precedent over stand-alone mode.
Ethernet: Support UDP, Ping, ARP protocols
60 Mbytes/Sec data throughput.
Fibers: Support Xilinx AURORA protocol
625 Mbytes/Sec data throughput
Pulse Specification:
Minimum Pulse Width: 8 nS
Maximum Pulse Width: 2000 nS
Trigger Rate: 420KHz Continuous Processing 100nS Pulse Width.
Mode Of Operation: Sum, Sample
FPGA firmware update: Front Panel using USB JTAG or update via Ethernet port

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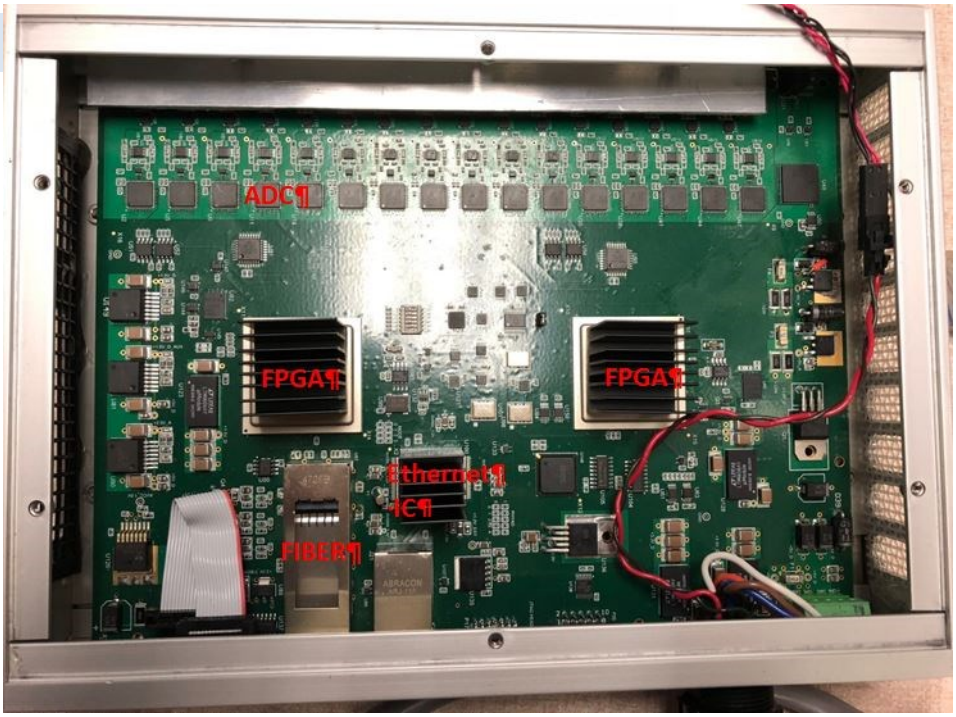
Rear Panel

Front Panel



Rear Panel

EFADC250 Internal Circuits View