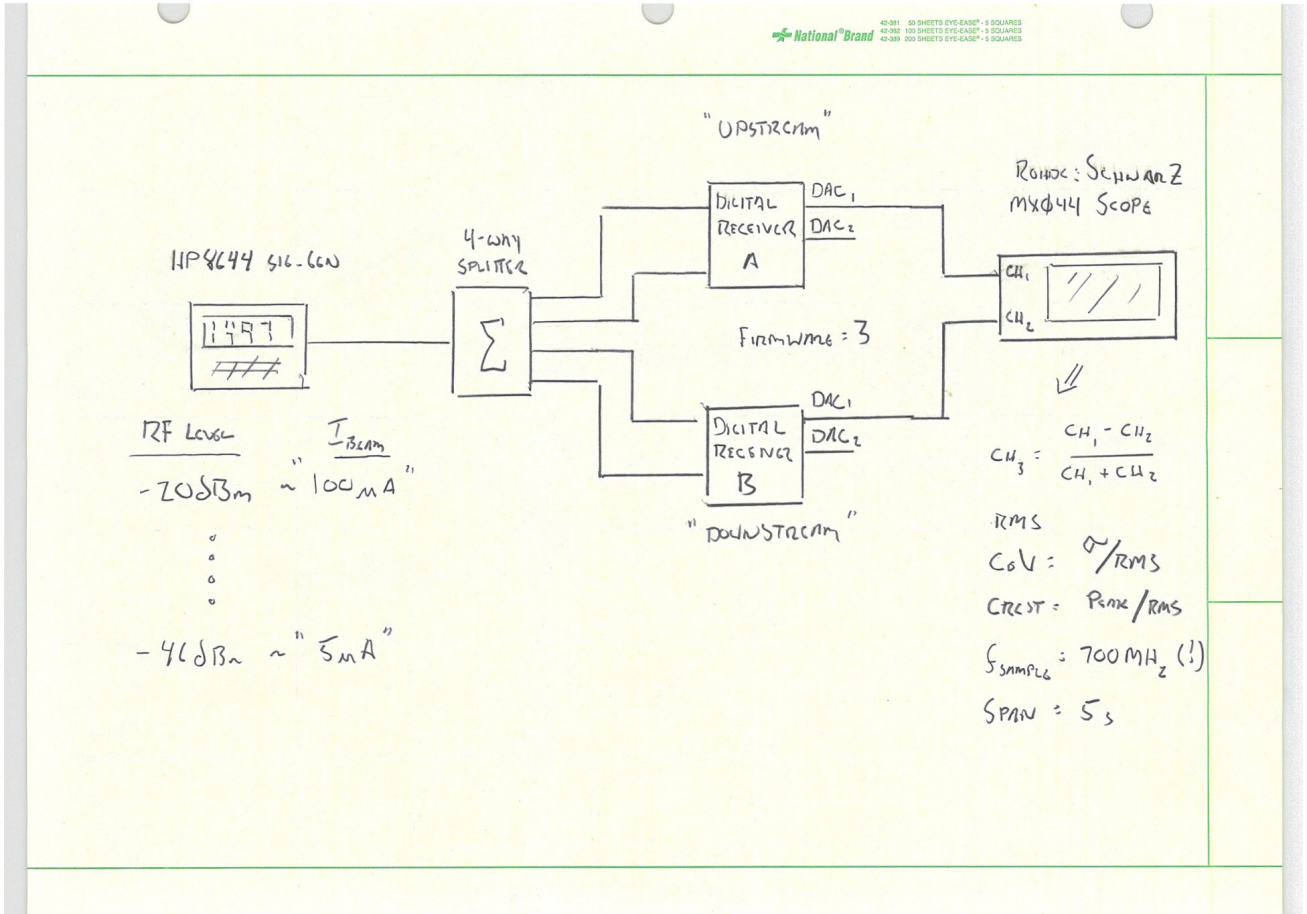
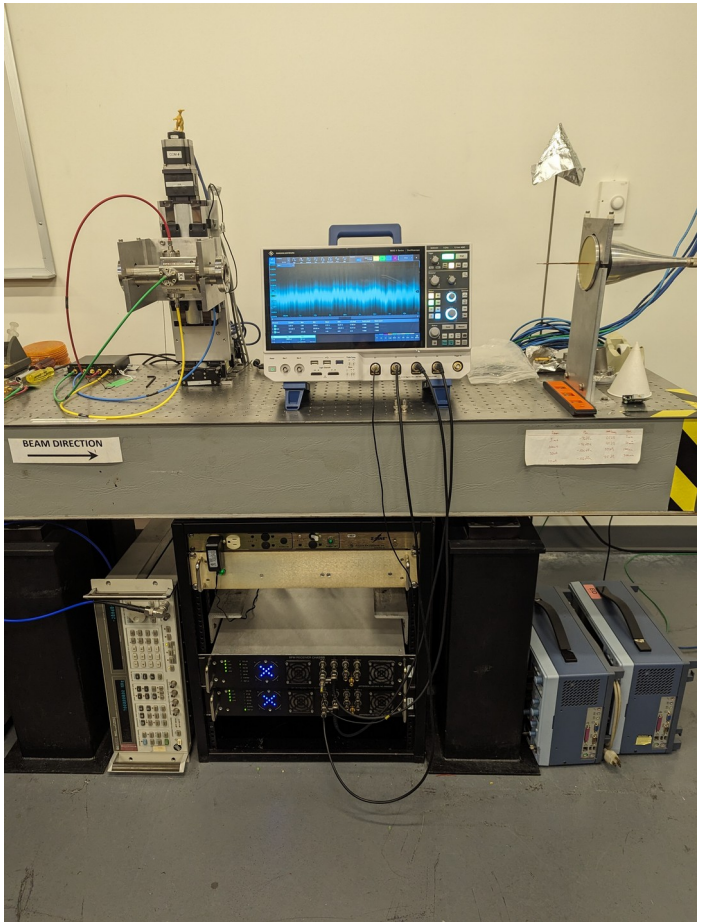
# Input signals band-limited to 20 MHz

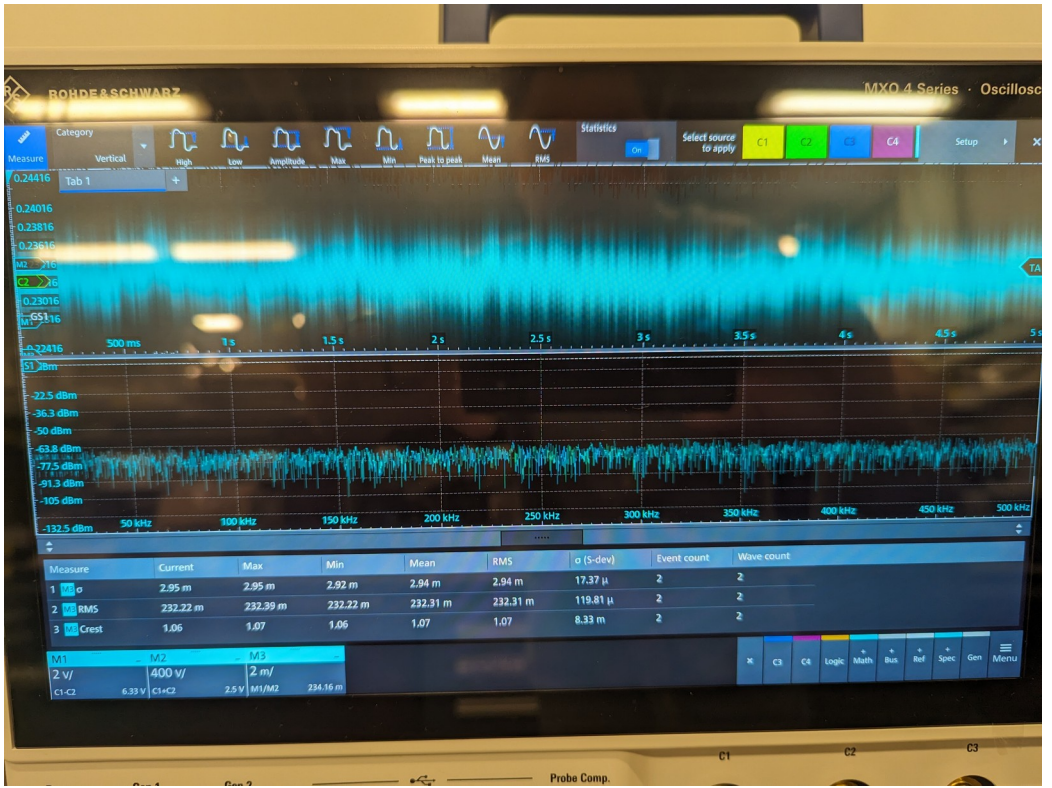


# 5 Second Time Span (500 ms/div)

$$\frac{Rx_A - Rx_B}{Rx_A + Rx_B}$$

$$\frac{Rx_A - Rx_B}{Rx_A + Rx_B}$$ ...with spectrum to 1 MHz

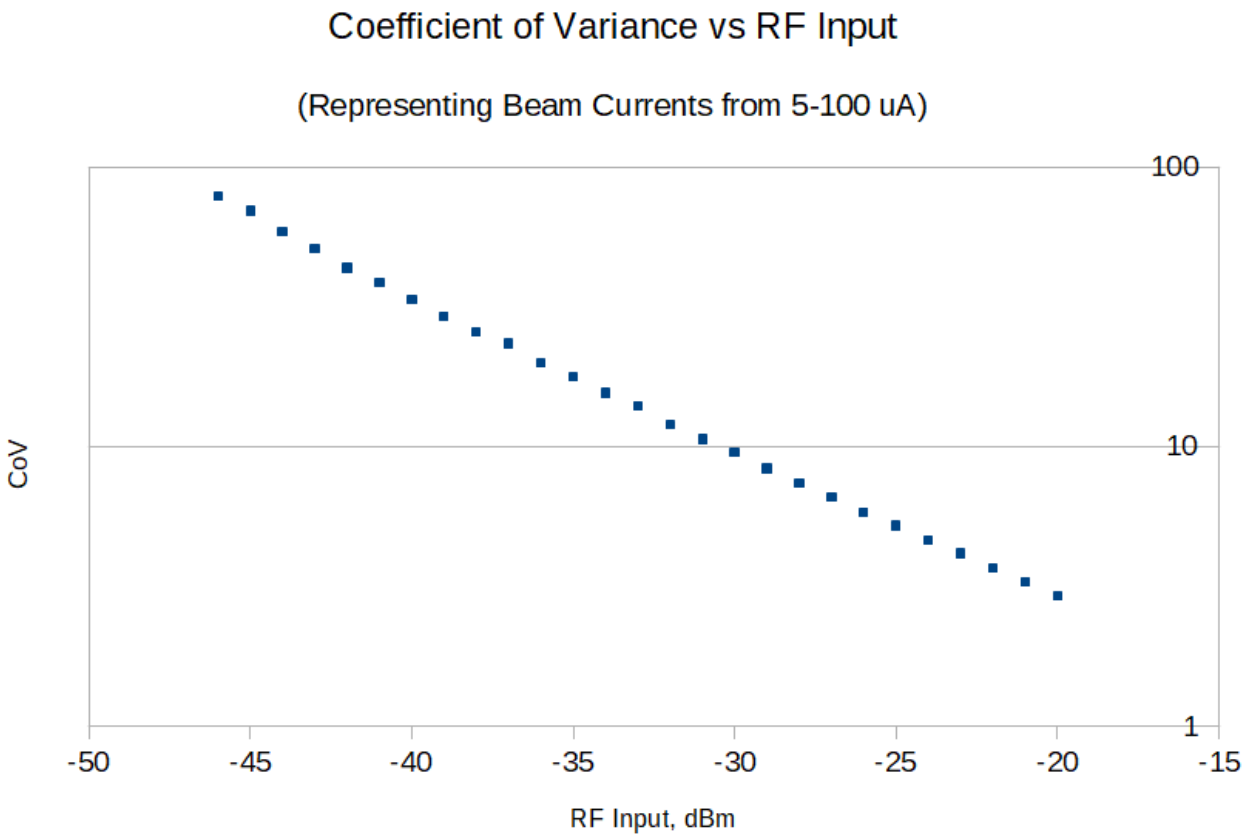
**50 Ohm Test Load on Ch1 and Ch2:**

CoV = 261.16

RMS = 324.72

C.F. = 128

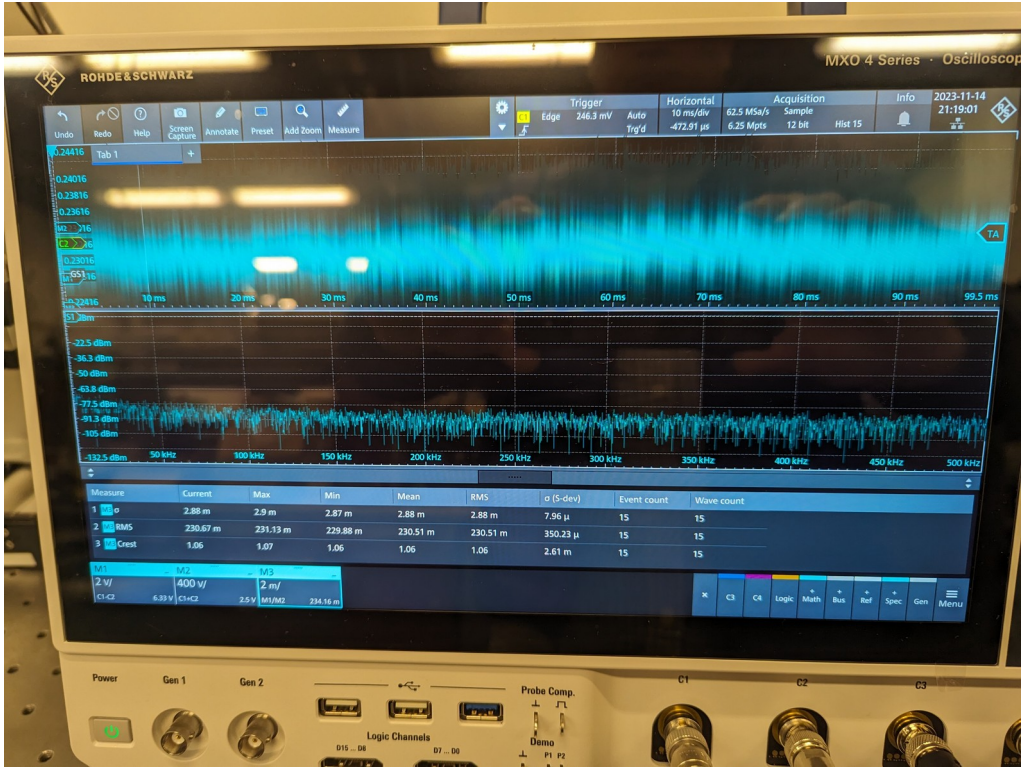
...well within the measurement range



# 100 m-Second Time Span (10 ms/div)

$$\frac{Rx_A - Rx_B}{Rx_A + Rx_B}$$

$$\frac{Rx_A - Rx_B}{Rx_A + Rx_B}$$ ...with spectrum to 1 MHz

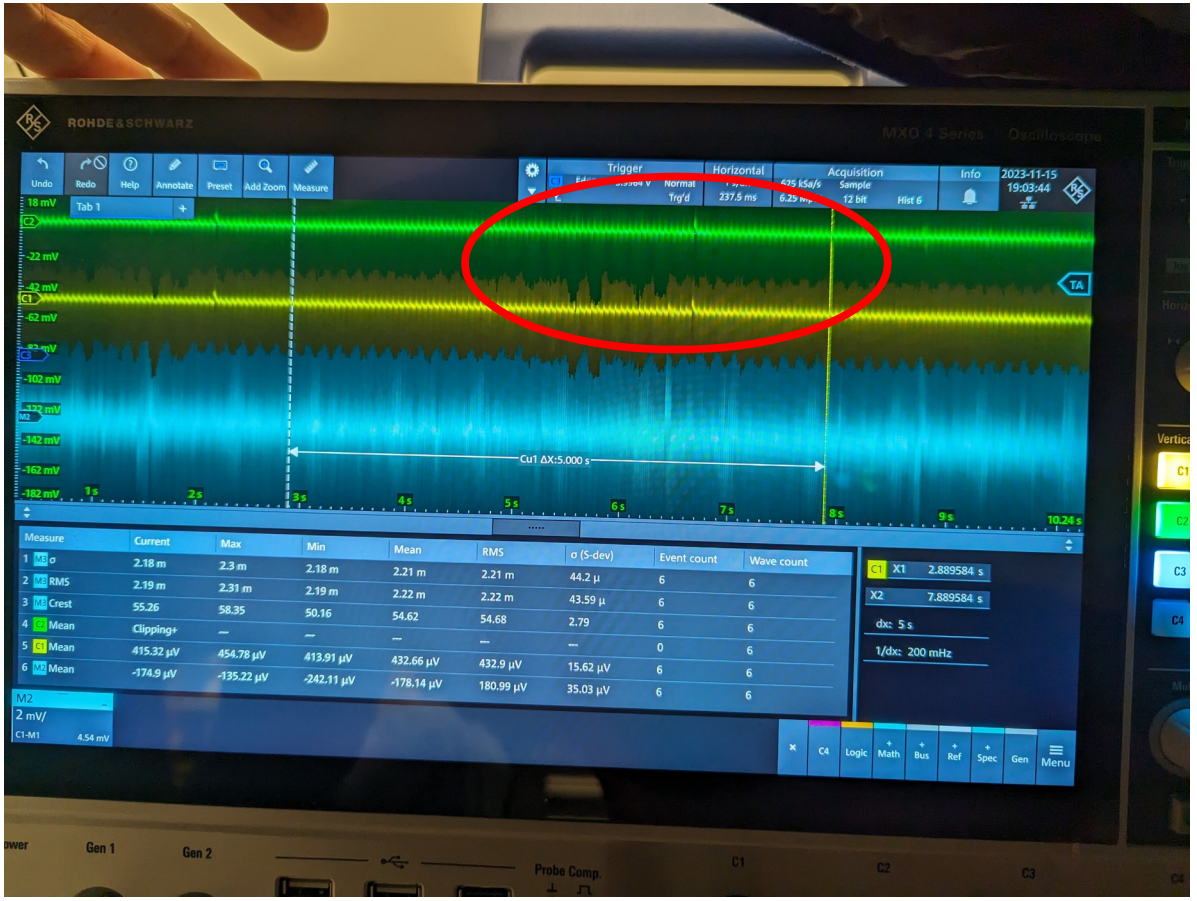



# 10 m-Second Time Span (1 ms/div)

$$\frac{Rx_A - Rx_B}{Rx_A + Rx_B}$$ ...with spectrum to 1 MHz


$$\frac{Rx_A - Rx_B}{Rx_A + Rx_B}$$ ...with spectrum to 15 kHz

# Measurements with Devi




**RF ramp:**
**-22.2 dBm to -20.2 dBm**
**0.01 dB steps**

Ch B (a/c coupled, 5mV/)

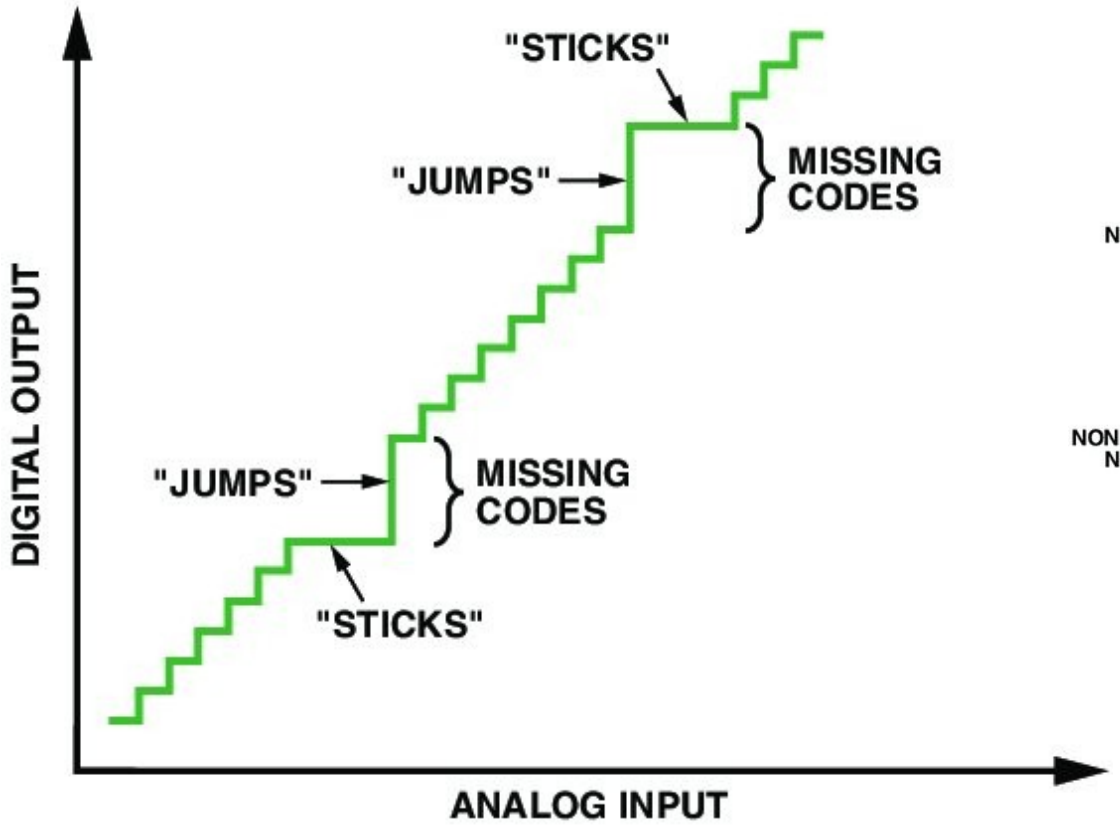
Ch A (a/c coupled, 5mV/)

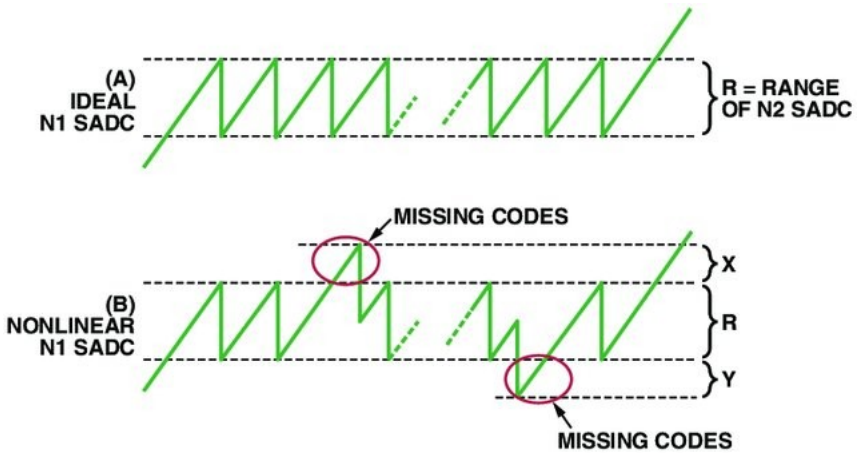
Ch A – Ch B (2 mV/)


“Blip” occurs in same locations, and very close to Devi’s receivers.

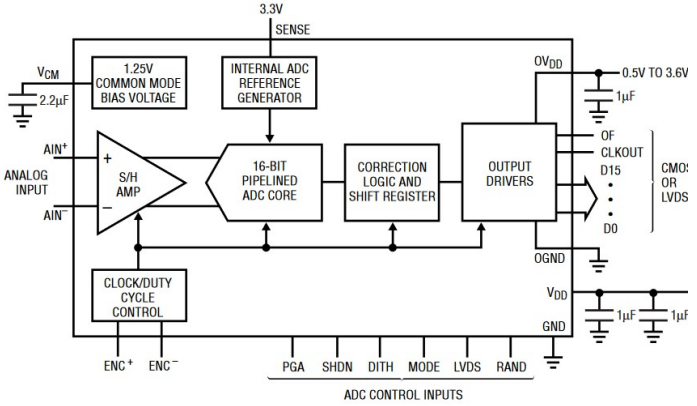
We are using the Unser firmware, so this suggests something ADC/DAC related?

# Possible (likely?) Issue: INL, DNL



LTC2208:

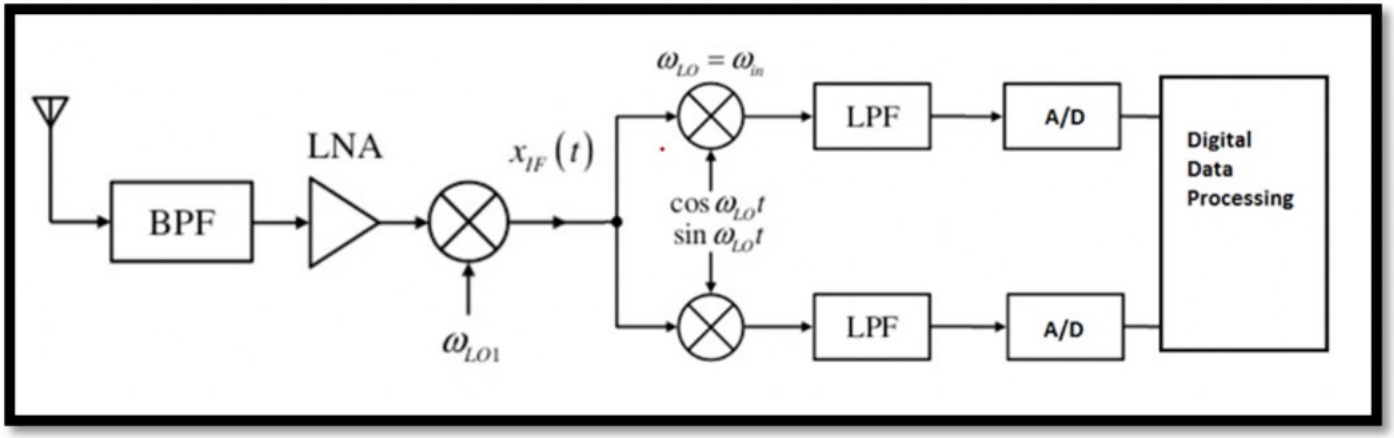



## CONVERTER CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. (Note 4)**

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Integral Linearity Error | Differential Analog Input (Note 5) $T_A$ = 25°C | | | ±1.2 | ±4.0 | LSB |
| Integral Linearity Error | Differential Analog Input (Note 5) | ● | | ±1.5 | ±4.5 | LSB |
| Differential Linearity Error | Differential Analog Input | ● | | ±0.3 | ±1 | LSB |
| Offset Error | (Note 6) | ● | | ±2 | ±8.5 | mV |
| Offset Drift | | | | ±10 | | µV/°C |
| Gain Error | External Reference | ● | | ±0.2 | ±1.5 | %FS |
| Full-Scale Drift | Internal Reference<br>External Reference | | | ±30<br>±15 | | ppm/°C<br>ppm/°C |
| Transition Noise | External Reference | | | 2.9 | | $LSB_{RMS}$ |

# If True….At Least for ADC…..




Consider a non-zero IF architecture….

Input RF rolls through all ADC codes...homogenizing the output I/Q values

...avoids “hammering” same spot on the ADC.

Perhaps consider Max’s dithering for ADC and DAC?