Re-designing the Helicity Board

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March 19, 2009

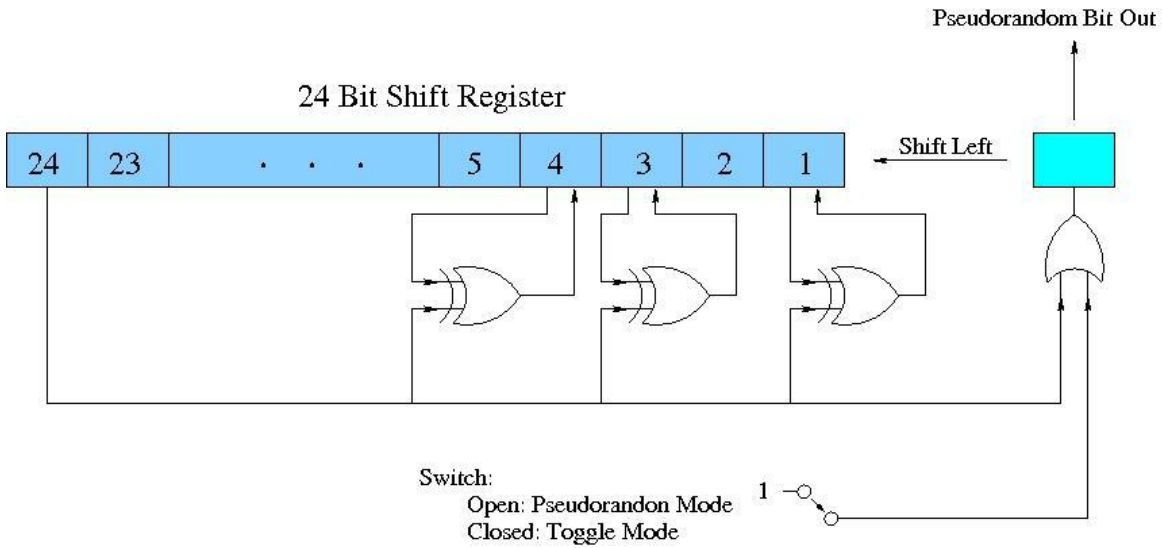
Current Design

Pseudo-Radom Helicity Generator

- ✓ Use 24-bit Shift Register
- ✓ It is Pseudorandom, not “Random” because it is deterministic, once a sequence of 24 helicity states is known, the next states can be predicted, and it repeats its cycle.
- ✓ For any initial seed, there are $2^{24} – 1 = 16{,}777{,}215$ (maximal length) random pairs before the sequence repeats, 13 days for 30 Hz helicity reversal rate.

IB1 = 000000000000000000000001
IB24 = 100000000000000000000000
MASK = 100000000000000000001101
iseed = 101010101010101010101010

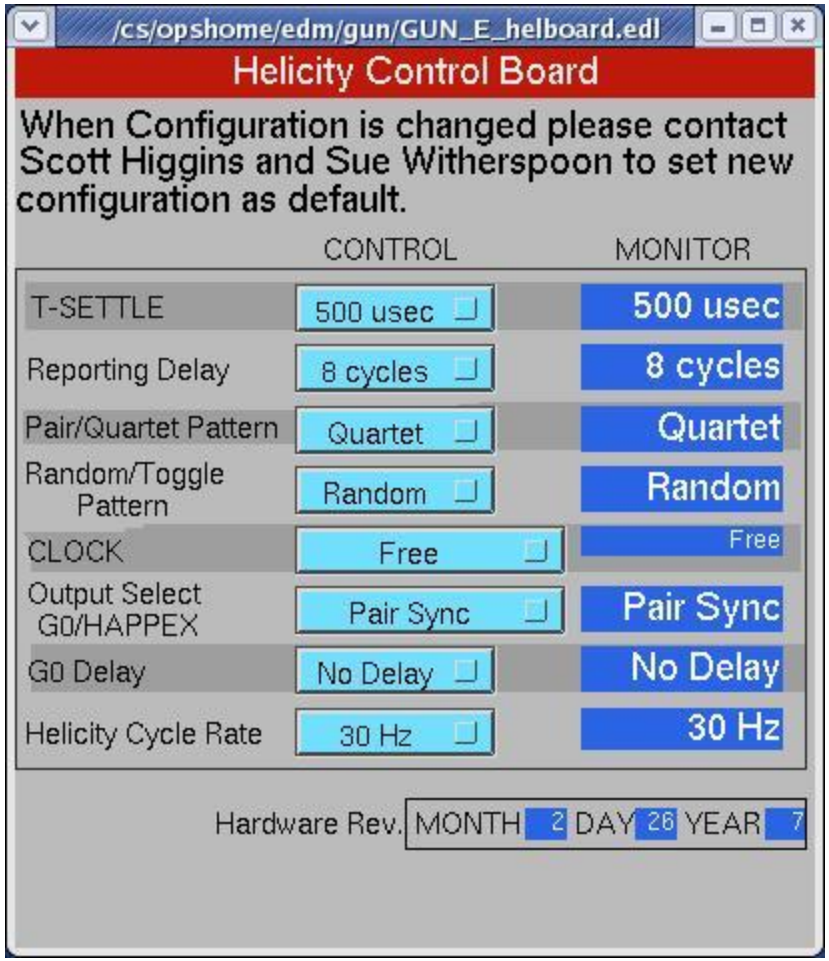
If(iseed & IB24)
{ hel = 1
iseed = ((iseed ^ MASK) << 1) | IB1
(Change all masked bits, shift, and put 1 into bit 1) **}**
else
{ hel = 0
iseed <<= 1 *(Shift and put 0 into bit 1)* **}**



Programming

Software:

1. MPS (T_Settle): 500, 200, 100, and 60 µs
2. Reporting Delay: No Delay, 2, 4, or 8 Cycles
3. Helicity Pattern: Pair (+- or -+) or Quartet (-++- or +--+)
4. Toggle or Random
5. Integration Window (T_Stable): 33.3332 ms or 3.920 ms
6. CLOCK: Free running (f = 29.xx = 1/(T_Settle+33.3332 ms) or 30 Hz Beam Sync (f = 30 = 1/(T_Settle + T_Stable)
7. Output Select: Pair Sync or Helicity Delay (used with G0 dummy Pockels Cell)
8. G0 Delay: No Delay, 1, 2, or 4 Cycles. Delay of helicity signal for Helicity Delay
9. Helicity Cycle Rate: 30 Hz or 250 Hz



Hardware Signals

Inputs:

1. LEMO_0: Beam Sync FIBER_9

Outputs (Fiber-optic Signals):

1. Real time helicity: FIBER_2 to Helicity Magnets, FIBER_10 to Pockels Cell and IAs
2. QRT: FIBER_3 to Halls and Mott Polarimeters
3. MPS: FIBER_4 to Halls and Mott Polarimeters
4. T120: FIBER_5 (¼ T_Stable = 8.3333 ms)
5. Reporting Helicity: FIBER_6 to Halls and Mott Polarimeters, iocse9 and iocse14
6. Pair Sync or Helicity Delay: FIBER_7 to Halls and Mott Polarimeters

More Details

1. We only have two choices of helicity reversal rates at any given time
2. To change the helicity reversal rate, a new code must be uploaded in the field to the helicity generator ioc
3. For both helicity reversal rates, a common choice of T_Settle (4 options)
4. The Helicity Board has 20 MHz internal clock

5. On March 16, 2009: John floated the Helicity Board Crate and the Helicity Magnets Crate.

Cycle Rae (HZ)	MPS (µs)	MPS (Hz)	QRT (Hz)	Helicity (ms)	Helicity (Hz)
30	500	29.58	7.386	33.83	14.78
30	200	29.76	7.451	33.53	14.91
30	100	29.90	7.474	33.43	14.96
30	60	29.94	7.485	33.39	14.97
250	500	226.3	56.56	4.420	113.1
250	200	242.7	60.68	4.120	121.4
250	100	248.8	62.68	4.020	124.4
250	60	251.3	62.81	3.980	125.6

Notes:

1. These values as measured by a scope
2. Signals to Parity DAQ: MPS (T_Settle), QRT, Reporting Helicity, and Pair-Sync
3. The length and frequency of Pair-Sync are identical to Helicity
4. The length of QRT is identical to Helicity
5. The integration window is generated by MPS AND Pair-Sync
6. The integration window for 30 Hz is 33.33 ms and for 250 Hz it is 3.92 ms

Notes:

1. The 30 Hz Beam Sync signal is missing

2. On Monday October 13, 2008, the Helicity Board was re-programmed:
   - ✓ T_Settle: 10, 60, 100, 500 μs
   - ✓ Helicity Cycle Rates: 30 Hz or 1 kHz
   - ✓ Integration Window (T_Stable) is 980 μs for 1 kHz

3. Parity ADC internal programming:
   I. For 30 Hz helicity reversal:
      - ✓ Acquisition starts 40 μs after the gate begins
      - ✓ There are 4 blocks of 4161 samples/block for each gate.
      - ✓ The acquisition time is 33.328 ms

   II. For 250 Hz helicity reversal:
      - ✓ Acquisition starts 40 μs after the gate begins
      - ✓ There are 4 blocks of 485 samples/block for each gate.
      - ✓ The acquisition time is 3.880 ms

   III. For 1 kHz helicity reversal:
      - ✓ Acquisition starts 40 μs after the gate begins
      - ✓ There are 4 blocks of 117 samples/block for each gate.
      - ✓ The acquisition time is 936 μs

Cycle Rae (HZ)	MPS (µs)	MPS (Hz)	QRT (Hz)	Helicity (ms)	Helicity (Hz)
30	500	29.58	7.386	33.83	14.78
30	100	29.90	7.474	33.43	14.96
30	60	29.94	7.485	33.39	14.97
30	10	29.99	7.496	33.34	14.99
1000	500	675.7	168.9	1.480	337.8
1000	100	925.9	231.5	1.080	463.0
1000	60	961.5	240.4	1.040	480.8
1000	10	1010	252.5	0.9900	505.1

Notes:

1. These values as measured by a scope
2. The integration window for 1 kHz is 0.980 ms

Why Re-designing the Helicity Board

✓ Clean up leftovers from G0. Drop the “MPS” label!

✓ Make it easy to program and easy to choose any reversal rate and any T_Settle time

✓ Change the Shift Register to 30-Bit. The sequence will repeat every 25 days for 1 kHz helicity reversal rate.

✓ Add another pattern: Octet (+-+--+-+ or -+-++-+-)

✓ We will need new fiber output signals:

- 2 additional outputs for 4-way IA feedback scheme where the applied IA voltage is determined not only from the current helicity state but also from the previous helicity state.

- Output of the Helicity Board Clock signal.

New Design

Hardware Signals

Inputs (Fiber-Optic TTL Signals):

1. 30 Hz Beam Sync
2. Spare input

Outputs (Fiber-Optic TTL Signals):

1. Real Time Helicity (two outputs):
    I. Standard: Pockels Cell and IAs
    II. Complementary: Helicity Magnets

2. Delayed Helicity: Halls and Polarimeters, iocse9 and iocse14

3. T_Settle: Halls and Polarimeters

4. Pair Sync: Halls and Polarimeters

5. Multiplet Sync: now QRT - start of a Quartet or Octet, Halls and Polarimeters

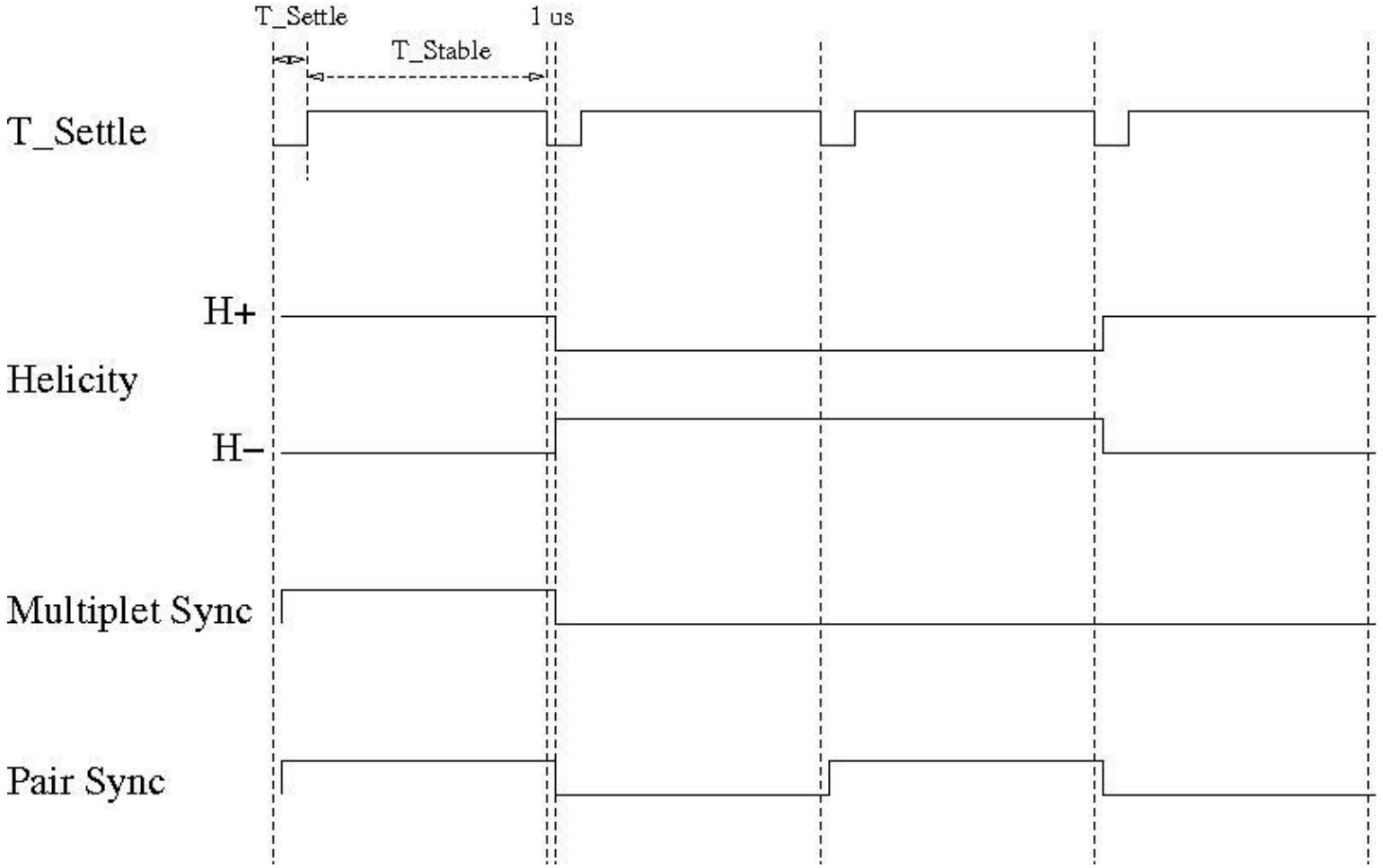
6. IAs Control (two outputs): IA1 and IA2, indicate current and previous patterns

7. 20 MHz Internal Clock: Halls and Polarimeters

8. Few Spare Fibers

Timing of Signals

1. The transition to T_Settle should start 1.00 µs before all other signals. Now it is 100 ns; this time is too short



Pseudo-Radom Helicity Generator

✓ Use 30-bit Shift Register

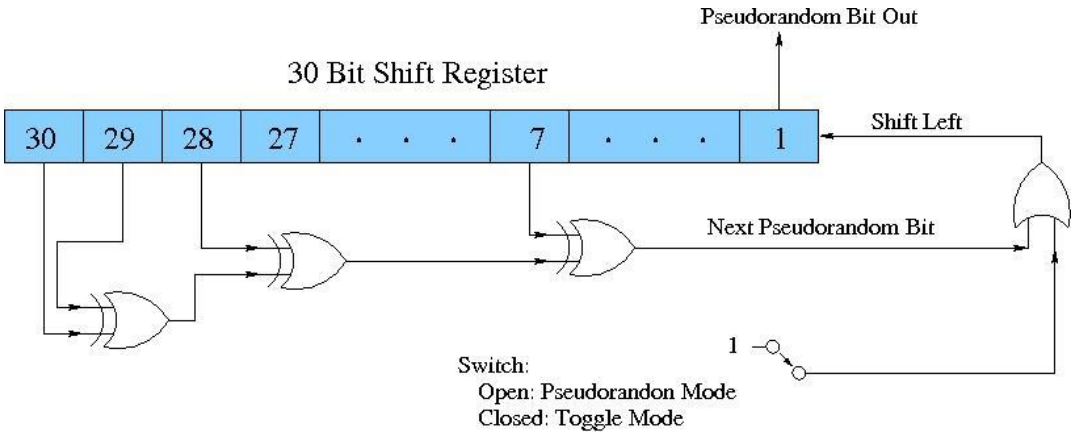
✓ It is Pseudorandom, not “Random” because it is deterministic, once a sequence of 30 helicity states is known, the next states can be predicted, and it repeats its cycle.

✓ For any initial seed, there are $2^{30} – 1 = 1{,}073{,}741{,}823$ (maximal length) random pairs before the sequence repeats, 25 days for 1000 Hz helicity reversal rate.

```
UInt_t bit7    = (fgShreg & 0x00000040) != 0
UInt_t bit28   = (fgShreg & 0x08000000) != 0
UInt_t bit29   = (fgShreg & 0x10000000) != 0
UInt_t bit30   = (fgShreg & 0x20000000) != 0

UInt_t newbit = (bit30 ^ bit29 ^ bit28 ^ bit7) & 0x1

fgShreg = newbit | (fgShreg << 1 ) & 0x3FFFFFFF
```



Programming

1. Select Toggle or Random

2. Choose Reporting Delay: n Cycles, n = 0 … 1000 cycles

3. Select Helicity Pattern: Pair (+- or -+), Quartet (-++- or +--+), Octet (+--+-++- or -++-+--+)

4. Select Clock:
   I. Free:
      - Choose T_Settle value between 10 µs - 1000 µs
      - Choose Integration Window (T_Stable) value between 400 µs – 1,000,000 µs
      - Display Helicity Reversal Rate: f = 1/(T_Settle + T_Stable)

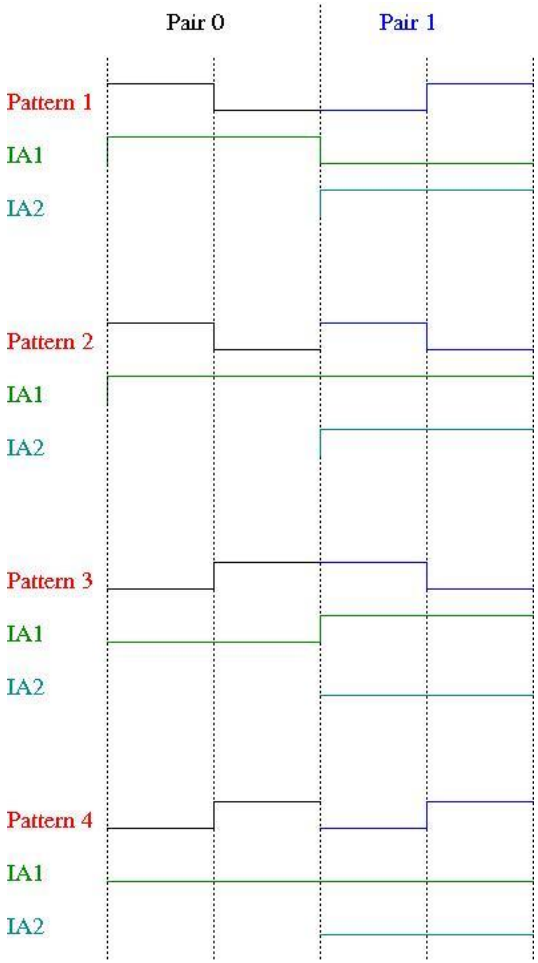
   II. 30 Hz Beam Sync: Force phase-lock during T_Settle
      - Choose T_Settle value between 10 µs - 1000 µs
      - Choose Helicity Reversal Frequency f: 30, 120, or 240 Hz
      - Display T_Stable: T_Stable= 1/f - T_Settle

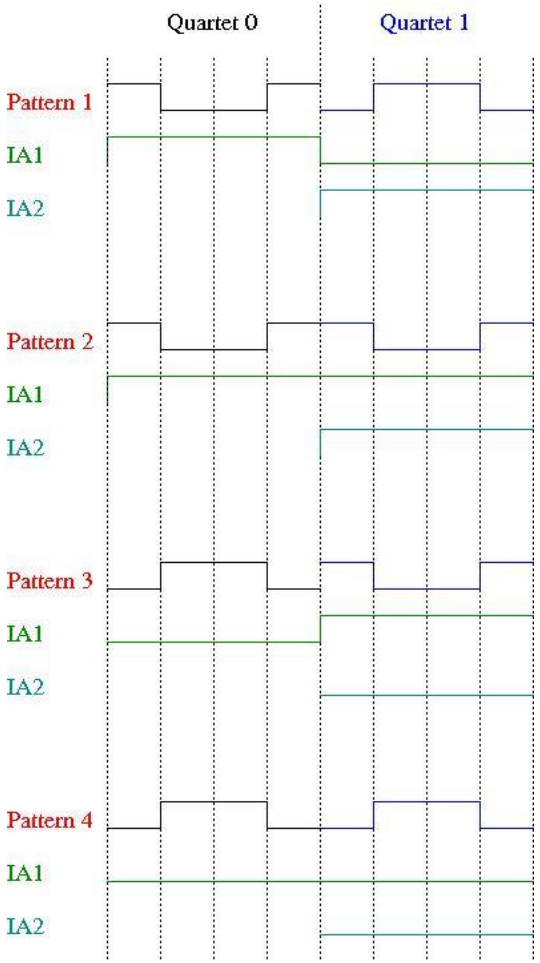
How to Reduce 60 Hz Line Noise?

1. Choose T_Stable such that: f>1 kHz

2. Integrate over 60 Hz noise:
    - Choose T_Stable = 33,333 µs (exactly two 60 Hz cycles).
    - Choose T_Stable + T_Settle = 8,333 µs (half 60 Hz cycles), select Quartet Pattern, line-phase locked. Then, A = +1-2-3+4.
    - Choose T_Stable + T_Settle = 4,167 µs, select Octet Pattern, line-phase locked. Then, A = +1-2-3+4-5+6+7-8.

IAs Outputs: Pairs, Quartets, & Octets





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New Fibers Needed?

1. 2 new fibers needed from IN01B05 to the Laser Table: IA1 and IA2

2. Use the existing T120 fibers to carry the 20 MHz Clock signal from IN01B05 to the Parity DAQ in IN02B24 and to the Parity DAQ in Hall C