

Mott Detectors and Data Acquisition System

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The Mott detectors consist of four sets of plastic scintillator detectors: two horizontal (Left and Right) and two vertical (Up and Down). The four sets are identical and each set is made of two detectors: DE and E detectors. The DE detector is made of EJ-212 plastic scintillator of the size 1 mm x 1 inch x 1 inch. The detector is glued to an Acrylic Light Guide (0.125 inch x 1 inch wide x 2 inch long). The light guide is glued to 1-inch photomultiplier tube (PMT) (Hamamatsu R6427 in an H7415 Assembly) – see Figure 1. The E detector is made of EJ-200 plastic scintillator cylinder of the size 3 inch diameter x 2.5 inch long painted with EJ-510 with one end clear which was glued to a 3-inch PMT (Hamamatsu R6091 in an H6559 Assembly) – see Figure 2.

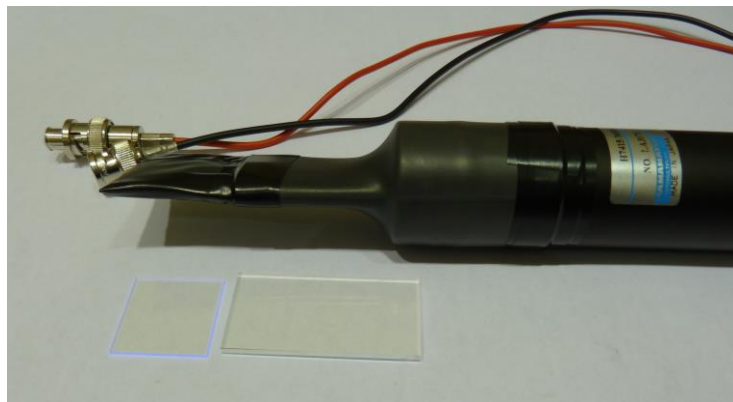


Figure 1: DE detector.



Figure 2: E detector (before wrapping it with black tape).

DE-E detector set (shown in Figure 3) is designed to eliminate signal from gammas where the detection efficiency in the thin DE detector is very small. For electrons, about 10 keV is deposited in the DE detector while the rest of its energy is deposited in the E detector. The PMTs HV are adjusted such that signals of ΔE and E are about -200 mV. The DE PMT HV is about -1300 V while the E PMT is operated at about -1200 V. Figure 4 shows an E raw signal (top) and a DE raw signal (bottom).

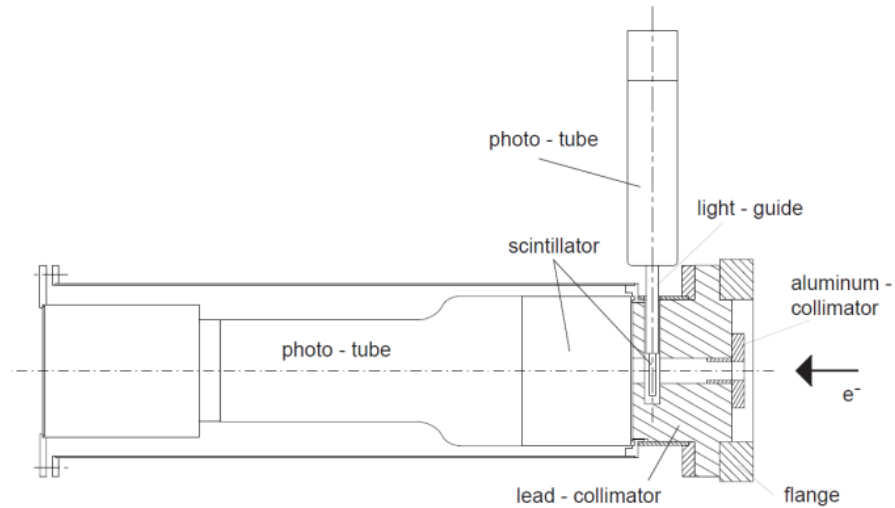


Figure 3: Mott detector assembly.



Figure 4: E and DE raw detector signals.

Figure 5 shows the electronic logic diagram from the PMT all the way to the Data Acquisition readout. The DE detector signal is delayed by 48 ns using a cable delay then sent to a linear fan-out Philips Scientific NIM Module 748. A copy of the detector signal is readout by a Flash Analog to Digital Converter (FADC). Another copy is sent to 715 Constant Fraction Timing Discriminator. A third copy is sent to 705 Octal Discriminator that generated a veto signal with thresholds of -450 mV (more than twice the size of signal from individual Mott electron). This veto signal is then used to eliminate any pileup events in the DE detector which turns out to be very negligible. There are two outputs from the 715 Timing Discriminator: one output goes to a Struck SIS3801 scaler, the second output goes to Philips Scientific Logic NIM Module 754 to perform a coincidence between the DE and E detectors.

The E detector signal is sent to a linear fan-out where one copy is sent to FADC while the other copy is sent to a Timing Discriminator. The timing discriminator has two outputs: one to the scaler and the other to the logic AND module to generate the coincidence signal from a set of DE-E detectors. The coincidence signals are then sent to scalars and to Philips Scientific Logic NIM Module 754 to perform an OR with the other three detector sets.

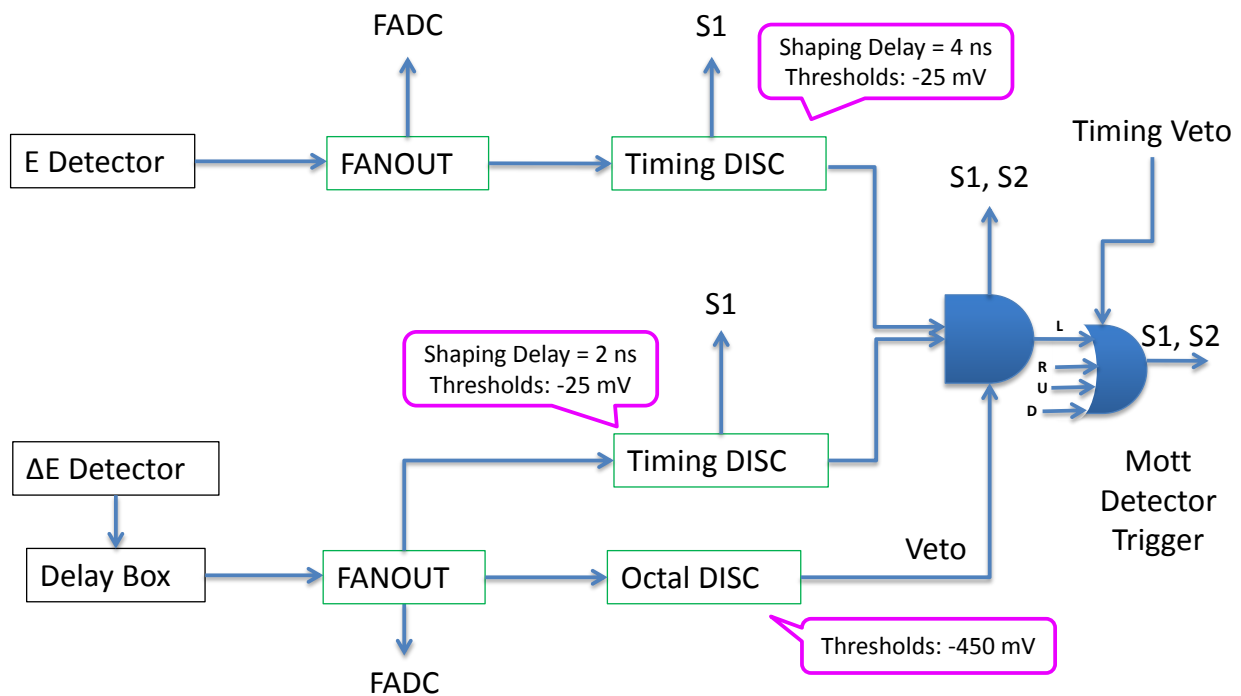


Figure 5: Path of DE and E signals from one set of detectors. The four sets of detectors have identical paths and are combined with an OR logic module.

The four sets of detector are then combined with an OR logic NIM module 754. There are two outputs from this module: one goes to scalars to count the number of Mott events in the four detector sets and one (labeled as Mott Detector Trigger) is used as an input to the Data Acquisition trigger system. The timing veto to eliminate the dump

events is implemented using this module. The timing veto signal of a width of 12 ns is generated from the 31 MHz laser-timing signal.

The Data Acquisition system (DAQ) is VME based and used MVME6100/VxWorks from Motorola during Run I. Before Run II, the DAQ was upgraded to use Intel/Linux VME Single Board Computer (SBC) model VX915 from Concurrent Technologies. In addition to the control board, the VME crate (CAEN VME64X VME8200) has the following boards: Trigger Interface and Distribution (TID) Module made by Jefferson Lab Data Acquisition Group, an FADC and its Distribution Board, also made at Jefferson Lab, CAEN v775 Time to Digital Converter (TDC), and two Struck SIS3801 scalars (S1 and S2).

The TID is responsible for providing a low-jitter system clock and fixed latency trigger signals for the Front-end readout boards in the VME data acquisition crate. We have two trigger signals: a Mott Detector Trigger signal (shown in Figure 5) that is used to collect (the random) Mott events and Helicity Trigger signal that runs at a fixed rate and can be used to read the scalars' counts per helicity window (to measure the helicity correlated charge asymmetry, for example). If the TID is not busy reading out a previous event, it accepts the current event and generates a logic signal called L1A. This signal is used to trigger the readout of the FADC, to start the TDC and to stop/start S2 Scaler (scaler Load-Next-Event LNE signal).

The FADC is a 250 MS/s (Samples/second) 12-bit ADC that is used to sample the detector signals similar to a digital oscilloscope. It has 16 channels input. The eight channels used for the Mott detectors PMT signals have -500 mV full-range. Figure 6 shows an example of the 4 ns samples for few Mott events in the E detectors. For every Mott event in any of the four detector sets, 50 samples from each of the 8 FADC channels for all the four detector sets are part of the readout.

How is the energy calculated from FADC? For each Mott event, 50 samples of the detector raw signal are written to the data file. In the analysis, for each event, the first 10 samples are used to calculate the average pedestal (p) ($p = \frac{1}{10} \sum_{s=0}^9 FADC_Sample_s$) and the energy (in units of channels) is calculated by summing the samples from 10 to 49 with pedestal subtraction, $E = \sum_{s=10}^{49} (FADC_Sample_s - p)$.

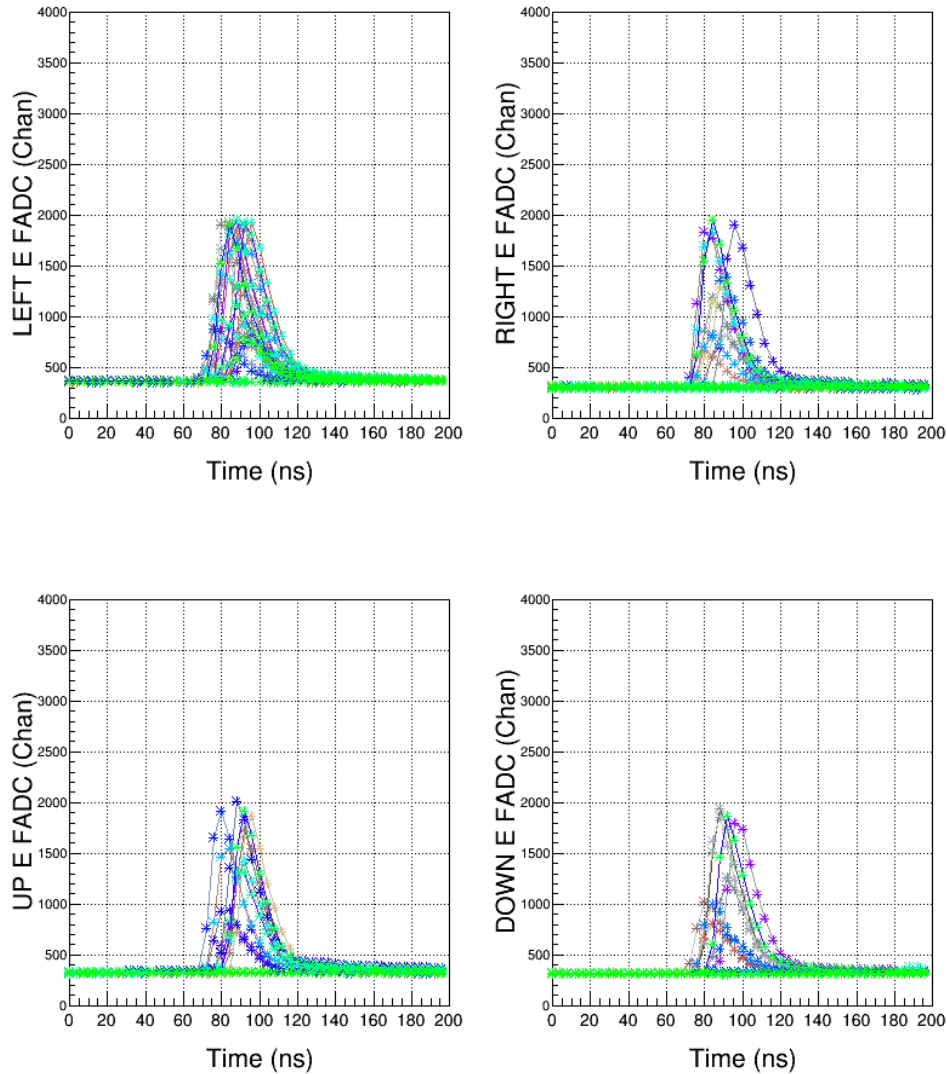


Figure 6: FADC raw 50 samples (every 4 ns) of E detector signals for few Mott events in each detector set.

The TDC has a full scale of 134 ns and a bin resolution of 34 ps/channel. The TDC is operated in Common Start Mode where the start is the TID L1A signal. Two TDC channels are used to calculate the time-of-flight of Mott electrons. The stop of the first channel comes from the 31 MHz laser system and the stop of the second channel is a copy of the Mott Detector Trigger signal, delayed by 322 ns. Then, the time-of-flight is calculated as $TDC_{CH1} - TDC_{CH2}$. This way, the digitization timing jitter of the TID L1A signal is removed.

Two Struck SIS3801 scalers are part of the DAQ. The first scaler S1 is gated by one of the helicity signals (T_Settle) and always counts when the Pockels Cell HV is stable (i.e., does not count while the Pockels Cell HV is settling after flipping between -2.5 kV and +2.5 kV). The data from S1 are tagged with the helicity state: positive or negative helicity. A voltage signal from a cavity beam current monitor (BCM) is converted to

frequency (VtoF) and fed into one of the channels of this scaler to calculate the beam charge asymmetry.

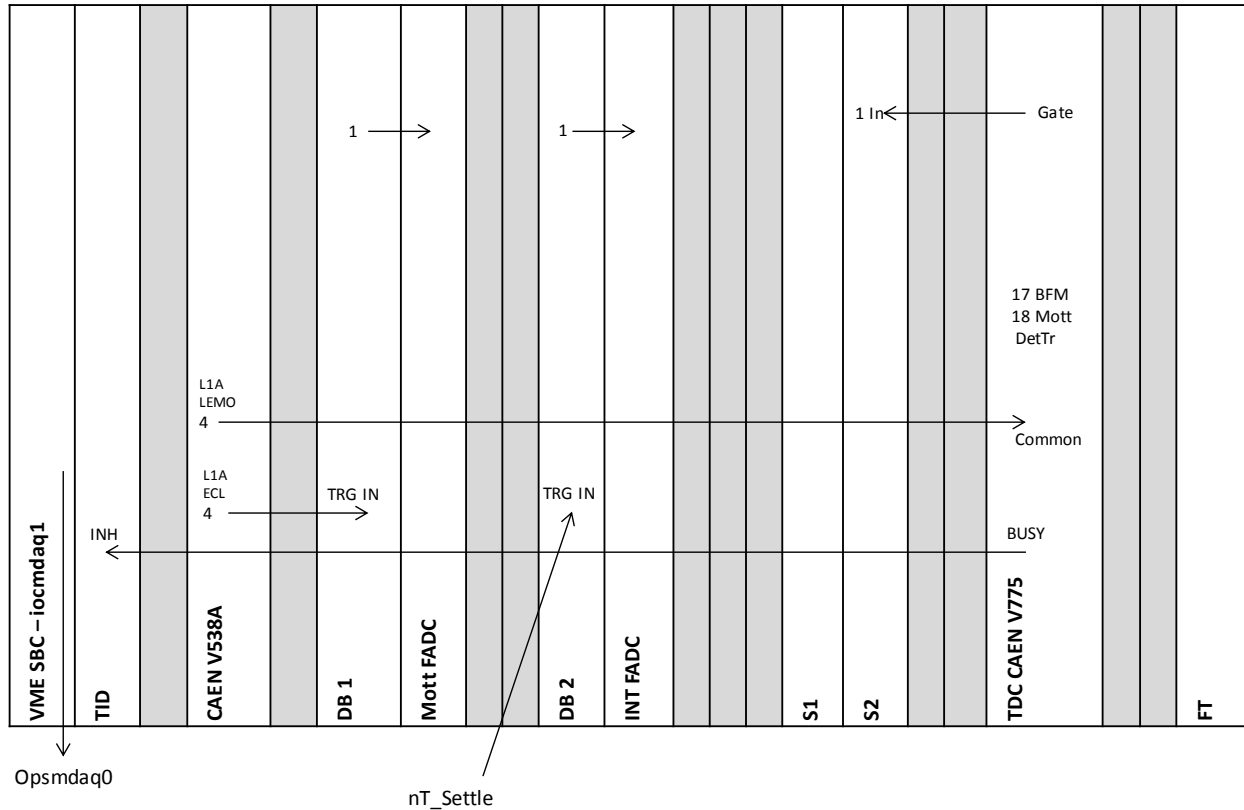


Figure 7: Mott DAQ VME crate.

The second scaler S2 is free running scaler that only counts when the DAQ is running and is readout whenever a Mott event is accepted. Scaler S2 counts the number of Mott Detector Triggers and the number of Accepted Mott Triggers used to calculate the DAQ deadtime for the rate measurements. For each Mott run, the run time is calculated using a 121 kHz clock that is readout with S2 scaler. The accumulated electron charge in each run is calculated from the BCM VtoF readout in this scaler. Data from both scalers are always written to EPICS variables and archived even when the Mott DAQ is not running (albeit, S2 only counts when the DAQ is running). Figure 7 shows a schematic diagram of the Mott DAQ VME crate.

The Helicity signals are generated by a board in an electrically isolated VME crate in the Injector Service Building [1]. The board generates a 0.5 ms “T_Settle” signal to indicate the time when the HV on Pockels Cell changes. This signal goes to zero for 33.33 ms time period “T_Stable” to indicate that the HV on the Pockels Cell is stable (thus, beam helicity is stable) and the Mott events are tagged as good during the stable period. The helicity pattern used is Quartet (+--+ or -+-). The helicity flipping is random and is in real time (no delay between the signal sent to change HV on Pockels Cell and the signal sent to the DAQ to report the helicity). Pattern-Sync signal indicates the start of the Quartet pattern. Figure 8 shows the helicity signals used in the Mott DAQ. The helicity signals are plugged in the FADC Channels 13-16 with -1 V full range and are

used to calculate the Mott asymmetry. The helicity signals are also fed to S1 Control Input to be used to calculate the charge symmetry.

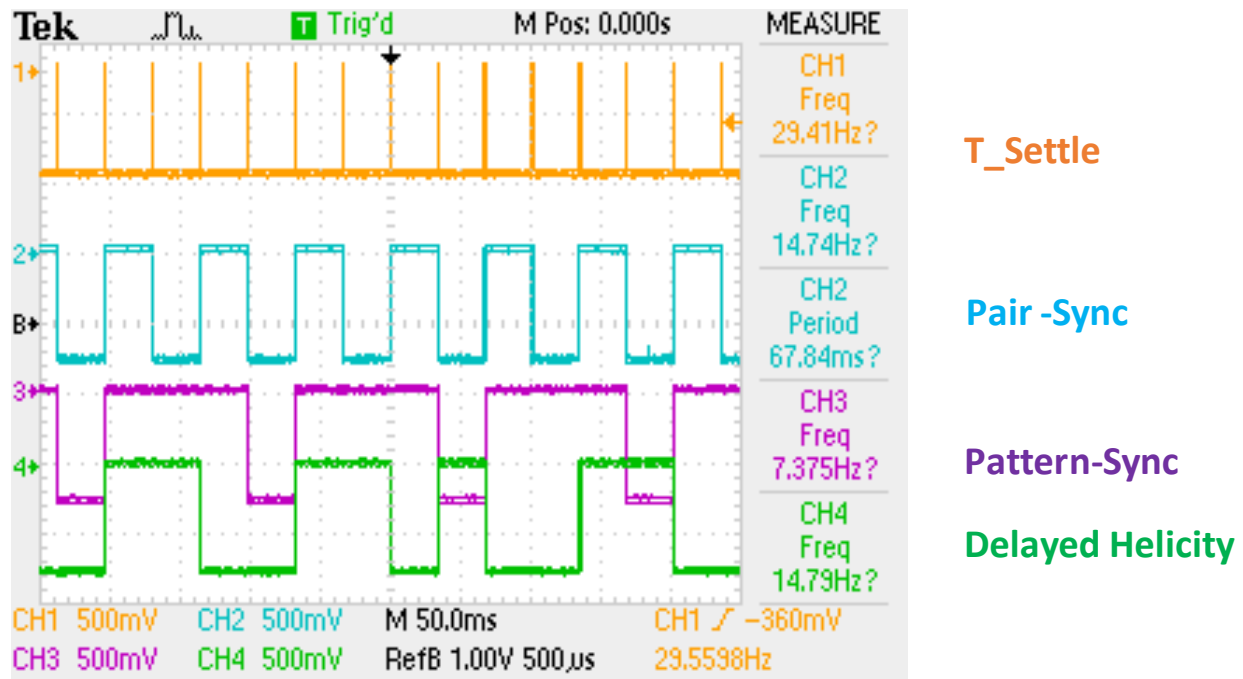


Figure 8: Helicity signals.

We used CEBAF Online Data Acquisition (CODA) [2] software to collect all the information pertain to an event and write it to a data file. The DAQ collects Mott events at a rate of about 2 kHz with 15% deadtime. The deadtime is dominated by the readout of FADC (100 μ s, event-by-event readout – no blocks), TDC (16 μ s) and S1 and S2 (32 μ s). Each data file (run) has few hundreds of thousands of events. Off-line, analysis software goes through all the events and for each event, the data from the FADC, TDC and Scalers S1 and S2 are written to a root file.

References:

- [1] “Helicity Control Board User’s Guide – Programming and Hardware.” R. Suleiman et al. (2010).
- [2] Jefferson Lab data acquisition support group (DAQ group)
<https://coda.jlab.org/drupal/>