JLAB

Silicon Vertex Tracker System Operations Manual

v1.7

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Abstract

This document provides an overview of the CLAS12 Silicon Vertex Tracker (SVT) System and serves as an Operations Manual for the detector. Instructions are provided for shift workers related to basic steps of operating and monitoring the SVT controls, monitoring the detector system and responding to alarms, and knowing when to contact the on-call personnel. More complete details are also provided for SVT system experts regarding the channel mapping to the readout electronics, the cable connections and routing in Hall B, higher-order system operations, and detector servicing. This document also provides references to the available SVT documentation and a list of personnel authorized to perform SVT system repairs and modify system settings.

Table of Contents

1 SVT Overview

This document describes the operating procedures that will be followed to commission and operate the CLAS12 Silicon Vertex Tracker (SVT). In CLAS software SVT is named as BST (Barrel Silicon Tracker). The goal of these procedures is to ensure the quality standards defined by the Technical Design Report (TDR) of the detector; optimize the sequence of operations during construction, installation, and operation in terms of time, manpower, and computing resources; ensure the proper functioning of the SVT before and after installation in Hall B; obtain initial calibration data necessary for the reconstruction of the physics events; determine the performance of the SVT; and optimize the overall detector configuration according to the requirement of the physics runs.

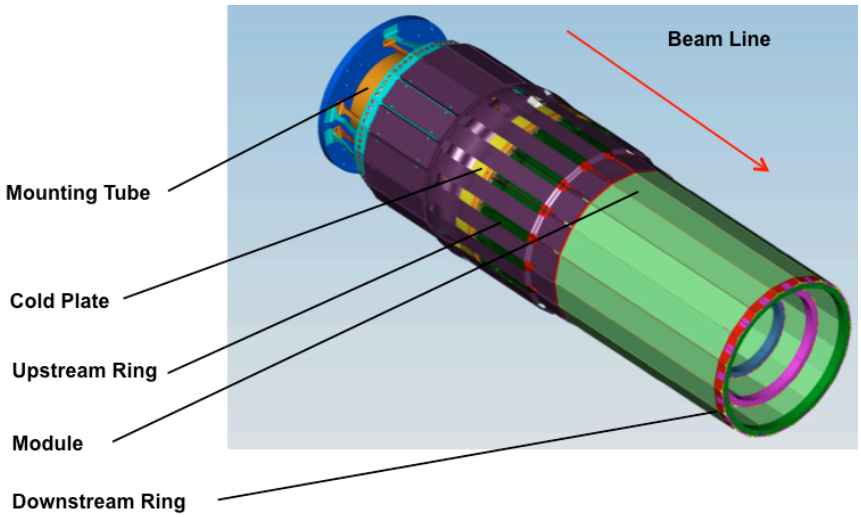


Figure 1 SVT Mechanical Layout

The aim of the tracker is to measure the trajectories of charged particles (tracks) with required momentum, angle, and positional resolution, and with high track reconstruction efficiency.

The SVT (Figure 1), which has a coverage in θ within 35°–125° and a coverage of ~2π in φ, has three polygonal regions, R1–R3, that have 10, 14, and 18 sectors respectively. Each sector contains modules, whose top and bottom sides have three (Hybrid, Intermediate, and Far), 320 μm thick, silicon sensors, which are wire bonded together, a pitch adapter, and a readout hybrid - part of the readout electronics located on the hybrid flex circuit board (HFCB).

The bottom side of the module, closer to the beam, is referred to as the U layer; the top side of the module is referred to as the V layer. Each side of the module has 256 readout strips.

R1–R3 have inner radii of ~65 mm, ~92 mm, and ~119 mm, respectively, with sector numbering as shown in Figure 2.

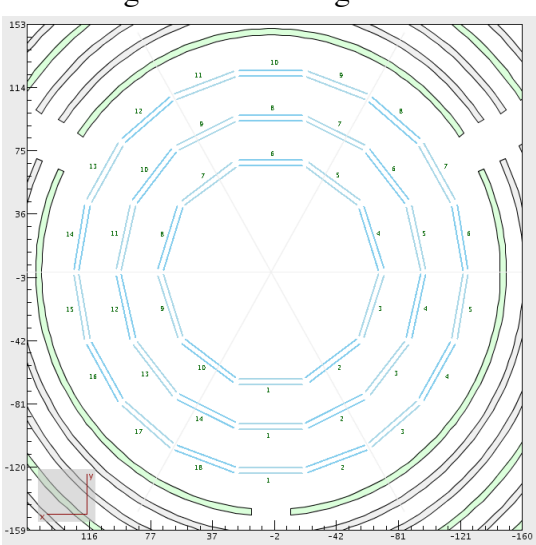


Figure 2 SVT module layout in XY plane

The radial distance Δr between R1 and R3 has been maximized because the momentum resolution goes as Δr^{-2}. To match the absolute momentum resolution of the forward tracking system, the central tracking system's fractional momentum resolution requirement for particles with a momentum of 1 GeV is required to be ~5%—needed to identify a missing pion in exclusive reactions. Table of principal SVT parameters and design values is shown in Figure 3.

PARAMETER	DESIGN VALUE
Number of regions (radii, cm)	3 (65, 93, 120)
Sectors (modules)/region	10, 14, 18
Module dimensions (L x W x T)	41.9 cm x 4.2 cm x 0.39 cm
Number of silicon layers/module	2 (*U, V*)
Strip layout	(0°— 3°) Graded angle
Sensor thickness	320 µm
Readout pitch	156 µm (hybrid side)
Number of readout channels/module	512
Total number of readout channels	21,504
Readout ASIC	FSSR2
Backend electronics	Custom-made VXS cards
Angular coverage θ	35°–125°
Angular coverage Φ	~2π
Spatial resolution	50-65 µm
Momentum resolution	~6%
θ resolution	10–20 mrad
ϕ resolution	~5 mrad
Designed to operate at a luminosity of	10^{35} $cm^{-2}s^{-1}$

Figure 3 Table of SVT parameters

2 Information for Shift Workers

2.1 *Shift Worker responsibilities*

The shift worker in the Hall B Counting House has the following responsibilities with regard to the SVT system:

1. Updating the Hall B electronic logbooks with records of problems or system conditions (see Section 2.1.1).
2. Contacting SVT system on-call personnel for any problems that are discovered (see Section 2.1.2)
3. Responding to SVT system alarms from the Hall B alarm handler (see Section 2.1.3).
4. Turning on or off the high voltage (and low voltage after the trip or if requested by the expert) for the SVT system using the power supply control interface (Figure 9).
5. Monitoring the SVT Slow Controls status, post plot of current stability in the HBSVT elog once per shift (see Section 2.4.1).
6. Monitoring data quality and detector performance using clas12mon under BST tabs and post monitoring plots in HBLOG (see Section 2.4.2).

2.1.1 Updating the Logbook

The electronic logbook (or e-log) [https://logbooks.jlab.org/book/hbsvt] is set up to run on a specified terminal in the Hall B Counting House. Shift workers are responsible for keeping an up-to-date and accurate record of any problems or issues concerning the SVT

system. For any questions regarding the logbook, its usage, or on what is considered to be a “logbook worthy” entry, consult the assigned shift leader.

2.1.1 Common issues and actions to take before calling the expert

All issues should be reported in the HBLOG and HBSVT logbooks with screenshots and detailed description. Use “notify” field in the elog to add SVT expert email address.

2.1.1.1 EPICS IOC communication failure

EPICS IOC communication issue will result in magenta color of the SVT detector status in clascss and “disconnected” status in the SVT Overview (see Figure 4).

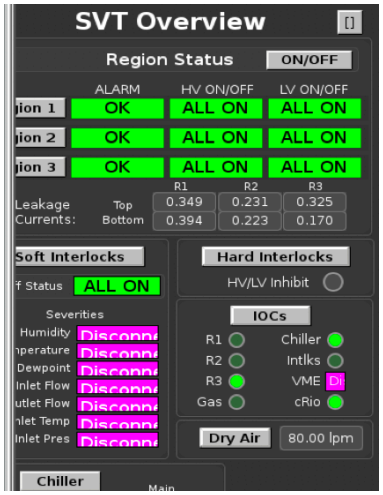


Figure 4 VME IOC communication issue

Actions:

- Open clascss menu: IOC-IOC Health-VME, see Figure 5
- Press “Reboot” under the “hard reboot” column, for iocvmesvt raw
- Wait 3-5 minutes and check magenta colors to become green
- If after 5 min the issue is not solved, call the slow controls expert

Figure 5 IOC VME Health menu

2.1.1.2 Freezing SVT plots

SVT plots (under the SVT Overview, top right corner menu button) can become frozen.

Actions:

- Open IOC menu from the SVT Overview, see Figure 22
- Press “Reboot” under the “hard reboot” column, for iocsoftsvtR2 raw
- Wait 3-5 minutes
- If after 5 min the issue is not solved, call the slow controls expert

2.1.1.3 Front end readout chip latch up

Mon12 online monitoring histograms should be checked and compared with previous runs using comparison tool at https://clas12mon.jlab.org/mon12/histograms/

Latch ups will result in zero hit occupancies in CD summary and BST Hit Maps histograms as shown in Figure 6.

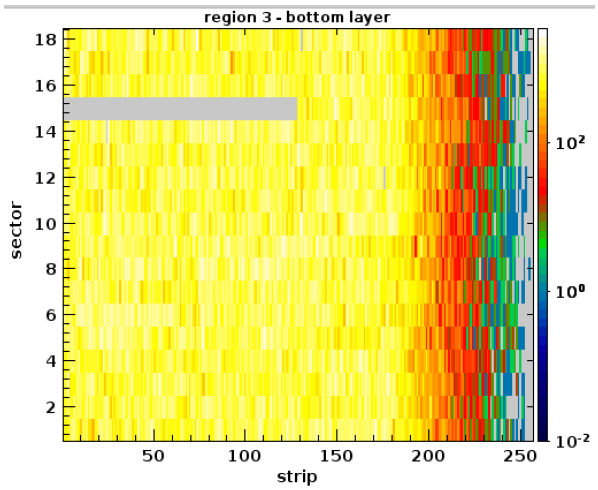


Figure 6 Example of chip latch up (region 3, sector 15, first chip)

Actions:

- stop the run
- reboot SVT crate controllers:

  roc_reboot svt1

  roc_reboot svt2

- configure, download, and start a new run

2.1.1.4 SVT module power up issue

Some HV channels could fail to ramp up or ramp down when “HV ON” or “HV OFF” command issued (Figure 9). This will result in “mixed” state of the region in the SVT Overview.

Actions:

- Repeat last command (press HV ON or HV OFF)
- If the issue is not solved, use individual module power supply control menu as show in Figure 13

2.1.2 Contacting SVT System Personnel

As a general rule, shift workers should spend no more than 10 to 15 minutes attempting to solve any problem that arises with the SVT system. At that point they should contact the assigned SVT/CVT on-call expert to either provide advice on how to proceed or to address the problem.

This document is divided into a section for shift workers and SVT system experts. **Only SVT system experts are authorized to make changes to the SVT parameter settings, to work on the hardware or electronics, or to modify the SVT system software.** This division between shift worker responsibilities and expert responsibilities is essential to maintain in order to protect and safeguard the equipment, to ensure data collection is as efficient as possible, and to minimize down time. If the shift worker has any question regarding how to proceed when an issue arises, the shift leader should be consulted.

2.2 *Slow Controls*

The SVT slow controls system is accessed through CLAS CS Studio user interface to the EPICS slow controls. It allows powering up and down the SVT LV and HV power supplies, access individual power supply channels, and operate the cooling and gas purging system.

To start the clas CSS slow controls GUI open the terminal on the clon machine and run the command "**clascss**". Select "CVT" menu button menu and choose submenu "SVT Overview". This will bring up the window with SVT controls and status info (Figure 7).

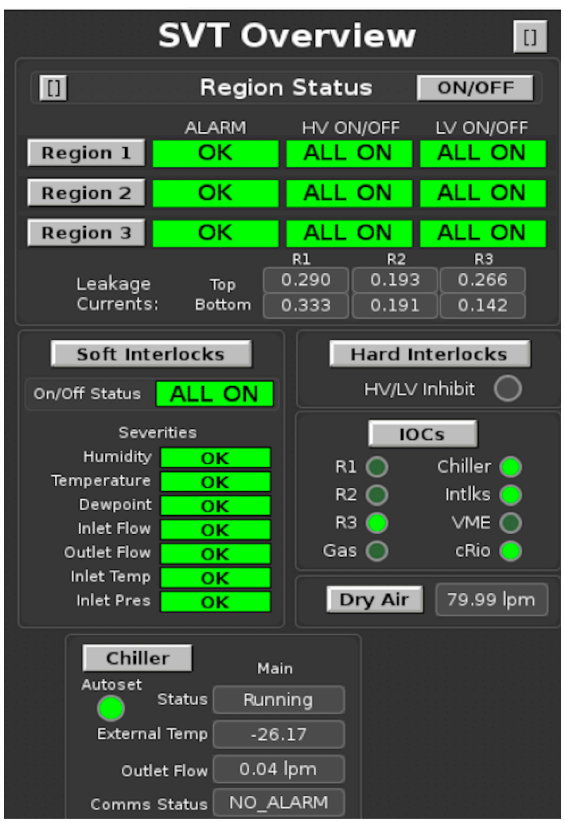


Figure 7 SVT Overview

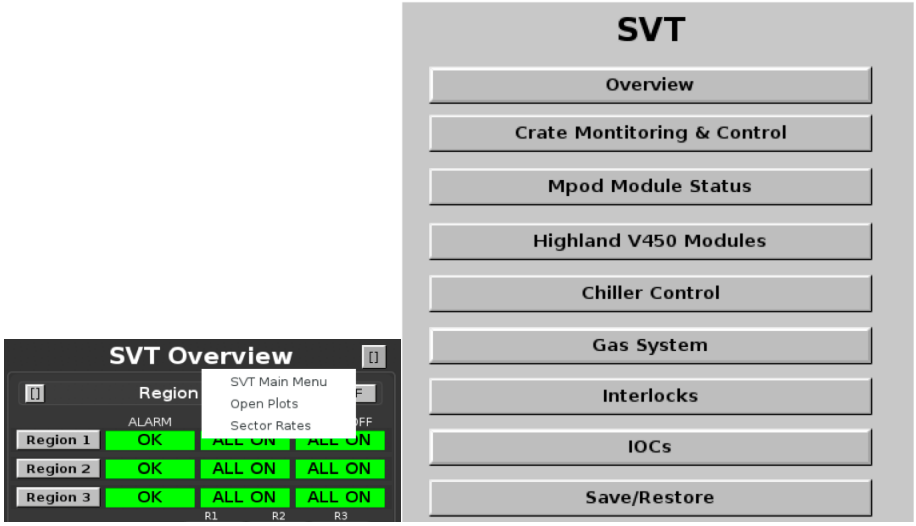


Figure 8 SVT Slow Controls main menu

By selecting one of the menu buttons a corresponding GUI will be opened.

By pressing the button in the top right corner, the submenu can be accessed to select "SVT Main Menu", open plots or display sector rates (Figure 8).

SVT overview screen shows color coded region power supply status (which can be green (ALL ON), red (ALL OFF), or yellow (MIXED), and the interlock status indicators. There are also buttons to bring up various menus: SVT power on/off menu (Figure 9), hardware and software interlock menus, chiller menu, gas purging menu, and IOC menu. At the bottom there are monitoring indicators for cooling system and IOC heartbeat indicators.

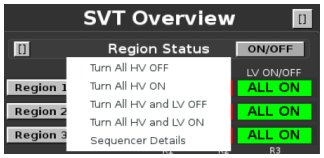


Figure 9 SVT ON/OFF Menu

2.3 *SVT Operation*

The power supply system consists of low voltage and high voltage supplies, and MPOD crates. **All changes of PS settings are done only by the SVT experts.** The low voltage supply powers the analog and digital portions of the readout chips. The high voltage supply provides up to 500 V for biasing the sensors and monitors the leakage current over a wide range. Full depletion voltage of the sensors is from 65 to 80 V. Normal operating range of reverse bias for the SVT sensor is 60 - 85 V. Some sensors could be at lower bias due to the limitations on the leakage current.

2.3.1 General procedures for SVT module services

Here are the general procedures to turn ON and OFF module services.

Turning the SVT system ON:

- Check the dry air flow on the SVT Overview screen, the flow should be within **70-100 lpm**.

- Check interlock status. All color-coded software interlock status indicators should be green. HV/LV inhibit indicator should be off (grey color).
- Check IOC communication status. IOC heartbeat lights should be blinking (green color).
- Check the status of the chiller. The chiller should be "ON". **SVT hardware and software interlocks will prevent powering up the SVT if the chiller is not running.**
- Open "plots" (see Figure 8) for monitoring hybrid temperatures, currents and voltages.
- **Turn ON SVT HV by choosing "Turn All HV ON"** (Figure 9). Confirm your request in the popup window. Check the color-coded region PS status. If after powering up the status is "mixed", repeat this step. If hardware interlock status becomes red, press "hard interlocks" button and press "clear all inhibits".
- Monitor sensor leakage currents. Leakage currents should be below 600 nA. During ramp up the current could raise to several microamps.
- Under "Strip Tool Live" load the config file "pics/tools/StripCharts/SVT/svt-leakage-region.stp", Figure 28. Watch for current stability and post the plot in the HBSVT elog once per shift.

Turning the SVT HV OFF:

Turn OFF SVT HV by choosing "Turn All HV OFF" (Figure 9). Check the color-coded region PS status. HV for all regions should be in OFF state. If after powering up the status is "mixed", repeat this step. Call the SVT expert if unable to turn off the SVT HV.

2.3.2 Gas Purging System

The SVT dry air purging system is designed to provide dry environment inside the detector to avoid condensation. Cold dry air purging through the SVT serves for cooling the silicon sensors. Gas flow through the SVT barrel is controlled and monitored by MFC via CLAS CSS. Oil filter is installed on this line. MFC is bypassed by the rotameter preset to 40 lpm when there is no flow through the MFC.

2.3.3 Alarm Handler

The BEAST alarm handler system running in the Counting House monitors the SVT Slow Controls system. One of the main responsibilities of the shift worker is to respond to alarms from this system, either by taking corrective action or contacting the appropriate on-call personnel. Any time the parameter included in the interlock goes outside predefined safe limits, SVT power is ramped down and the chiller is put in stand-by mode to prevent unsafe operation.

The SVT should be powered on only after ensuring that whatever condition caused the trip has been addressed, cooling system is operational, ambient humidity and dew point readings are within limits. The readings are color coded, black background is normal, orange – warning, red – out of the operational limits.

2.3.4 Cooling System

The front-end chips of the SVT modules have to be cooled to ensure normal operating conditions. The cooling system of the SVT consists of the portable chiller, plastic cooling tubes, coolant pressure, and temperature, meters, and the cold plate with copper tubes inside circulating liquid coolant. The SVT modules have integrated copper heat sinks thermally connected to the cold plate via copper plates with thermal grease. Performance of the cooling system is constantly monitored by EPICS IOC, logged to MYA database and interlocked by the alarm handler. The chiller (Julabo FP51-SL) ensures coolant flow through the cold plate. During nominal operation coolant pressure is about 7 psi. Coolant pressure also depends on the chiller pump stage set by the SVT experts. From the SVT Overview screen chiller control can be accessed by pressing the "Chiller" button (Figure 10) and selecting Julabo chiller.

Figure 10 Chiller Menu

The SVT chiller is controlled from the "Chiller Control" GUI (Figure 11). The chiller menu has control buttons to start and stop the chiller, set the pump stage, cooling temperatures, temperature limits, and alarm settings for the monitored temperature. The shifter is allowed to turn the chiller ON after the trip. **All changes are made only by the experts.** On the right side of the chiller screen there are color-coded status indicators for parameters of the cooling system.

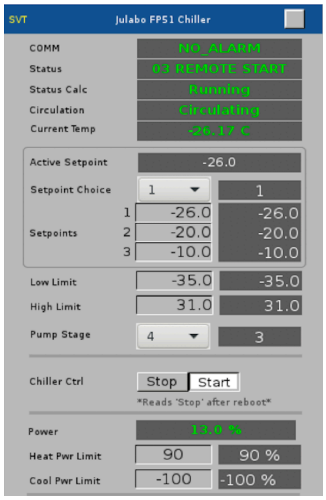


Figure 11 Julabo chiller GUI

If the chiller is stopped, in order to start it, software and hardware interlocks "inlet flow", "outlet flow", "inlet temperature", and "inlet pressure" should be disabled (otherwise the interlocks will stop the chiller). Hardware interlock latches should be reset. **After the chiller is started, all interlocks must be re-enabled.**

There are two temperature settings for the chiller corresponding to SVT ON and OFF (when both LV and HV are ramped down) state. Temperature settings are switched automatically depending on the state of LV power supplies. In normal operation auto temperature setting should be enabled. The values are defined by the SVT experts (Figure 12).

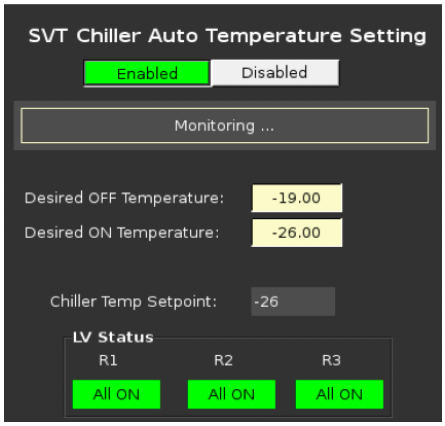


Figure 12 Chiller Auto Temperature Setting

2.3.5 SVT Module Control GUI

The control and monitoring of the power for the SVT modules (sectors) is done via "MPOD Module Status" menu (under the SVT main menu), which has submenus for each SVT region. An example of such GUI is presented in Figure 13.

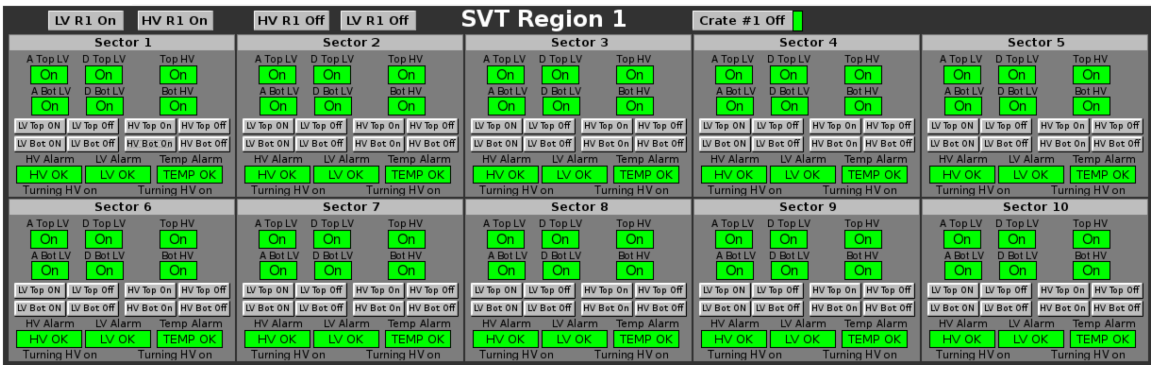


Figure 13 SVT module control and status GUI

There are control buttons to turn on and off the LV and HV power for the whole region, and to power off the MPOD crate. The shifter should not power off the MPOD crates unless instructed by the SVT expert. **The LV is turned on first and turned off last.** The power sequencer will not allow to bias the sensors (HV) without powering the front-end chips (LV). The correct sequence is ensured by the alarm handler logic. The GUI is divided into the sector menus. Each sector menu has the color-coded status indicators (green – on, red – off), control buttons and log indicator. There are indicators and buttons for sector HV/LV, and temperature alarm status, analog and digital LV, and HV for each side of the module (top, bottom). The control buttons used to manage the power of the individual components. The command status string at the bottom of the sector menu shows the last action for each

side of the module (i.e. “Turning HV on”). Another (compact) version of the same GUI is available, Figure 14.

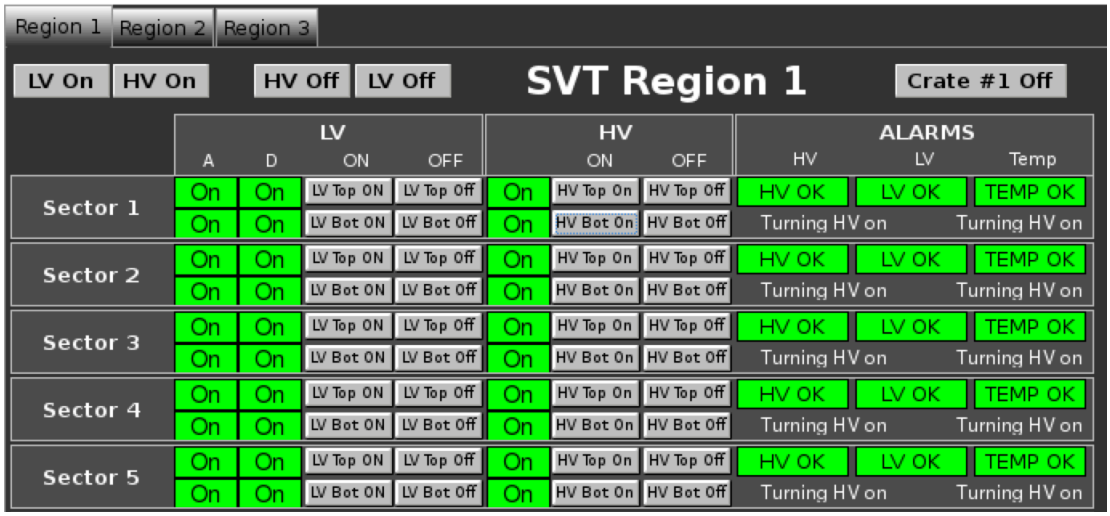


Figure 14 Compact version of module control and status GUI

In normal operation SVT power is controlled by the global ON/OFF sequencers (“ON/OFF” button on the “SVT Overview” screen. Using “ALL ON” and “ALL OFF” buttons will ensure the proper power ramping command sequence is executed, Figure 15. If some modules will not change their state (ON/OFF), they can be controlled from the module control GUI (Figure 13). Remember, the LV is turned ON before the HV, turned OFF after the HV (the GUI should prevent incorrect sequence).

Figure 15 SVT Power Control GUI

Monitoring of HV bias voltages and sensor leakage currents is done via “MPOD Module Status” button and “HV Leakage Currents, List View” menu (Figure 16). **Alarm settings can be modified only by the SVT experts (“A” buttons).**

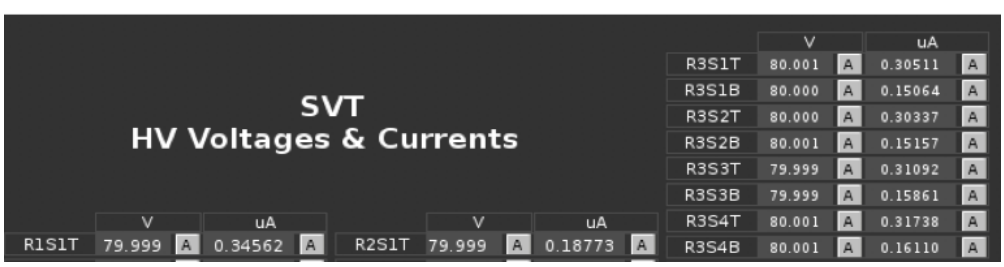
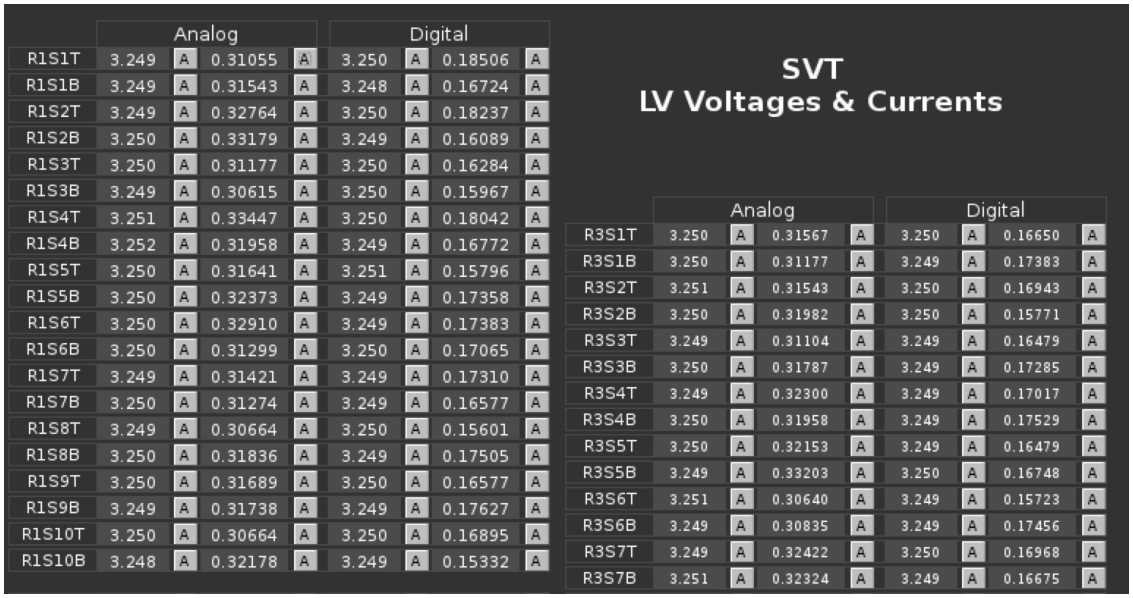


Figure 16 HV Monitoring (sensor bias voltage and leakage currents in microamps)

"LV Voltages and Currents, List View" menu opens a window with analog and digital LV readings, Figure 17. **Alarm settings can be modified only by the SVT experts ("A" buttons).**

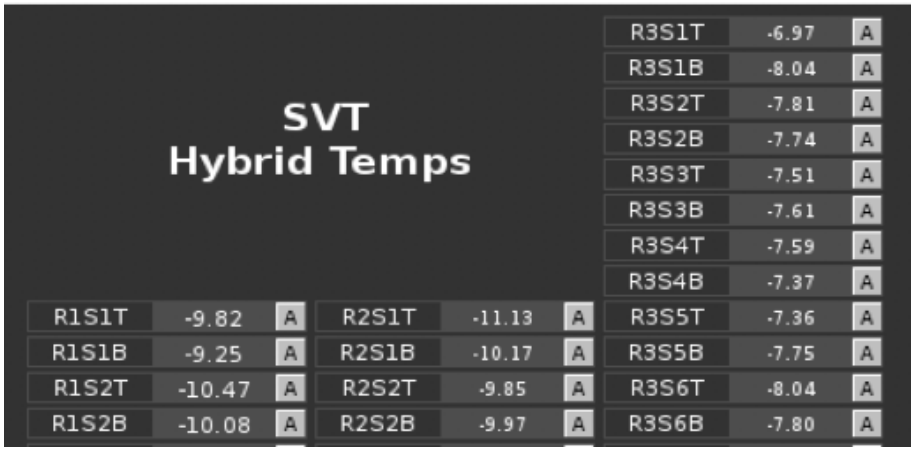


	Analog				Digital			
R1S1T	3.249	A	0.31055	A	3.250	A	0.18506	A
R1S1B	3.249	A	0.31543	A	3.248	A	0.16724	A
R1S2T	3.249	A	0.32764	A	3.250	A	0.18237	A
R1S2B	3.250	A	0.33179	A	3.249	A	0.16089	A
R1S3T	3.250	A	0.31177	A	3.250	A	0.16284	A
R1S3B	3.249	A	0.30615	A	3.250	A	0.15967	A
R1S4T	3.251	A	0.33447	A	3.250	A	0.18042	A
R1S4B	3.252	A	0.31958	A	3.249	A	0.16772	A
R1S5T	3.250	A	0.31641	A	3.251	A	0.15796	A
R1S5B	3.250	A	0.32373	A	3.249	A	0.17358	A
R1S6T	3.250	A	0.32910	A	3.249	A	0.17383	A
R1S6B	3.250	A	0.31299	A	3.250	A	0.17065	A
R1S7T	3.249	A	0.31421	A	3.249	A	0.17310	A
R1S7B	3.250	A	0.31274	A	3.249	A	0.16577	A
R1S8T	3.249	A	0.30664	A	3.250	A	0.15601	A
R1S8B	3.250	A	0.31836	A	3.249	A	0.17505	A
R1S9T	3.250	A	0.31689	A	3.250	A	0.16577	A
R1S9B	3.249	A	0.31738	A	3.249	A	0.17627	A
R1S10T	3.250	A	0.30664	A	3.250	A	0.16895	A
R1S10B	3.248	A	0.32178	A	3.249	A	0.15332	A

	Analog				Digital			
R3S1T	3.250	A	0.31567	A	3.250	A	0.16650	A
R3S1B	3.250	A	0.31177	A	3.249	A	0.17383	A
R3S2T	3.251	A	0.31543	A	3.250	A	0.16943	A
R3S2B	3.250	A	0.31982	A	3.250	A	0.15771	A
R3S3T	3.249	A	0.31104	A	3.249	A	0.16479	A
R3S3B	3.250	A	0.31787	A	3.249	A	0.17285	A
R3S4T	3.249	A	0.32300	A	3.249	A	0.17017	A
R3S4B	3.250	A	0.31958	A	3.249	A	0.17529	A
R3S5T	3.250	A	0.32153	A	3.249	A	0.16479	A
R3S5B	3.249	A	0.33203	A	3.250	A	0.16748	A
R3S6T	3.251	A	0.30640	A	3.249	A	0.15723	A
R3S6B	3.249	A	0.30835	A	3.249	A	0.17456	A
R3S7T	3.249	A	0.32422	A	3.250	A	0.16968	A
R3S7B	3.251	A	0.32324	A	3.249	A	0.16675	A

Figure 17 LV PS readings

Hybrid temperatures can be monitored with the button "Highland V450 Modules" and the menu "List View (Detector), Figure 18. Beware that these readings are valid only when LV is ON (temperature sensors are powered up from the same PS modules as frontend chips). **Alarm settings can be modified only by the SVT experts ("A" buttons).**



						R3S1T	-6.97	A
						R3S1B	-8.04	A
						R3S2T	-7.81	A
						R3S2B	-7.74	A
						R3S3T	-7.51	A
						R3S3B	-7.61	A
						R3S4T	-7.59	A
						R3S4B	-7.37	A
R1S1T	-9.82	A	R2S1T	-11.13	A	R3S5T	-7.36	A
R1S1B	-9.25	A	R2S1B	-10.17	A	R3S5B	-7.75	A
R1S2T	-10.47	A	R2S2T	-9.85	A	R3S6T	-8.04	A
R1S2B	-10.08	A	R2S2B	-9.97	A	R3S6B	-7.80	A

Figure 18 Monitoring Hybrid Temperatures

Plots of LV and HV voltages and currents are accessible from the SVT Overview screen or from the main menu button "MPOD Module Status" (Figure 8) with "HV Leakage Currents, Plot View" menu, Figure 19.

Figure 19 Monitoring Plots for HV and LV PS

2.3.6 SVT Alarm Handler and Interlocks

The SVT alarm handler monitors the slow control parameters and prevents unsafe conditions of the detector. All SVT module power supplies have hardware and software current and voltage limits set by the experts. Interlocks provide detector protection for ambient conditions, power supplies, cooling system, and gas purging system.

The alarm handler GUI is part of the CLAS Alarm Tree and has a hierarchical tree, which displays the color-coded status of the SVT slow control interlock system (Figure 20). Please refer to general description of the CLAS slow control software for details on using the Alarm Handler GUI.

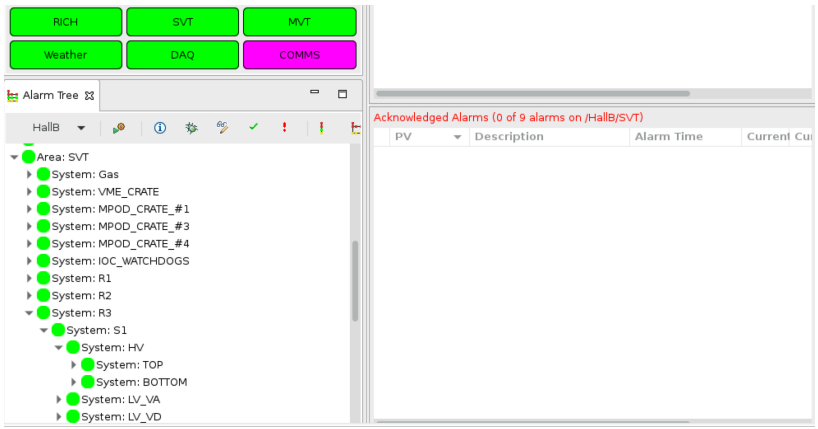


Figure 20 Alarm handler user interface

Green color represents the normal operating state. Yellow represents a warning and red – an error. The magenta color means lost connection. To acknowledge and clear the error or the warning a corresponding button has to be pressed. The top level (SVT) provides the status of the entire detector. There are expandable views for each region, sector, their LV/HV power supplies, voltages and currents. There are separate views for each MPOD PS and for the slow controls VME crate, EPICS IOC watchdogs, ambient and cooling system interlocks. The control and monitoring of the SVT software interlocks is done with the interface by pressing the "soft interlocks" button on the SVT Overview screen, see

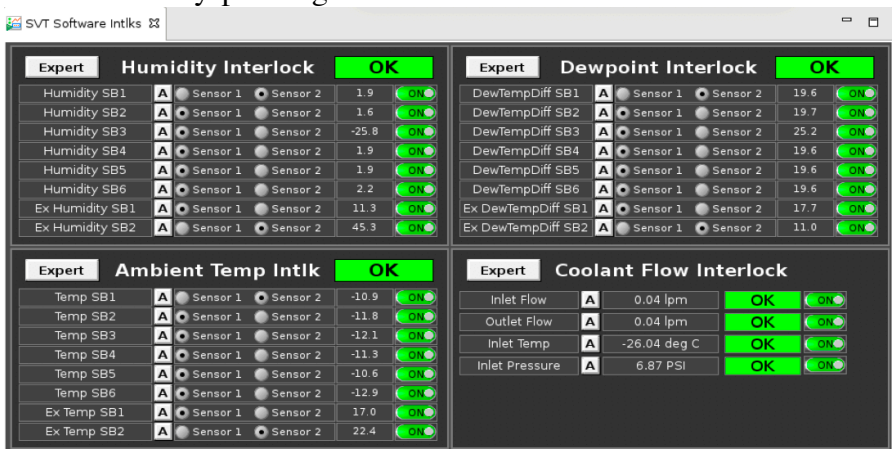


Figure 21. The flow, temperature, and pressure of the coolant are managed via "Coolant Flow Interlock" section. The indicators are color-coded (green – good, yellow – warning, red – off limits). The interlock settings are modified by pressing the corresponding "A" button (experts only). There are color-coded status indicators for the chiller and digital monitoring displays. On the right side of the digital displays there are buttons which control whether the parameter is used in the interlock. **In normal operation all interlocks should be enabled unless specific instructions are provided by the SVT experts.**

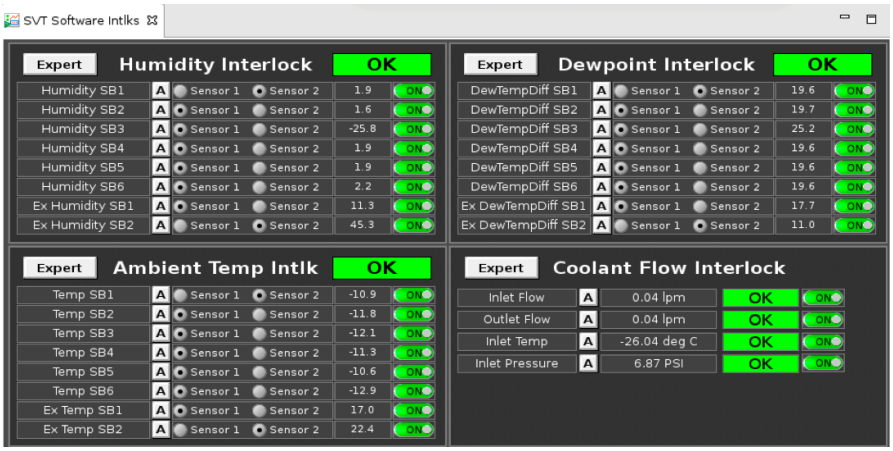


Figure 21 Software Interlocks GUI

Ambient temperature interlock section provides means to monitor the reading from the ambient temperature sensors. There are 2 duplicated (sensor1 and sensor2) sensors in each board and 3 boards in regions 2 (SB1-SB3) and 3 (SB4-SB6). Region 1 has no ambient sensors installed. The sensor boards are glued to the cold plate. Two boards (External SB1, SB2) are located outside of the barrel and are monitoring the external ambient temperature.

Similar interfaces exist for ambient humidity and the dew point interlocks. The dew point interlock displays the difference between the environment temperature and the corresponding dew point. The indicators are color-coded (green – good, yellow – warning, red – off limits). The interlock parameters are set by the "A" buttons (experts only).

2.3.7 Resetting the IOCs

If there is a communication problem present, which typically appears for all sectors in a given region, the usual cause is an issue of communication between the IOC computer and the HV mainframe. The software IOC status window is accessible from the SVT Overview GUI with the "IOCs" button. To reboot the IOC for a given region, click on the "Reboot" button for the specific IOC, Figure 22.

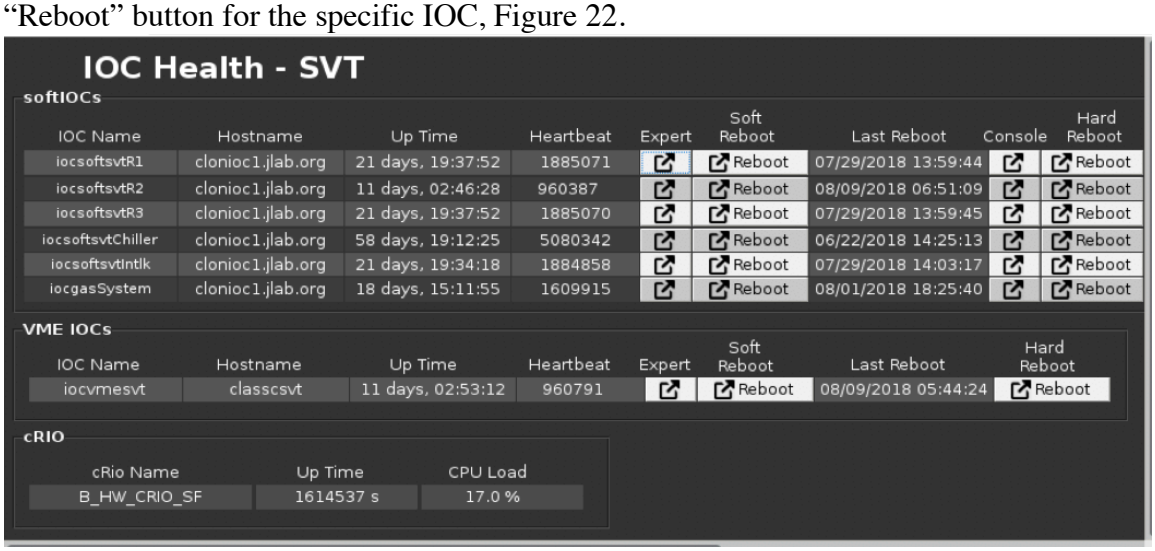


Figure 22 IOC Health GUI

If the hardware interlock inhibit indicator on the SVT Overview window is red, past hardware interlock errors can be cleared from the "Hard Interlocks" button which brings the corresponding PS inhibits window, Figure 23. "Clear All Inhibits" will clear MPOD crate inhibits if the error state resulted in raising the hardware interlock is no longer present.

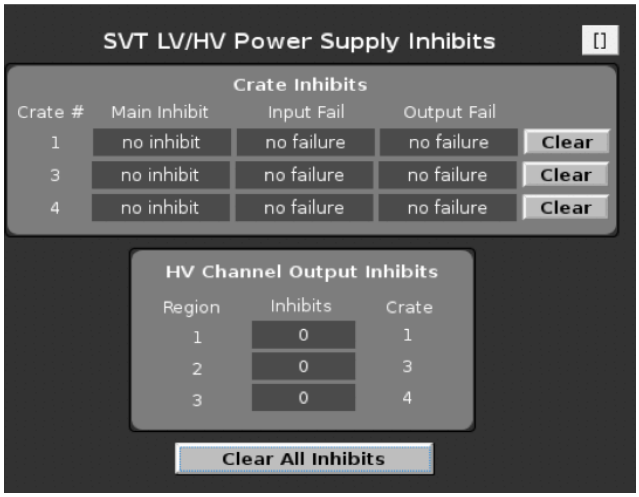


Figure 23 MPOD Crate Inhibit Status GUI

2.3.8 SVT Hardware Interlock System

The Hall B SVT Hardware Interlock System is a backup system designed to protect the detector from damage in the event the main control system fails or if network communication is lost. This is a standalone system and is completely independent from the main EPICS-based slow control system and does not rely on network communications to safeguard the SVT detector. Hardware interlock system provides redundant safety for critical parameters in case of alarm handler failure. **Only the SVT experts are allowed to make changes to the interlock configuration parameters.** All changes are reported in the logbook.

2.3.8.1 Hardware & Software Description

The Hardware Interlock System is based on the National Instruments CompactRIO (cRIO) Programmable Automation Controller (PAC) platform. cRIO is a reconfigurable embedded control and acquisition system. The cRIO system's hardware architecture includes I/O modules, a reconfigurable field-programmable gate array (FPGA) chassis, and an embedded controller. The cRIO integrated dual-core controller runs on a LabVIEW Real Time Linux operating system.

2.3.8.2 Summary of Hazards Monitored

The Hardware Interlock System monitors key detector parameters and takes corrective action if a monitored signal is outside of pre-programmed limits. The signals monitored include:

- HFCB Temperature
- Detector Internal Temperature & Humidity
- Detector Internal Dew Point
- Ambient Temperature & Humidity
- Ambient Dew Point
- Coolant Flow

- Coolant Pressure
- Coolant Temperature
- Coolant Leak Detection

2.3.8.3 System Block Diagram

Figure 24 shows the block diagram of the Hardware Interlock System and the interfaces to the SVT system. The cRIO chassis obtains all of the monitored signals via connections to the SVT. patch panel.

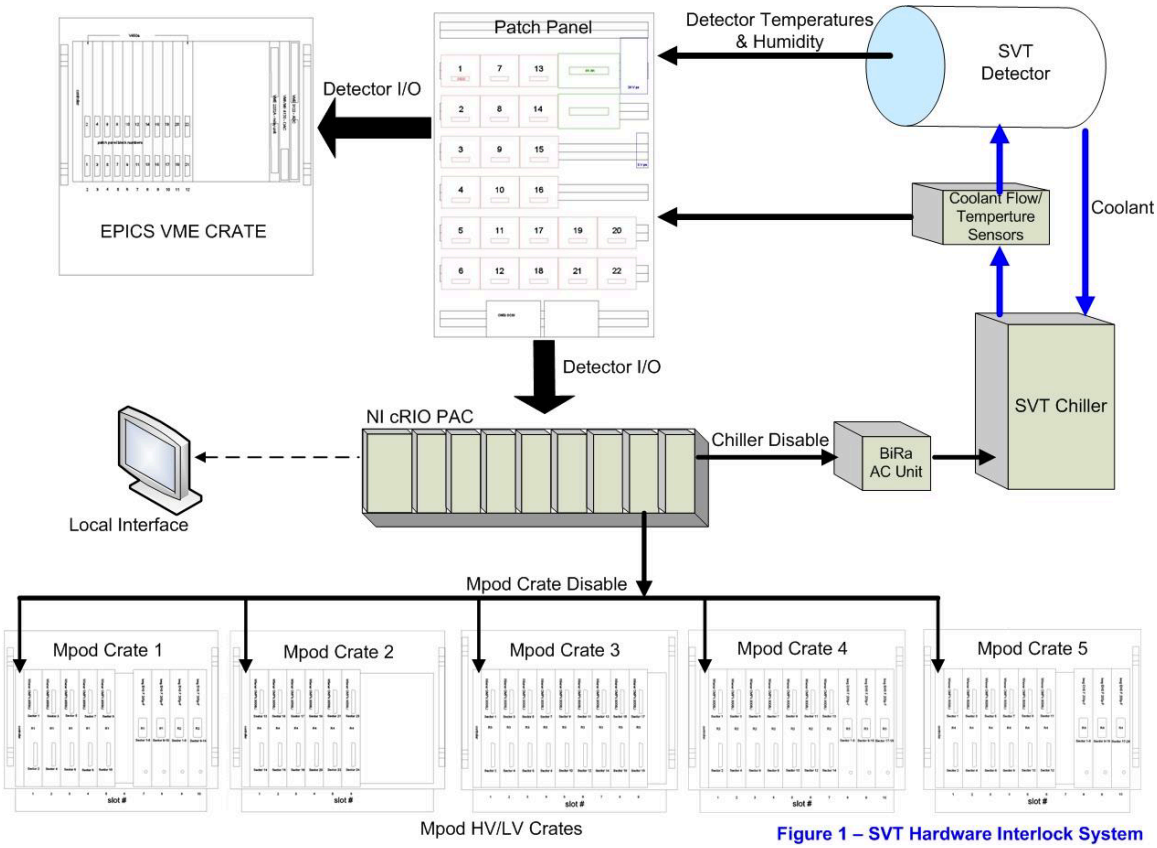


Figure 24 Block diagram of the SVT hardware interlock system

2.3.8.4 Mpod Crate Control

Under fault conditions, the Hardware Interlock System will disable the Mpod HV/LV crates via the front panel connector on the Mpod controller. When disabled by the Hardware Interlock System, the EPICS controls are overridden and all channels of the Mpod crate will ramp down at their pre-programmed rate. A reset of both the Hardware Interlock System and the EPICS Mpod control is needed in order to re-power the HV and LV channels.

2.3.8.5 Chiller Disable

Under fault conditions, the Hardware Interlock System will disable the SVT chiller. A BiRa Systems Model 8880-1B1Y AC Power Module is to disable the chiller. The AC power to the chiller is plugged into the AC Power Module. A signal from the monitoring

PAC will shut off the power to the chiller via the AC Power Module in the case of a fault.

2.3.8.6 Hardware Interlock System Trip Levels

The Hardware Interlock System is the last line of protection for the detector. If the main EPICS slow controls system works correctly, the Hardware Interlock System shall never need to take corrective action to protect the detector.
The trip levels for the Hardware Interlock System is slightly out of bounds from the EPICS trip levels to prevent both systems from tripping at the exact same level. The EPICS slow controls system (if working correctly) shall always trip first before the Hardware Interlock System.

2.3.8.7 User Interface

The user interface to the Hardware Interlock System allows the operator to remotely monitor the SVT and to set interlock trip levels. The user interface is also used to reset the system after an interlock trip event. The National Instruments cRio system monitoring the SVT works does not require the user interface program to be running in order to protect the detector. The user interface is accessed through the button in the top right corner of the "Crate Inhibit Status" screen launched with "Hard Interlocks" button on the SVT Overview screen (Figure 23). On the first tab (Summary of Interlocks) the current state of the SVT interlocks is shown (Figure 25). Figure 26 shows the main front panel of the user interface. The latched errors can be cleared by pressing the green "OFF" button 2 times. Interlock color coded status panel is on the left side of the GUI. The middle panel is for signal monitoring. On the right side the status of latched errors is displayed. All color-coded indicators should be green in order to enable powering on the SVT. The chiller has to be operating in order to clear the coolant flow errors.

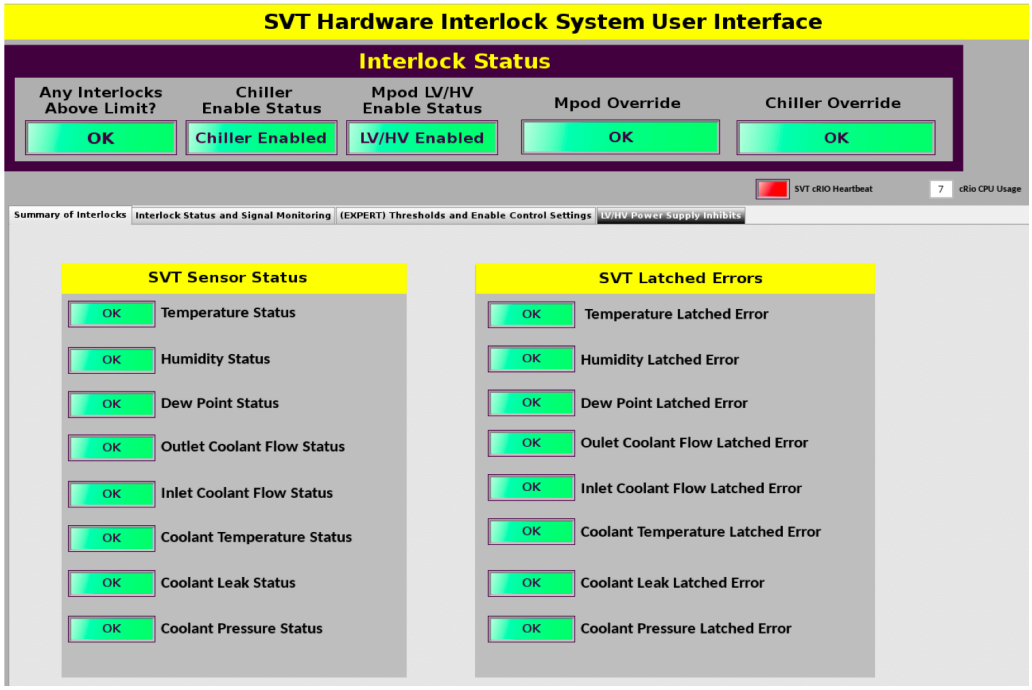


Figure 25 Hardware Interlock Status

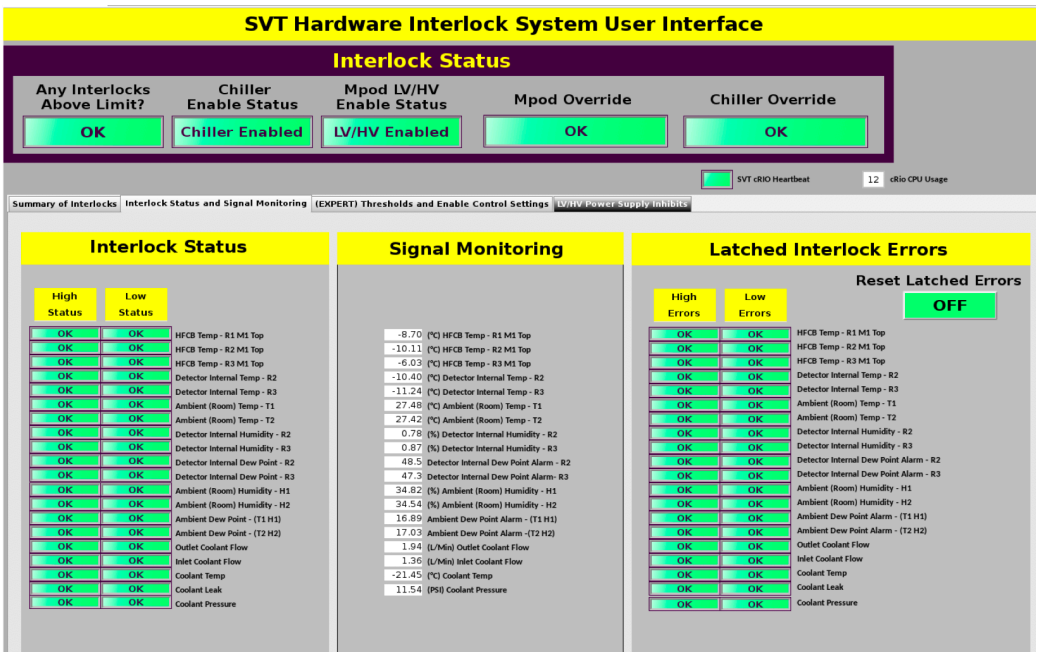


Figure 26 User Interface Main Front Panel

Figure 27 shows the interlock and enable setting screen. When SVT LV power is off, the HFCB temperature readings are not valid because these temperature sensors are powered from the LV PS. In order to prepare for powering the LV PS, HFCB hardware temperature interlock has to be disabled by pressing All HFCB Temps "Enabled". The color of the button changes to red. After powering up LV of all SVT regions this interlock must be enabled again except HFCB temp R3 M1 Top which has temperature sensor intermittent connectivity issues and is permanently disabled.

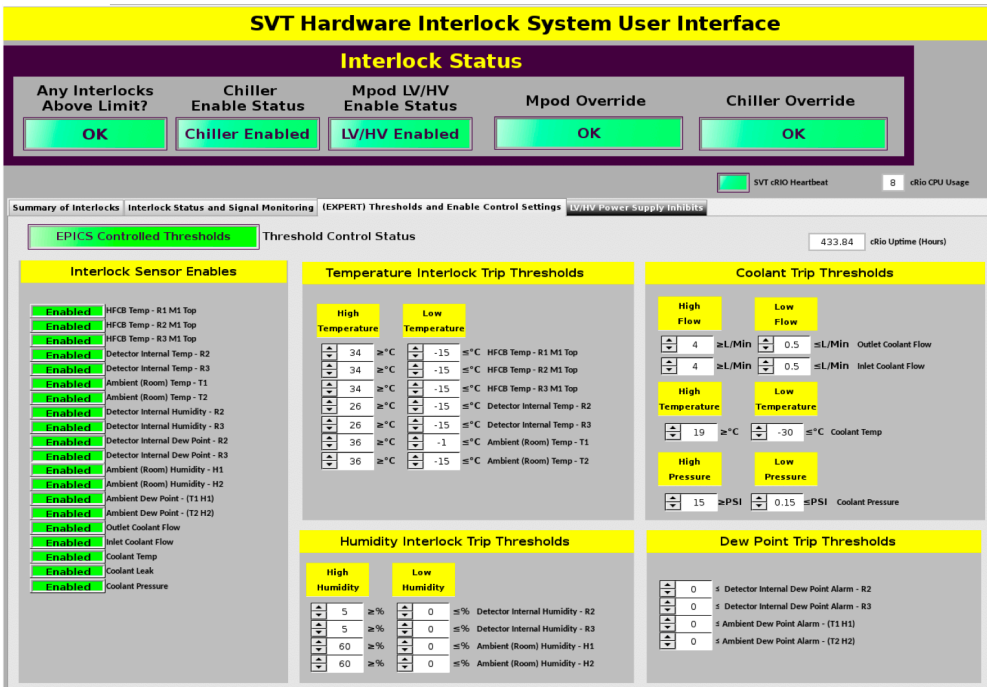


Figure 27 Interlock and Enable Setting Screen

2.4 *Detector Monitoring*

In order to maintain proper performance of the SVT, all critical characteristics of the system are tracked. This monitoring operation can be described by three types of operations:

1. Monitoring of all parametric characteristics of the SVT, such as voltages, currents and temperatures

2. Periodic calibration of the detectors and readout electronics (experts only)

3. Monitoring of the quality of data being collected by SVT

2.4.1 Monitoring of SVT Operating Parameters

The SVT slow controls system monitors the following parameters:

- the low voltages and currents
- the high voltages and currents
- the temperature of the modules (hybrid, ambient)
- the humidity inside and outside the SVT
- the status of the cooling system
- the status of the gas purging system

The temperature of the hybrids is monitored with "Highland V450 Modules" menu. It displays one reading for each side of the module. The indicators are color coded (green – good, yellow – warning, red – off limits). The interlock parameters are set by the "A" buttons (experts only).

All monitoring EPICS channels are saved to MYA database. The access to the database can be done via the "Strip Charts" button on the main CLAS12 CSS menu.

Under "Strip Tool Live" load the config file "pics/tools/StripCharts/SVT/svt-leakage-region.stp", Figure 28. Watch for current stability and post the plot in the HBSVT elog once per shift.

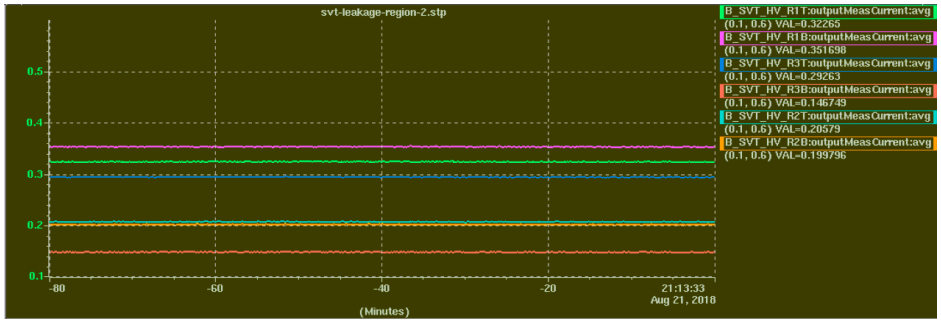


Figure 28 SVT sensor leakage currents (per layer, top and bottom side of the region).

2.4.2 Data Quality Monitoring (DQM)

SVT monitoring is done with clas12mon interface. SVT/BST monitoring plots are posted to HBLOG for every run as part of the CLAS12 monitoring procedure. For reference, here are the monitoring plots from RGA run.

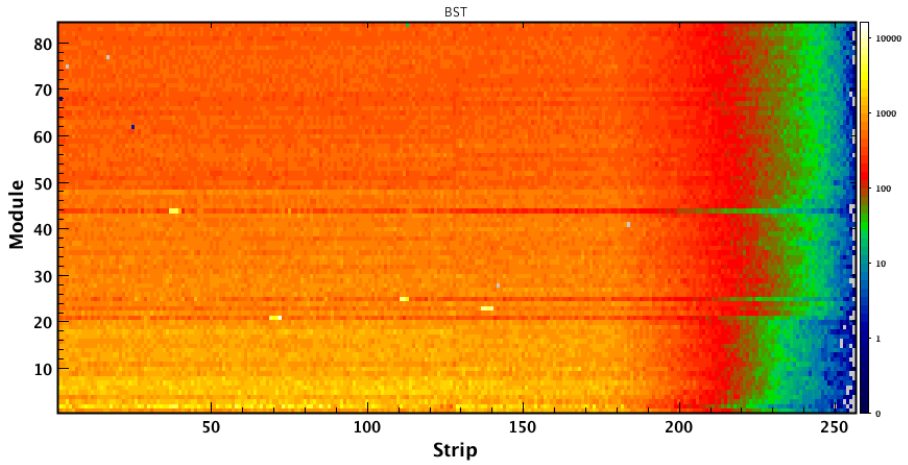


Figure 29 Monitoring plot for BST occupancy map

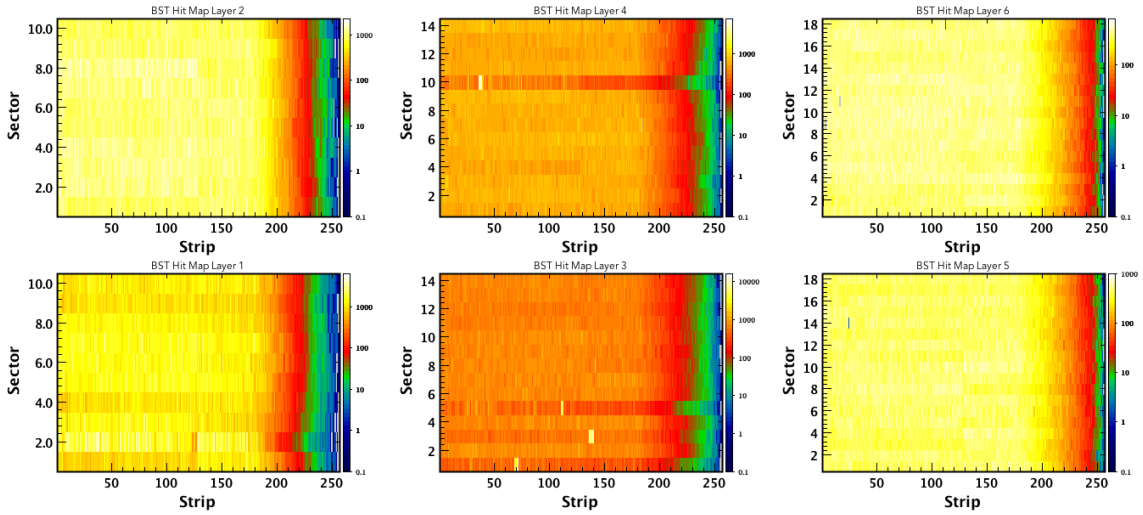


Figure 30 Monitoring plots for BST layer occupancy maps

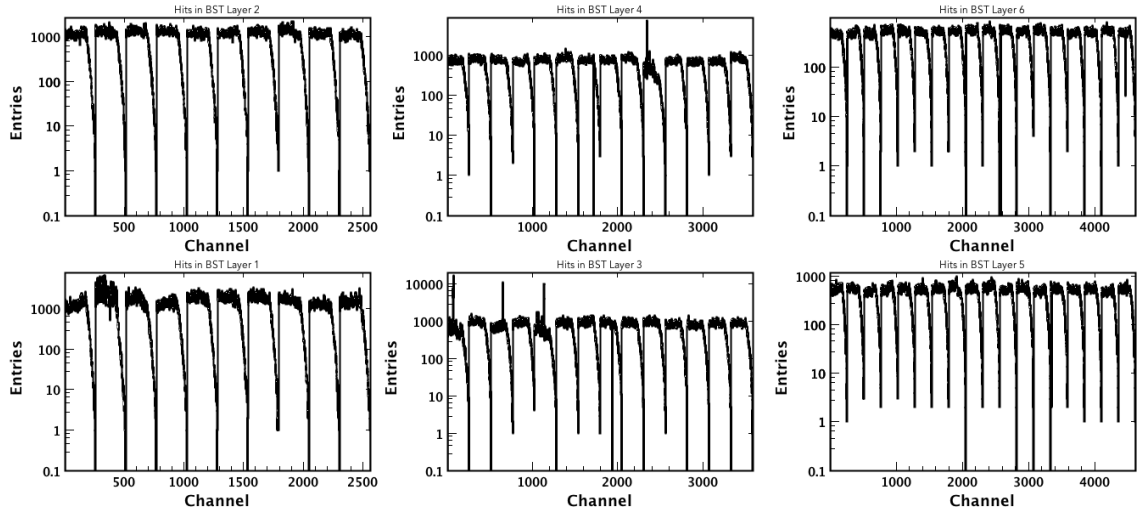


Figure 31 Monitoring plots for 1D BST layer occupancies

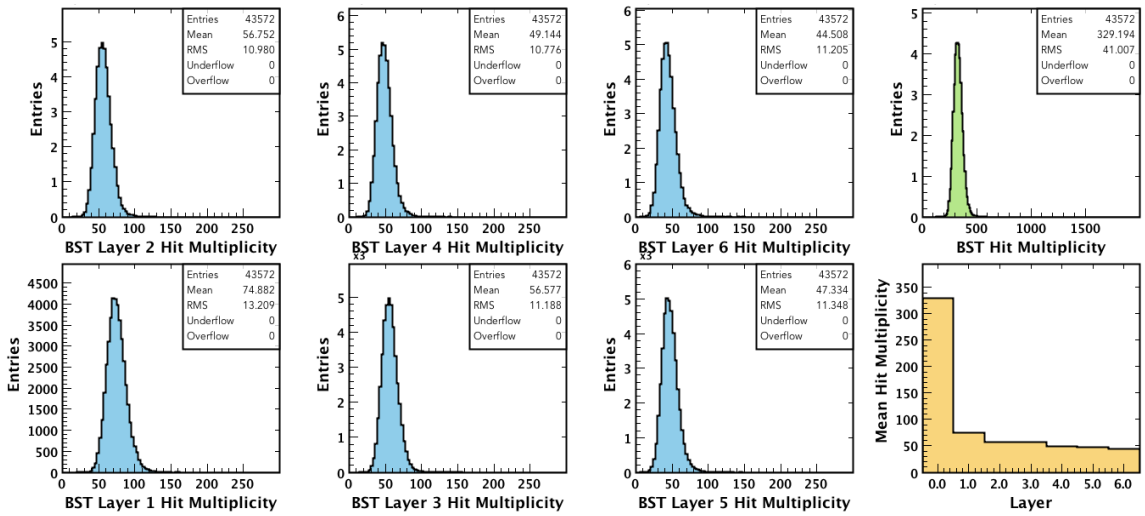


Figure 32 Monitoring plots for BST hit multiplicity

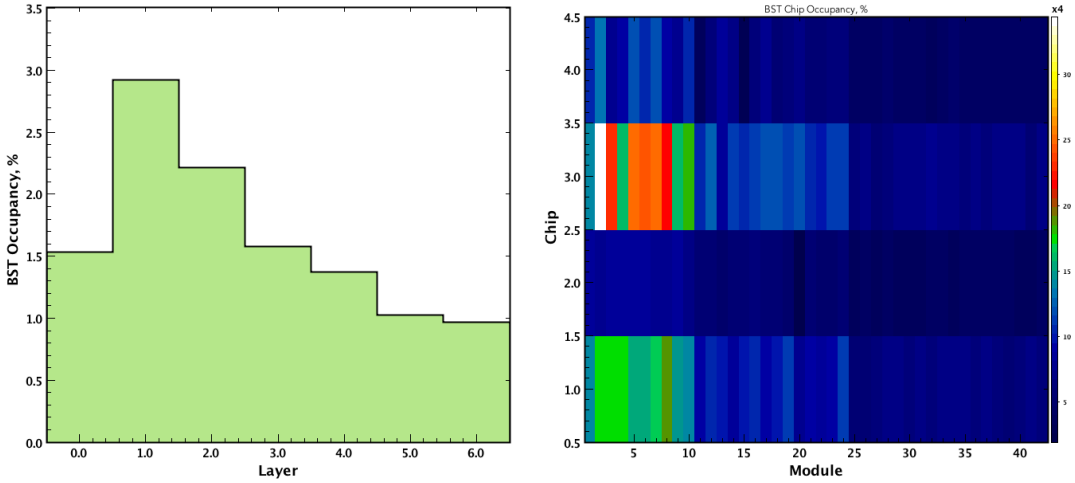


Figure 33 Monitoring plots for BST hit occupancy

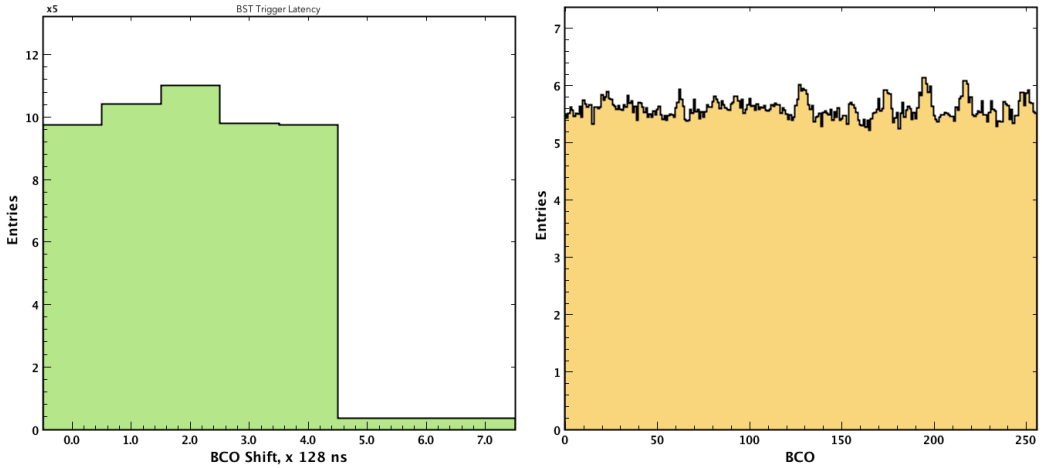


Figure 34 Monitoring plots for BST Latency and BCO (Bunch Cross Oscillator)

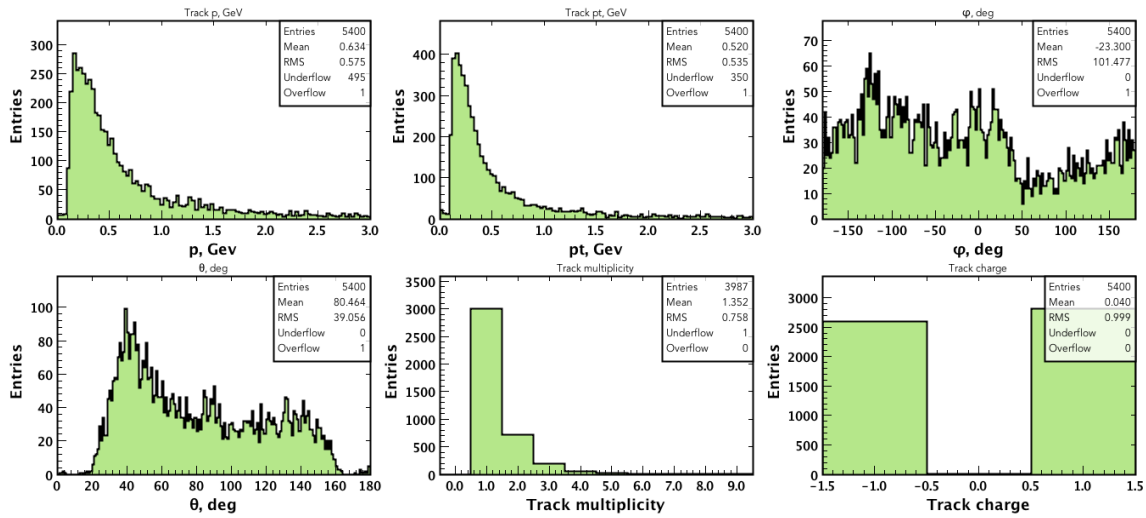


Figure 35 Monitoring plots for BST track reconstruction

3 Information for Subsystem Experts

3.1 *Detector layout*

The readout strips have a constant φ pitch of 1/85°. Such a layout reduces the dead area along the edge of the sensors, particularly important, because the modules, to reduce the radiation length seen by a particle's trajectory, do not overlap. As a consequence of the constant φ pitch, the layout of the strips is such that the strips pitch P (z, n, n +1) between the n-th and the (n +1)-th strip is a function of the z location and of the strip numbers n and n +1. The readout pitch of a module ranges from 156 μm at the Hybrid sensor end to 202 μm at the Far sensor end of the module. Because of the change in the pitch, the spatial resolution ranges from 45 μm at the Hybrid sensor end to 58 μm at the Far sensor end of the module. The r-z position of tracks is determined by the stereo angle, which is 3° at the Hybrid sensor end and ~2° at the Far sensor end (Figure 36).

The readout strips have graded angles—readout strip #1 is parallel to the longitudinal axis of the module, the z axis; the last readout strip, #256, has an angle of 3° with respect to the longitudinal axis of the module. The angle between any two consecutive readout strips increases by 1/85th of a degree, a constant φ pitch—this approach minimizes dead areas on the sensor. Due to the constant φ pitch, the lengths of the readout strips of the modules vary from 0.5 cm to 33 cm. The intermediate strip pitch is 0.078 mm and the readout pitch is 0.156 mm. The strip-to-pitch ratio is 0.256 for all three types of sensors.

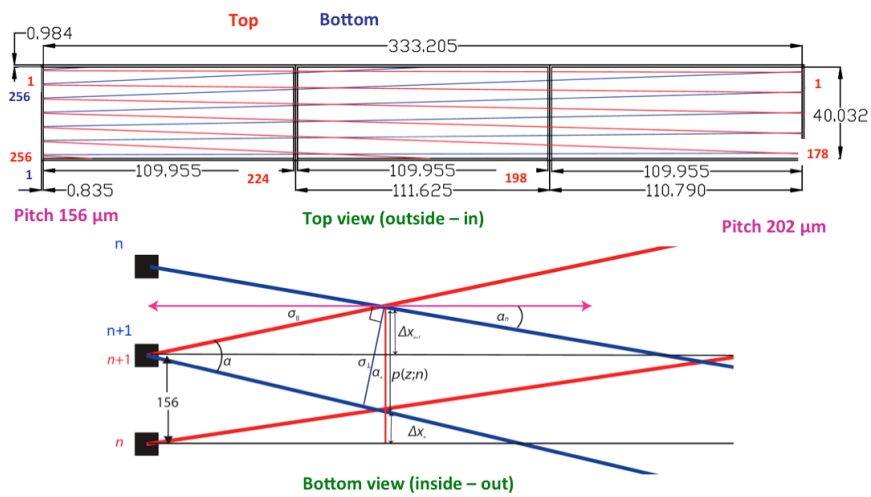


Figure 36 SVT sensor strip layout

3.2 *Module services*

Module services provide power, cooling, and communication to all the SVT modules. The services connected to the SVT include: power supply cables, data and control cables, cooling pipes, and cables for monitoring humidity and temperature. Once all the services are attached, the cooling circuits are tested for blockages, and the modules are powered, their electrical circuits are read out, checked, and repaired as appropriate.

Regular maintenance of SVT services (PS, cables, electronics, gas, cooling etc.) will be performed by JLab trained personnel/expert on-call.

Major detector maintenance will be responsibility of SVT experts and Detector Support Group.

3.2.1 Power Supplies

Figure 37 Wiener MPOD mainframe with HV and LV power supply modules

The ISEG high voltage power supply module residing in the MPOD mainframe (Figure 37) is capable of providing current up to 10 mA per channel with 10 mV steps and ripple less than 5 mV peak to peak. Due to the losses in cables, the actual voltage, which

appears at the module end of the cable, is measured and source adjusted appropriately. Each side of the module receives low voltage, 2.5 V for both analog and digital parts of the FSSR2 chip and high voltage for the sensors. The low voltage also powers analog output CMOS IC temperature sensors, one per side. An independent floating circuit supplies each voltage to each module. This enables control of grounding and shielding; all voltages are grounded to the common spot and shields of the cables are grounded at the power supply.

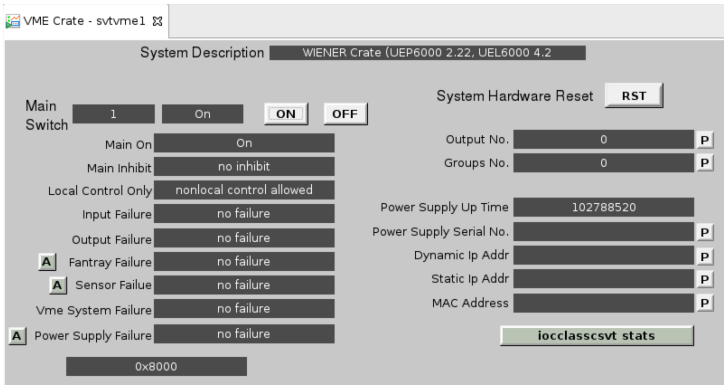


Figure 38 Slow Control VME Crate GUI

"Crate Monitoring and Control" button opens up a sub-menu to select the controls for all crates, individual MPOD or a VME slow control crate (**Error! Reference source not found.**).

MPOD crate GUI (Figure 39**Error! Reference source not found.**) allows controlling and monitoring the status of the crate and it's power supply modules. In case of error it will be displayed on the status indicators and can be cleared by pressing the "Clear" button.

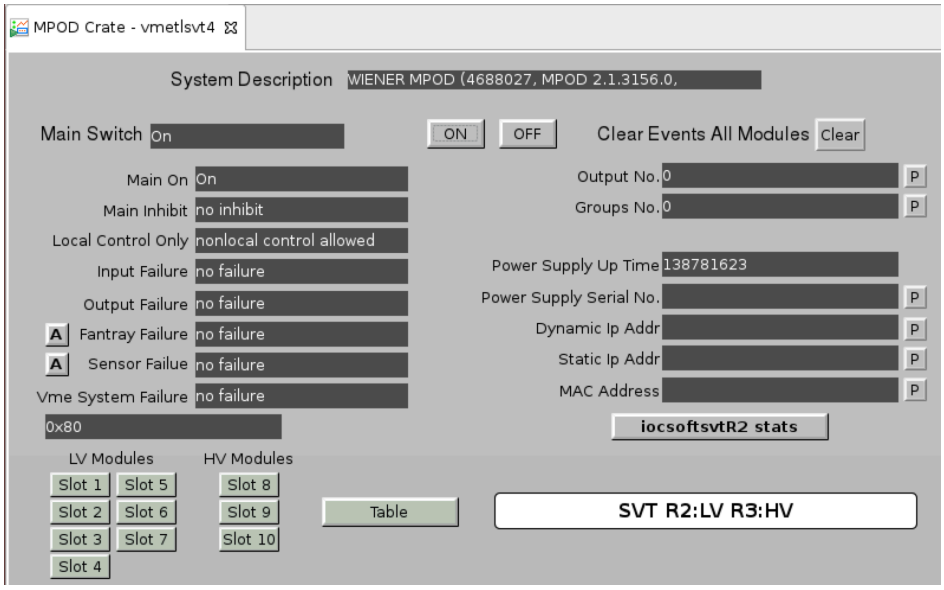


Figure 39 MPOD Crate GUI

Clicking on the "Table" button will bring the detailed HV and LV power supply module GUI (Figure 40) which displays the status of individual channels and allows to change the

settings for voltages, currents, change the state and reset the channel. Channels are labeled according to the logical PS map and hardware connection.

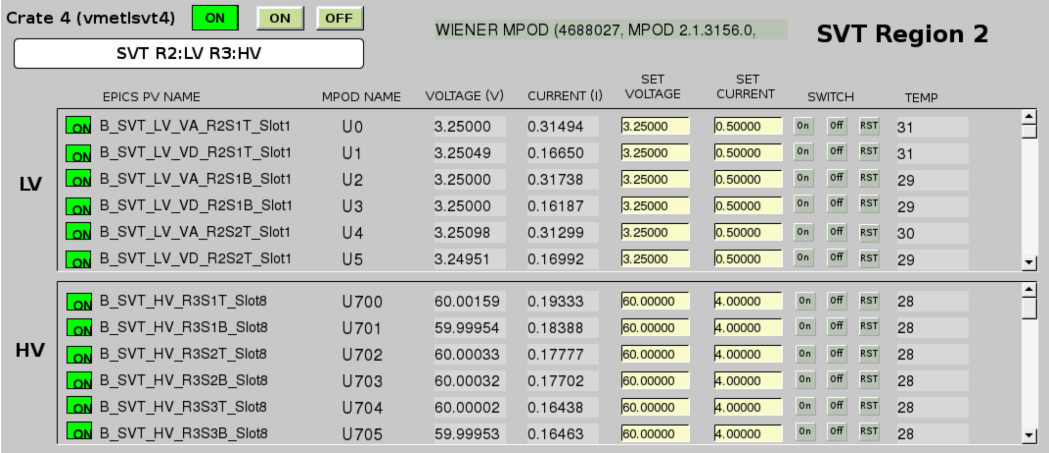


Figure 40 MPOD power supply module GUI

Individual power supply channels can be accessed via the corresponding "Slot" button (Figure 40**Error! Reference source not found.**), which would bring the channel menu (Figure 41, Figure 42). Detailed channel status information, settings and alarm limits are available from this menu.

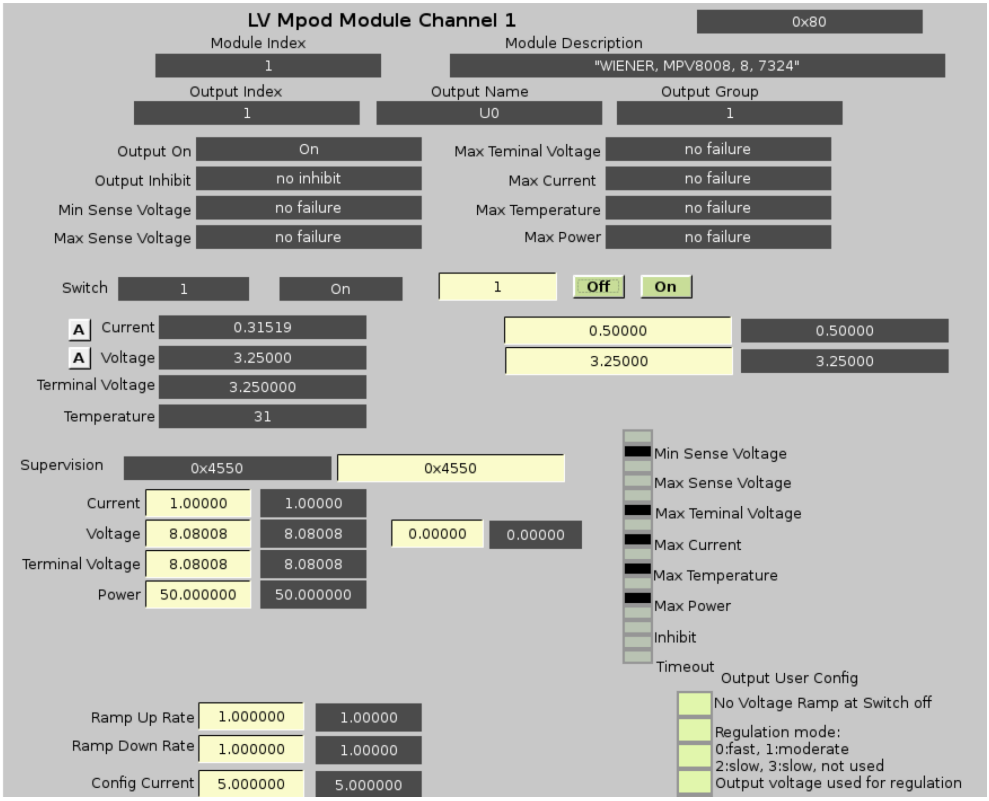


Figure 41 MPOD LV Power Supply Channel GUI

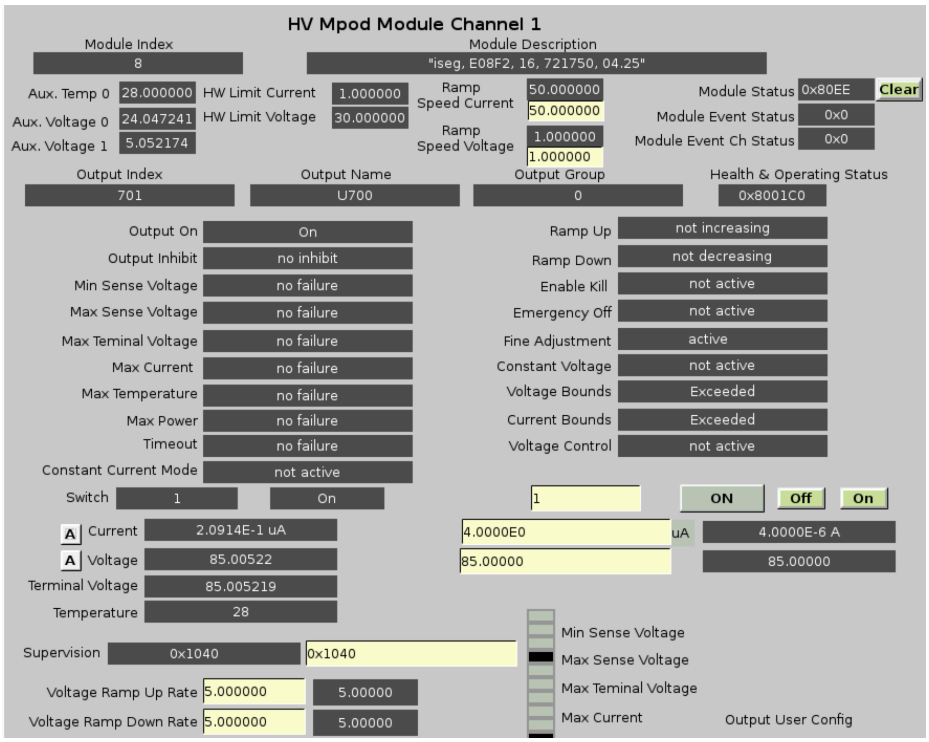


Figure 42 MPOD HV Power Supply Channel GUI

3.2.2 Cables and Connections

Checkout of the cable routing schemes of the signal readout with high and low voltages applied to the detectors and reading out electronic noise and currents on HV and LV lines is carried out with calibration signals injected channel-by-channel into the front-end electronics. This procedure identifies false signal cablings and faulty signal and power connections.

Chosen mapping of SVT data cables in the crates ensures uniform occupancy and data rate. Hardware module mapping for SVT VXS crates is shown in Figure 43. Crate controllers are placed in the slot 1, Signal Distribution (SD) modules – in slot 12, and Trigger Interface (TI) modules – in slot 21. All operations requiring disconnecting the cables must be performed on powered off crates following ESD protection rules.

Region	Sector	Crate	Slot	Channel	Module	Region	Sector	Crate	Slot	Channel	Module	Region	Sector	Crate	Slot	Channel	Module
1	1	1	3	1	28	2	1	1	7	1	82	3	1	1	13	1	18
1	2	1	3	2	79	2	2	1	7	2	83	3	2	1	13	2	12
1	3	1	4	1	44	2	3	1	8	1	85	3	3	1	14	1	31
1	4	1	3	1	48	2	4	1	8	2	86	3	4	1	14	2	34
1	5	1	3	2	26	2	5	2	7	1	65	3	5	1	15	1	39
1	6	2	4	1	74	2	6	2	7	2	25	3	6	2	13	1	49
1	7	2	4	2	67	2	7	2	8	1	29	3	7	2	13	2	57
1	8	2	5	1	70	2	8	2	8	2	37	3	8	2	14	1	36
1	9	2	4	2	71	2	9	2	9	1	53	3	9	2	14	2	11
1	10	2	5	1	24	2	10	2	9	2	56	3	10	2	15	1	87
						2	11	2	10	1	23	3	11	2	15	2	16
						2	12	1	9	1	35	3	12	2	16	1	8
						2	13	1	9	2	41	3	13	2	16	2	52
						2	14	1	10	1	43	3	14	2	17	1	77
												3	15	1	15	2	68
												3	16	1	16	1	81
												3	17	1	16	2	13
												3	18	1	17	1	19

Figure 43 Module map for SVT VXS crates 1 and 2

Hardware module mapping for MPOD crates is shown in Figure 44–Figure 46.

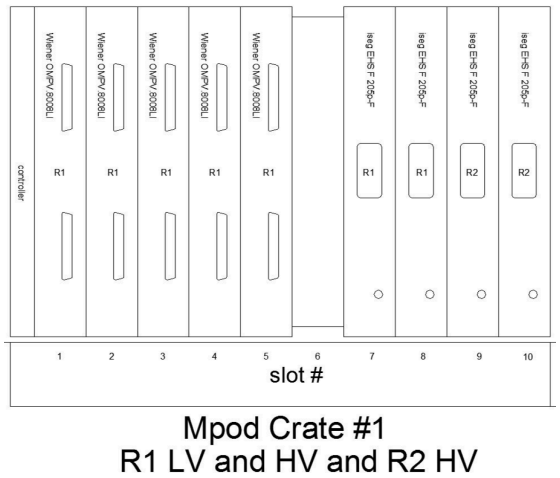


Figure 44 Power Supply Module Layout for MPOD Crate #1

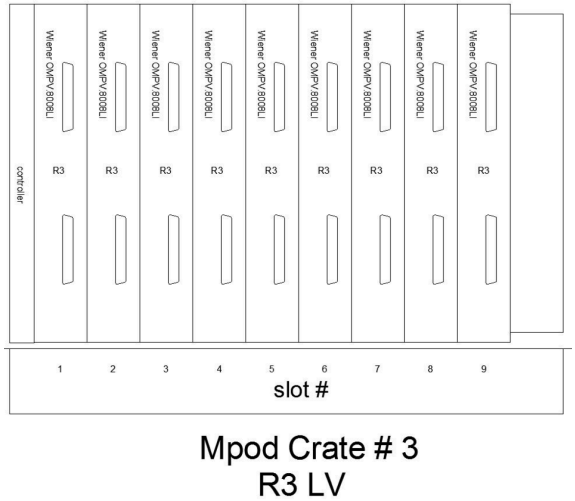


Figure 45 Power Supply Module Layout for MPOD Crate #3

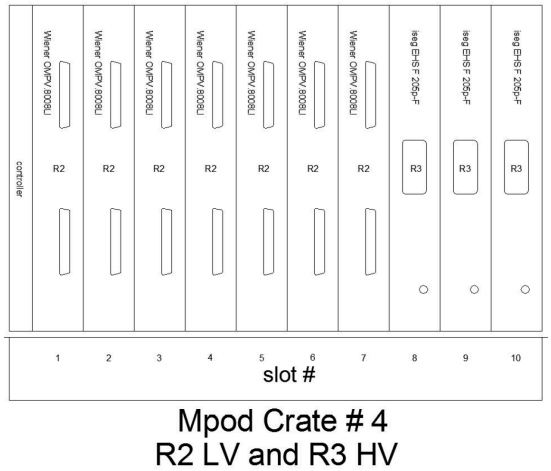


Figure 46 Power Supply Module Layout for MPOD Crate #4

Patch panel block layout and connection mapping is shown in Figure 47Figure 49.

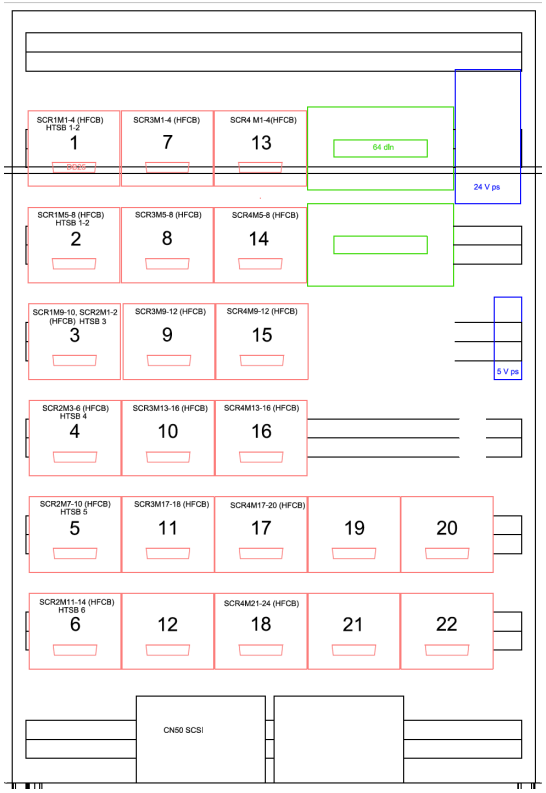


Figure 47 Patch Panel Block Layout

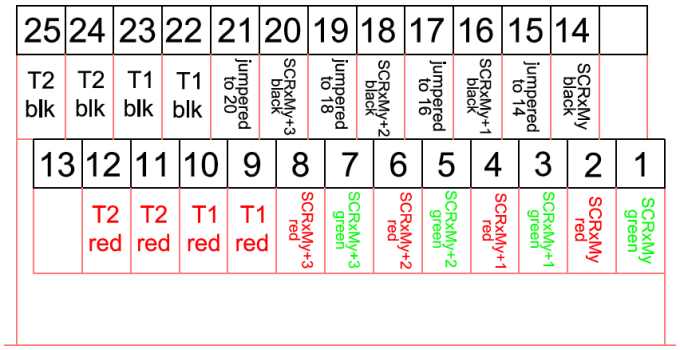


Figure 48 Patch Panel Blocks 1-18, except there are no T1/T2 connections (HFCBs) on blocks 7-18.

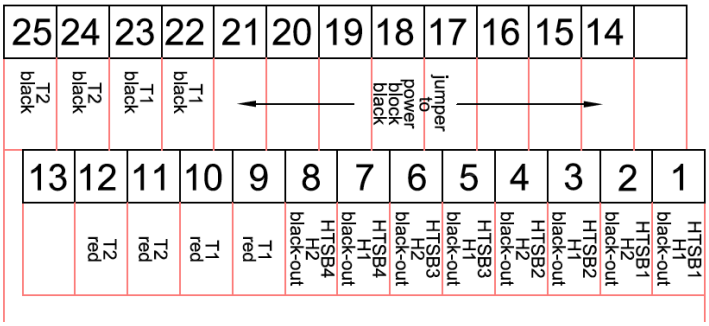


Figure 49 Patch Panel Block 19.

3.2.3 Cooling system

The front-end chips of the SVT modules have to be cooled to ensure normal operating conditions. Testing individual modules is done in the light-tight carrier boxes (Figure 50) with embedded heat sinks to which the modules are thermally coupled through the cooling contact surfaces. The chip temperatures, measured by sensors mounted on the electronics hybrid of the module, are monitored continuously. With passive cooling the modules have HV bias currents on the order of 0.4 μA at 85 V.

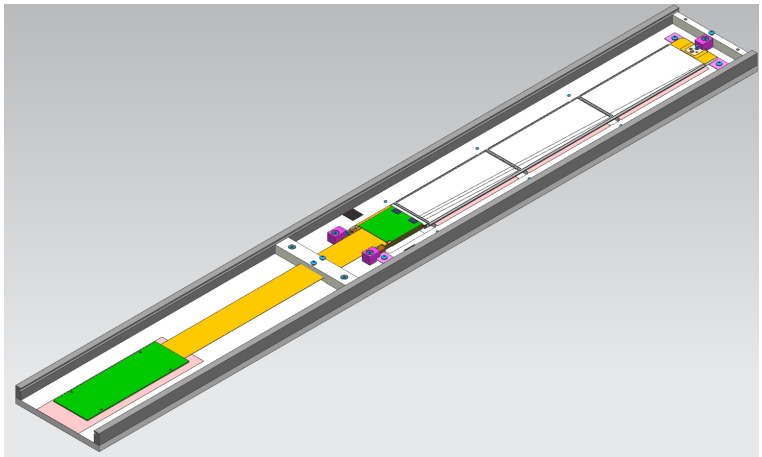


Figure 50 SVT module storage box

The SVT barrel requires a cooling system to keep the silicon sensors at a low temperature and to remove the heat produced in the readout electronics. Upper limits on the heat loads of the different heat sources in the SVT are calculated. Each module produces about 2 W of heat from the readout chips and up to 1 W due to the leakage current in the silicon sensors. This cannot be dissipated passively from the small SVT volume so active cooling is necessary.

The drip pans with plastic tubes are installed on the bottom of the SVT Faraday Cages.

3.2.4 Dry air purging system

The dry air flow is monitored by the slow control system. There are interlocks on gas flow and dew point. Dew point is calculated based on readings of multiple temperature and humidity sensors located inside and outside of the barrel. Dry air flow through SVT sensors is controlled remotely via MFC using the screen shown in Figure 51. Only SVT experts can change the flow settings. Dry air controlled by this MFC is cooled by passing it along with SVT liquid coolant line. It is essential for the SVT operation to keep this flow as it is used to cool the silicon sensors.

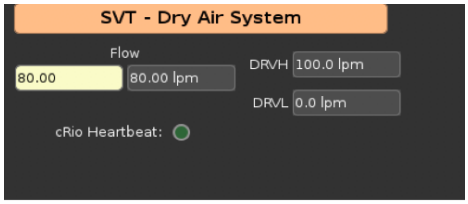


Figure 51 Dry air flow GUI

Air going through the MFC is bypassed via manual rotameter to ensure minimal flow in case of MFC failure. Manual rotameters are used to control the flow on the purging lines going through the SVT bore (between the inner shell of the SVT Faraday cage and the scattering chamber) and through the MVT bore (between SVT and BMT mounting tubes). Only SVT experts are allowed to change the flow settings.

3.3 *SVT Alarm Handler*

The alarm handler has built in logic algorithms, which are based on the fault charts. An example of the fault chart is presented in Figure 52.

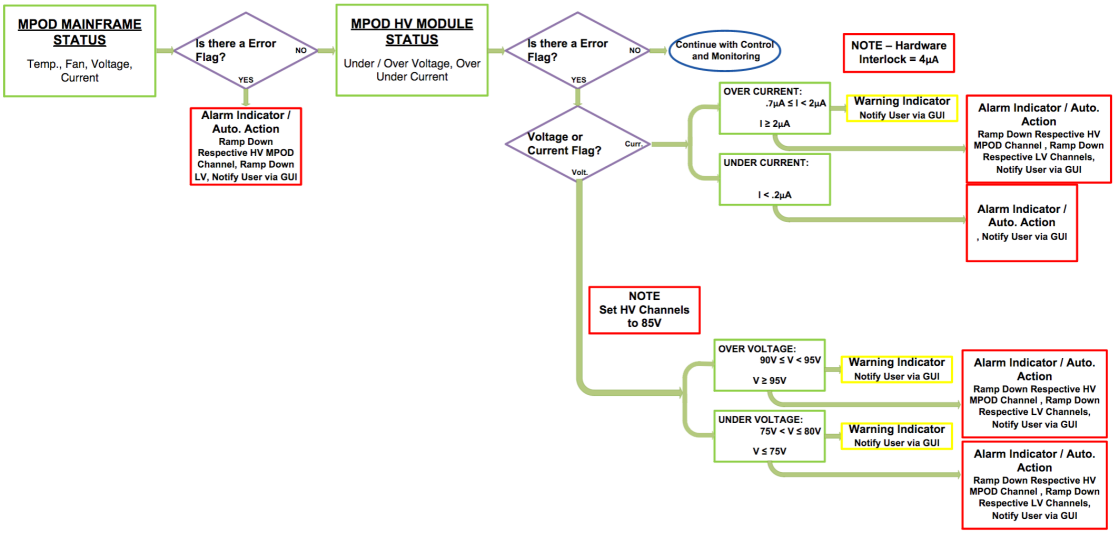


Figure 52 MPOD HV fault chart

Alarm handler logs are stored in the following directory:

/cs/dvlhome/apps/h/HallBSVTAlarms/dvl/output/

Interlock settings can be set by pressing on the "A" button for corresponding parameter. In the pop-up menu the software limits for warning (MINOR) and trip (MAJOR) state can be entered (Figure 53). Current value of the monitored parameter is displayed in the top right corner on the color-coded indicator.

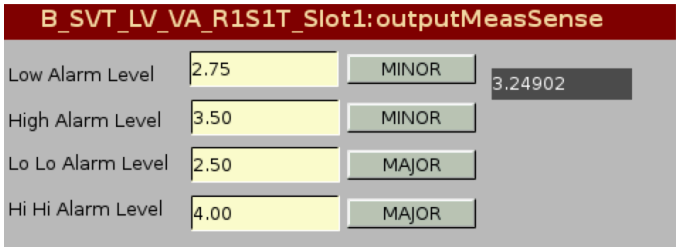


Figure 53 Alarm settings GUI

Restoring the software IOC configuration can be done using the "Save/Restore" button by the SVT or slow control experts.

3.4 *SVT DAQ*

SVT DAQ consists of 2 VXS crates with embedded crate controllers, readout cards, Signal Distribution (SD) cards, and Trigger Interface cards (TI). Modules are read out with VME Silicon Controller Module (VSCM) card (**Figure 54**), each card handles two SVT modules. Data acquisition is done with CLAS12 CODA system.

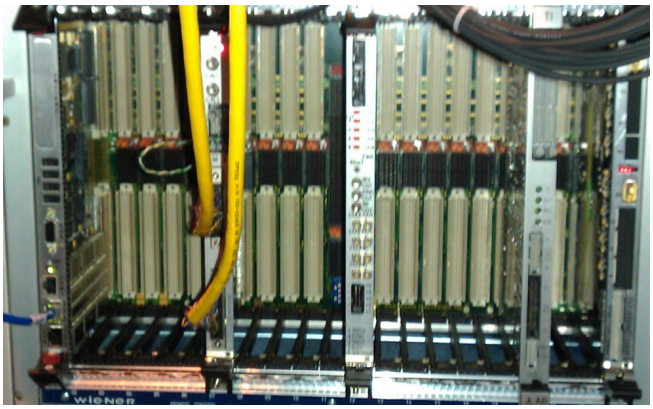


Figure 54. SVT readout VSCM module with two data cables in the VME crate.

4 SVT operation during tracker integration and commissioning

SVT assembly and commissioning is carried out at JLAB in the clean room in the EEL building. An important part of the commissioning is the exercise of the electrical functionality of the modules, by running appropriate tests to check continued operation.

The power cable connections for the assembly are the same as for the final system. Using the final power supplies requires the use of the appropriate connectors. The noise behavior of the barrel during assembly is directly comparable to the final system.

Noise figures are expected to provide a reasonable indication of performance in Hall B. Power supply currents and voltages are checked and the data path is checked using an analysis based on the raw data.

4.1 *SVT Calibration*

The front-end electronics has a built-in calibration facility, which allows charge pulses to be injected into the front end of the amplification stage upon request from the SVT Control System. The quantity of charge, the timing of the charge pulse and the sub-set of channels pulsed can be controlled by commands to the front-end chips.

With the binary readout architecture, the principal calibration procedure is to either vary the amplitude of the injected charge with fixed threshold or to vary the threshold with fixed amounts of injected charge. For each calibration pulse, the resulting status of the comparator (either hit or no-hit) is recorded. Result of one of these scans plotting detection efficiency as a function of threshold for a fixed input charge. The **"S" curve** response is typical showing 100% efficiency at low threshold and falling away to 0% efficiency at very high threshold. The point where this response crosses 50% locates the

mean value of the injected charge distribution. The width of the transition region (from 100% to 0%) measures the width of the distribution of charge measured at the comparator. For the case of calibration pulses of fixed amplitude, this distribution is, in fact, the composite noise of the readout system. A quick scan of each channel provides an easy measure of the overall gain of the analogue section (i.e. the 50% point) and the noise. Since the charge is injected at the very front of the readout stage and propagated through the entire chain, these calibration procedures provide an excellent diagnostic for the entire readout system.

The full calibration procedure will scan the threshold for a series of calibration pulses on each channel and collect the data. A quick fit of an error function to the "S" curve for each channel will produce the mean pulse amplitude and the standard deviation of the noise for that channel. These two values will then be stored in the historical trend charts for each channel and compared against allowed statistical limits.
The main function of the SVT DAQ during calibration is to produce occupancy histograms for analysis by the higher-level SVT DAQ software, known as scans.

The standard scan provides a histogram of the occupancy on a module as the threshold is varied.

SVT calibration scan takes about 20 minutes and is done with a terminal command:

clasrun@svtsystem1> calibration

During this scan the calibration of the SVT modules connected to the upper VSCM channels is performed first, then the modules connected to the lower channels are calibrated. The scan will produce the ASCII calibration files, one file for each chip. The directory in which these files are created is automatically created and is named by the time stamp when the scan started.

The calibration suite is launched with a command:

clasrun@svtsystem1> java –jar svtcalibration.jar

The calibration GUI will be opened and the directory containing the calibration files can be selected for processing from the menu. The processing of the calibration files takes 5-10 min depending on the CPU. When the analysis is done, the results of the SVT calibration will be presented in summary plots by pressing the "SVT" button.

The calibration GUI (Figure 55) has several windows. On the left side the detector view is shown. It displays the layout of the SVT modules in the barrel. Each module is represented by 4 rectangles according to the number of readout chips. Initial rectangle color is blue. The rectangles are placed in layers, the inner layer corresponds to the bottom sensors, the outer layer – to the top sensors. Region and layer numbering starts from 1 (inside out). The chips are numbered as 1 (U1 and U3), and 2 (U2 and U4). The module (sector) numbering starts from the bottom of each region.

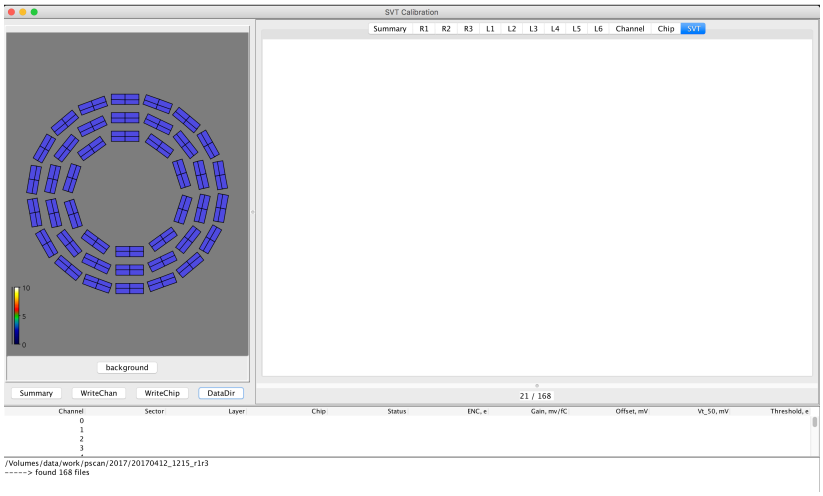


Figure 55 SVT Calibration GUI

On the top of the detector view there is a status panel which is filled with information when a specific chip is selected.

On the bottom of the detector view there are buttons to display the summary of the calibration analysis, to write the calibration tables as ASCII files for each chip or channel, and to select the calibration data directory and start processing the calibration scan.

On the right side of the detector view there are tabbed embedded canvases. The tabs represent different parts of detector. Region tabs (R1 to R3) display calibration plots for each region, layer tabs (L1 to L6) display plots for each layer. SVT tab displays calibration plots for the whole detector. Chip and Channel tabs show plots on a chip and channel (strip) level. Summary tab shows a histogram of operational percentage for the SVT and it's regions.

On the bottom of the canvas window there is an information panel showing the progress of the analysis (the number of processed chips and the total number of the chips in the calibration scan).

Below the button panel there is a table which displays the calibration constants for each channel of the selected chip.

On the bottom of the calibration GUI there is a log panel.

To start processing the calibration scan the directory containing the calibration data should be selected by pressing the "DataDir" button. The analysis will start when directory is chosen. The selected directory and the number of files in it (one file per each chip) will be displayed in the log view.

The progress can be checked on the information panel.

When analysis is done the log view will display the summary of the calibration data analysis.

This summary can be also displayed by clicking on the "Summary" button as shown in Figure 56.

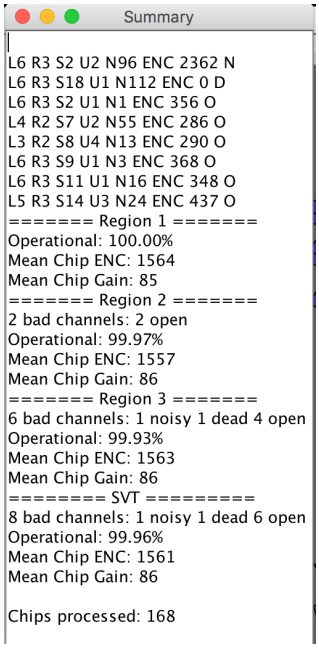


Figure 56 Calibration summary window

The summary starts with a list of bad channels found, their location (layer, region, sector, chip, channel number, ENC, channel status (N – noisy, D – dead, O – open), followed by the operational percentage, information about the bad channels, mean chip gain and ENC for each region and for the whole detector. Chips with bad channels are marked with maroon color in the detector view. If there are no bad channels found, the chip rectangle color is teal.

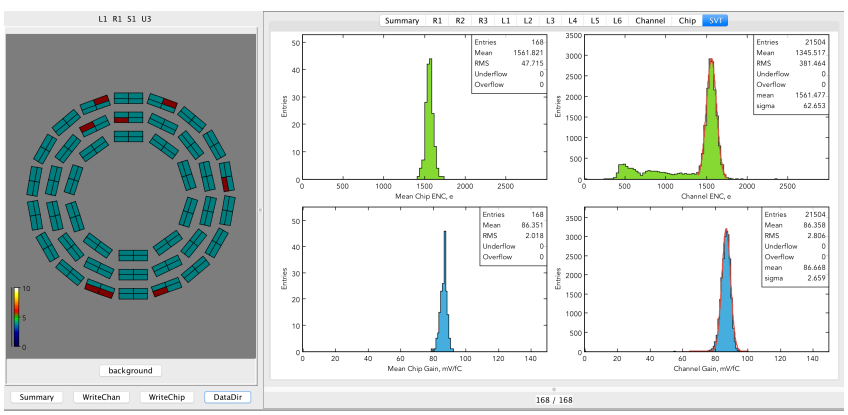


Figure 57 SVT Noise and Gain Calibration Summary Canvas

"SVT" tab has plots of ENC and gain for each chip and channel (**Figure 57**). Channel histograms are fit with a Gaussian. Mean chip gain and noise distributions are calculated for all the channels of U1/U3 chips, and for the first 50 channels of U2/U4 (33 cm long strips).

Channel ENC plot has a main peak corresponding to the full-length strips with mean around 1600 e, and a shoulder on the left side corresponding to the channels with shorter strips. The gain distributions are centered on ~85 mV/fC.

The “Summary” tab has a histogram (Figure 58) displaying operational percentage of the SVT (first bin), and of the regions (bins 1, 2, and 3).

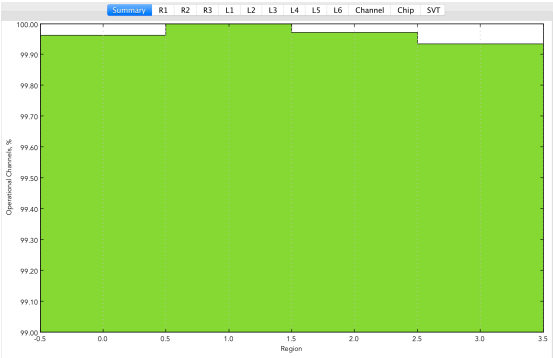


Figure 58 Detector operational percentage histogram

Region and layer tabs have the same plots as the “SVT” tab, filled for each region and layer separately (Figure 59Figure 60).

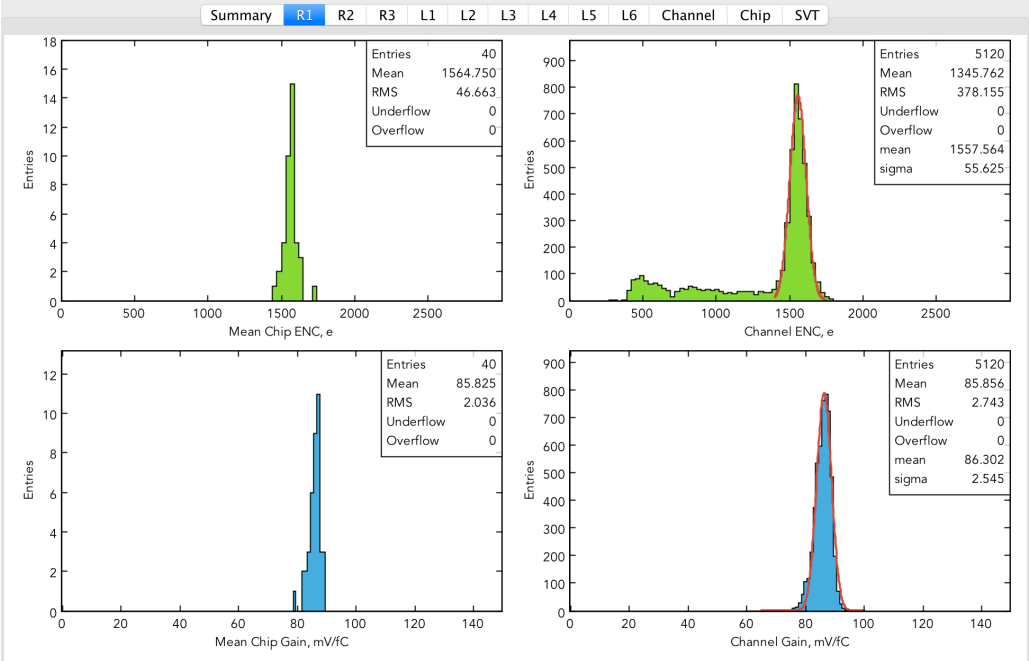


Figure 59 Calibration plots for Region 1

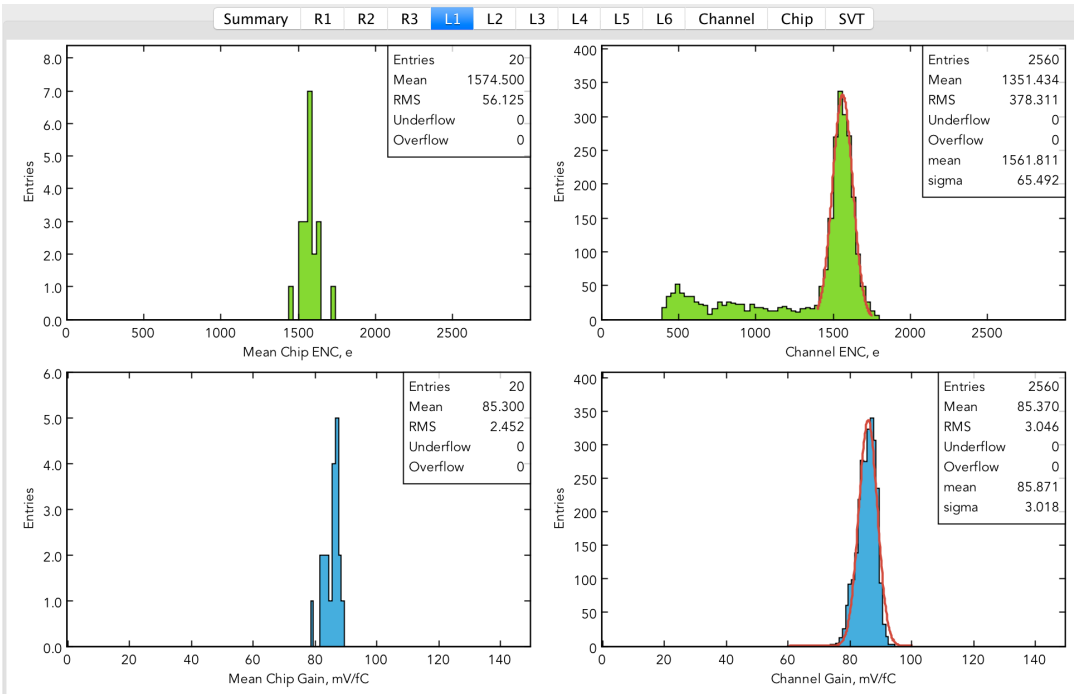


Figure 60 Calibration plots for Layer 1

Chip level plots can be displayed by selecting a chip in the detector view on the left side. The selected chip is marked with red color. The status panel on the top of the detector view is filled with information about the selected chip (layer, region, sector), crate, slot, VSCM channel (with blue color), mean ENC and gain of the chip. There are 6 pads in the "Chip" canvas: ENC vs. channel plot, gain vs. channel plot, gain dispersion histogram, threshold dispersion histogram, offset vs. channel plot, and V_{t50} vs. channel plot (Figure 61). For U1/U3 ENC and gain are uniformly distributed along the channels with slight shoulders at the chip edges. Mean ENC is about 1600 e, gain about 85 mV/fC. Offset and V_{t50} are also uniformly distributed along the channels, with V_{t50} around 300 mV and offset within tens of mV.

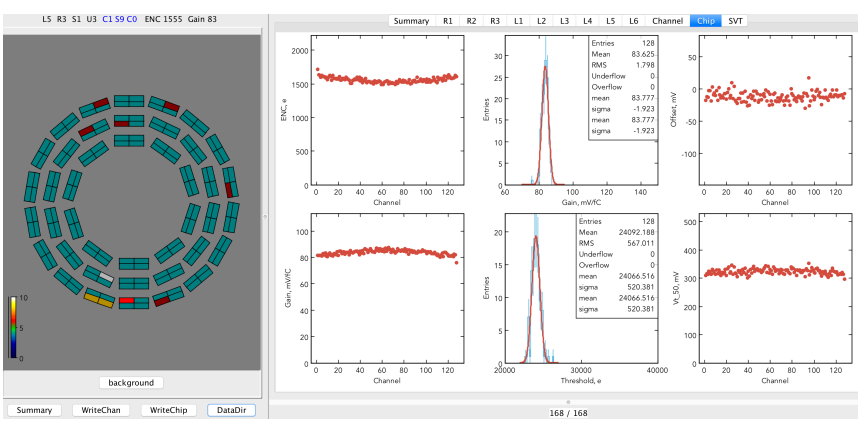


Figure 61 Typical calibration plots for U1 or U3 readout chips

The color of the chip rectangles which have been previously selected, will change to grey, if the chip has no bad channels, or to yellow, if there are bad channels found.

ENC vs. channel plot for U2/U4 has a slope starting at the channel 50 when the length of the strips starts to drop (Figure 62). Mean ENC and gain for these chips are calculated for the first 50 channels.

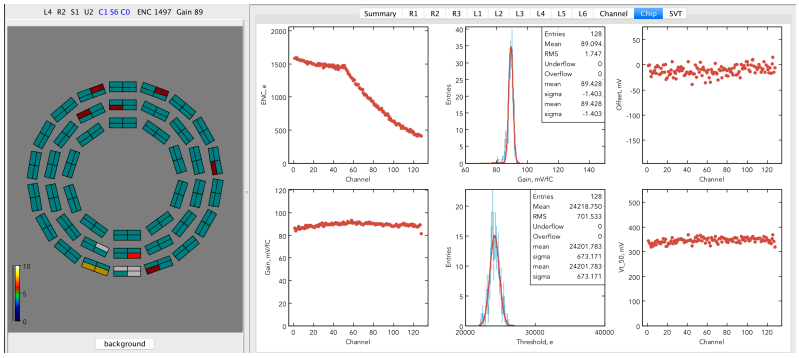


Figure 62 Typical calibration plots for U2 or U4 readout chips

In case where a bad channels were identified, the status panel would have their status (O – open, D – dead, N – noisy) and numbers in red color. An open channel would have low noise compared to adjacent channels (Figure 63). Dead channel would have ENC = 0.

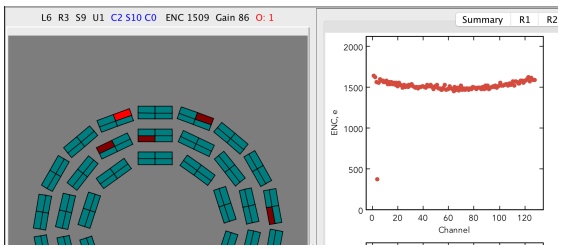


Figure 63 Example of a chip with an open channel

At the bottom of the histogram canvas there is a channel summary table (Figure 64). Each line corresponds to a single SVT readout channel (strip). The columns contain numbers for the channel location, status, ENC, gain, offset, V_{t50}, and threshold. Channel status is filled with an empty string for good channels, and with “open”, “dead”, “noisy” strings for bad channels.

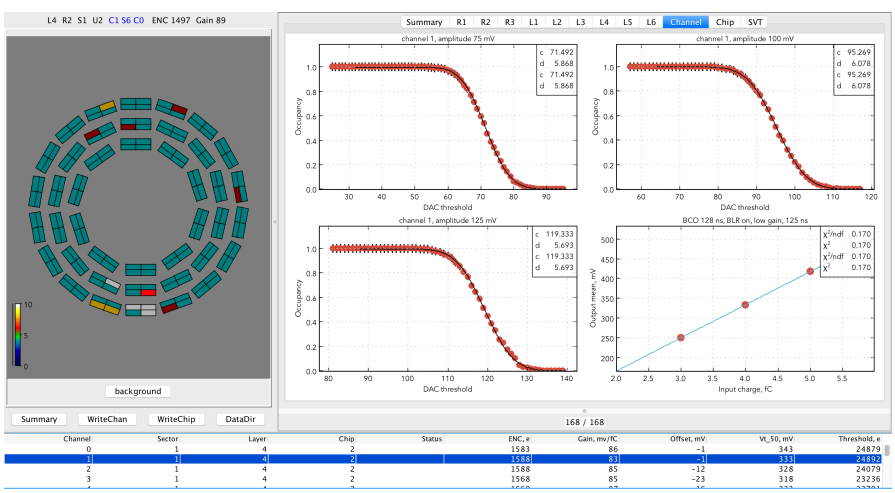


Figure 64 Typical calibration plots for a single readout channel

The channel occupancy and response curve plots can be shown on the “Channel” canvas by selecting the line in the table. The occupancy scans are done with calibration amplitudes of 3, 4, and 5 fC. Calibration constants for a channel are saved for the amplitude of 3 fC. The occupancy scans are fit with an error function. The parameter ***d*** corresponds to the Gaussian sigma of channel noise (in DAC counts). The parameter ***c*** corresponds to the amplitude of injected calibration charge. The response curve is fit with a line. The slope of this line corresponds to the channel gain in mV/fC, the intersect with Y axis provides the offset in mV.

In the rare cases where occupancy scan fit fails (Figure 65) the initial parameters of the erf should be adjusted by the SVT expert. In this example the channel was misidentified as noisy (see the status column) because even though 2 out of 3 erf fits converged, the fit for a scan with calibration charge equal to 3 fC which is used for ENC analysis, failed.

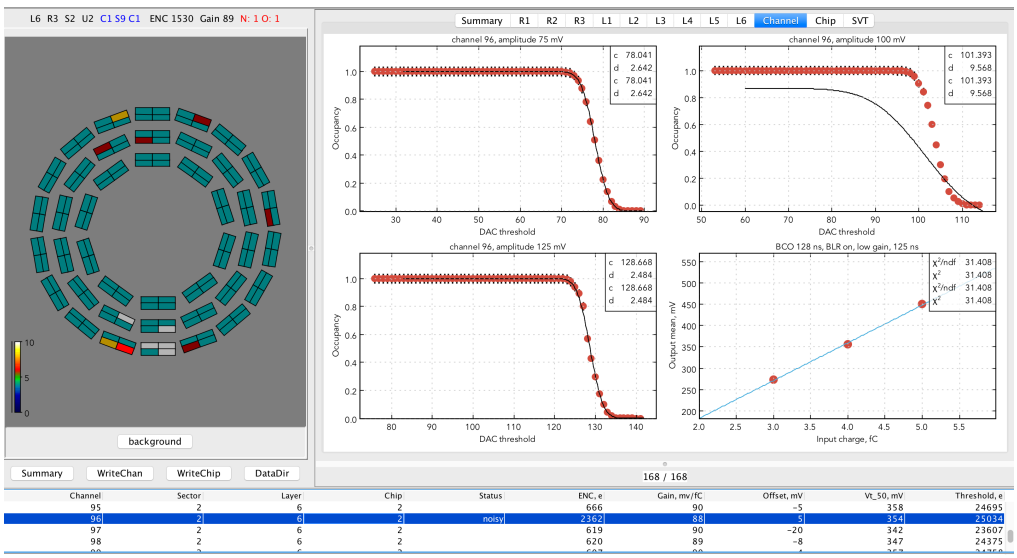


Figure 65 Calibration plots with failed fit of the threshold scan

In case of the dead channel, the threshold occupancy plots would have only zero occupancy data, and the response function plot would be empty (Figure 66).

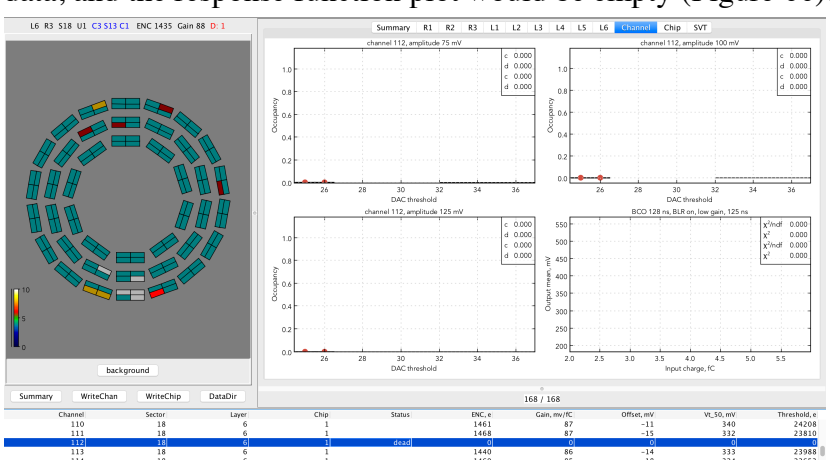


Figure 66 Channel calibration plots for a dead channel

SVT calibration data are stored in the CCDB. The ASCII tables with constants are written from the GUI by pressing “WriteChan”, and “”WriteChip”. Channel calibration table has columns corresponding to sector, layer, chip number (1 – U1/U3, 2 – U2/U4), mean, channel status (0 – good, 1 – noisy, 2 – open, 3 – dead, 4 - masked), ENC (electrons), gain (mV/fC), offset (mV), V_{t50} (mV), and threshold in electrons (Figure 67 left). There are 21504 rows in the channel calibration table. ENC and gain are calculated using calibration amplitude equal to 100 DAC.

Chip calibration table has columns corresponding to layer, sector, chip number (1 – U1/U3, 2 – U2/U4), mean ENC (electrons), ENC RMS, mean gain (mV/fC), gain RMS, mean offset (mV), offset RMS, mean V_{t50} (mV), V_{t50} RMS, threshold RMS (electrons), chip gain (0 – low, 1 – high), BLR mode (0 – off, 1 – on), BCO time (ns), shaper time (ns), 8 ADC thresholds in DAC (Figure 67 right). There are 168 rows in the chip calibration table.

```
1 2 1 1 0 1761 84 -14 322 23908
1 2 1 2 0 1698 82 -21 309 23347
1 2 1 3 0 1706 84 -22 314 23267
1 2 1 4 0 1640 83 -12 321 24070
1 2 1 5 0 1695 86 -7 336 24429
1 2 1 6 0 1645 85 -2 338 24817
1 2 1 7 0 1657 86 -13 331 23990
1 2 1 8 0 1648 85 -24 317 23209
1 2 1 9 0 1669 84 -7 329 24422
1 2 1 10 0 1628 86 -12 332 24083
```

```
1 2 1 1594  45  87   2 -22   8 327  10 573 0 1 128 125 30 45 60 75 90 105 120 135
1 2 2 1542  34  87   2  -8  11 342  11 812 0 1 128 125 30 45 60 75 90 105 120 135
1 1 1 1530  46  84   2 -16   8 322   8 582 0 1 128 125 30 45 60 75 90 105 120 135
1 1 2 1560  42  89   2 -12   6 342  10 421 0 1 128 125 30 45 60 75 90 105 120 135
2 2 1 1576  37  86   2 -11   8 333   9 595 0 1 128 125 30 45 60 75 90 105 120 135
2 2 2 1530  46  87   2 -15   9 334  11 623 0 1 128 125 30 45 60 75 90 105 120 135
2 1 1 1562  38  83   2  -7   7 326  10 538 0 1 128 125 30 45 60 75 90 105 120 135
2 1 2 1555  40  87   2  -9   8 341  10 560 0 1 128 125 30 45 60 75 90 105 120 135
3 2 1 1523  38  85   2 -10   7 329   9 482 0 1 128 125 30 45 60 75 90 105 120 135
3 2 2 1472  40  85   2  -7   8 332   9 571 0 1 128 125 30 45 60 75 90 105 120 135
3 1 1 1571  39  86   2  -7   7 335   9 555 0 1 128 125 30 45 60 75 90 105 120 135
3 1 2 1561  40  85   2 -12   8 327  10 598 0 1 128 125 30 45 60 75 90 105 120 135
4 2 1 1535  38  86   2 -10   8 334   9 542 0 1 128 125 30 45 60 75 90 105 120 135
```

Figure 67 Tables of the calibration constants per channel (left), per chip (right)

4.2 *General procedures for SVT module services*

Here are the general procedures to turn ON and OFF module services:

Turning the SVT system ON (from the OFF state):

- Turn on the slow controls VME crate (if it is in powered off state)
- Start EPICS detector control and safety system
- Check the gas flow in CLAS CSS, the flow should be about 80 lpm. Monitor the flow and detector ambient conditions (detector internal humidity should be less than 30%).
- Turn on the DAQ VXS crates (if they are in power off state), check the crate status displays
- Turn on the MPOD crates, (if they are in power off state), check the status displays
- Turn on the chiller, check for leaks and coolant level
- Turn on the SVT module LV (analog and digital, see below), check the PS status
- Turn on the sensor bias (HV), check for PS status (voltages, currents)

Turning the SVT system OFF:

- Turn off HV
- Turn off LV
- Turn off the chiller, monitor detector ambient conditions

- Turn off gas purging system (during normal operation in the Hall gas purging system is always ON)
- Turn off MPOD crates (if crate maintenance is required, during normal operation crates are always ON)
- Turn off VXS crates (if crate maintenance is required, during normal operation crates are always ON)
- Turn off slow controls VME crate (if crate maintenance is required, during normal operation crate is always ON)

4.3 *SVT operation during commissioning with cosmic rays*

The SVT is tested with cosmic rays to test performance, measure efficiencies, and collect alignment dataset. Cosmic rays are triggered using the coincident signals from the signal distribution boards in the VXS crates. The resultant hit data are transferred by the SVT DAQ, written to disk, and analyzed offline. As well as using the cosmic trigger, noise data are recorded in physics mode under a variety of test conditions, using fixed frequency or random triggers.

To time-in the SVT with the cosmic trigger, the modules' relative timings are calculated from known differences in cable lengths. The global delay is determined using dedicated monitoring histograms which record, as a function of the global delay, the number of coincident hits on neighboring chips on opposing sides of each module. After timing-in, hits from cosmic rays traversing the SVT can be observed on the online event display.

Steps to take a cosmic run:

- Start EDM (edmRun)
- Launch SVT menu GUIs (SVT/mainMenu)
- Set the SVT operating temperature via the SVT chiller controls
- Monitor the SVT temperatures, humidity, and dew points
- Control and monitor gas purging system
- Turn ON/OFF LV and monitor LV currents
- Turn ON/OFF HV and monitor sensor leakage currents
- Run module calibration scans if needed ("calibration")
- Start CODA ("runcontrol –rocs")
    - connect
    - configure
    - download (select the trigger configuration file)
    - prestart
    - start cosmic data run (go)
- Monitor the trigger and data rate
- End run

5 SVT operations during tracker integration and commissioning in Hall B

5.1 *Transportation requirements*

Because of the delicacy of the silicon modules, it is required that the SVT be transported to Hall B in an air-sprung, temperature-controlled, humidity-controlled thermal screen mounted on a truck. The acceleration experienced by the transport box is required to be less than 3 g (where g is the acceleration due to gravity) to avoid damage to the silicon modules and shaking loose connectors. The tilt is required to be less than 10°. The temperature is required to be 20 ± 3°C to avoid thermal stresses and the humidity kept at around 40% and certainly less than 70% to avoid condensation forming on the modules.

5.2 *Tracker integration tests*

The testing during tracker integration in Hall B is focused on checking the integrity of the service connections, performance of the cooling, and then verifying that the additional components did not cause deterioration in the SVT electrical performance. This latter part of the testing is crucial in demonstrating that whole SVT system design is robust with respect to inter-module pick-up and external interferences. No significant differences should be seen compared to the results from the testing of the SVT in the assembly clean room.

Before transportation to Hall B, the SVT is integrated with Micromegas. Further tests, including combined SVT/Micromegas cosmic ray studies, will then be performed in Hall B during detector integration and commissioning. These are the first large-scale tests of the SVT DAQ in physics mode. Several millions of physics-mode events are recorded in the synchronous operation of all SVT modules during the commissioning. In the noise tests, the occupancies obtained should not be significantly different from those found for tests made on the SVT before integration. No significant change in noise occupancy should be observed when running concurrently with Micromegas, when running at different trigger rates, or for synchronous versus asynchronous triggering. The data and control cable connections are monitored by the DAQ and the remainder are controlled and monitored by the DCS.

6 Module quality assurance measurements

For testing the SVT modules, a series of tests are planned. The goal of the performance tests is to check the functionality of each of the modules. These tests include measurements of:

- **Sensor current**: Check that the sensor behaves like a diode and can be fully depleted. The maximum allowed leakage current is 10 nA/cm^2 (470 nA per sensor).
- **Analog functionality of the module electronics**: Test the readout of the strips and ensure that at least 99% of all silicon strips can be read out and the noise on the strips agrees with the expected value for that module.
- **Digital functionality of the module electronics**: Check that the data can be read

out by the data acquisition system. In addition, the channel masking and chip basic functionality is tested.

- **Final commissioning**: After installation in Hall B, the SVT is tested to check that no problems have occurred during installation of the detector and to test the connections with the readout systems in the services caverns. A series of physics runs are performed with and without the beam and magnetic field.

At each of these stages, the tests for the module performance are repeated. Tests at later stages are aimed at finding problems with data acquisition and services, such as the power supplies and cables, and ensuring that no common mode noise was added to the system due to grounding/shielding problems.

With the SVT in its final position in the CLAS12 detector, all the modules are re-tested with the actual services that are used to operate the SVT during data taking.

6.1 *Digital tests*

The digital tests check functionality of the digital part of the FSSR2 chips on the module and the ability to read out data from the module. All the tests are based on measuring the occupancy of each channel while varying a specific setting in the chip configuration. The correct cabling has to be verified before the digital tests take place, as problems with the module communication would lead to test failures.

6.1.1 Module communication

When first powered, basic communication is confirmed when the SVT modules write to the chip registers and read back the response. The front-end electronics is set up to return the contents of their configuration registers, so a known bit pattern can be expected. A hard-reset test checks the initialization of the modules. Once the module has been checked for basic power and readout functionality, the electrical performance can be tested.

6.1.2 Channel masking

The readout chips of the modules apply a mask to the measured hits on all the strips. A channel that is masked always returns “0”. Masking is necessary for strip channels with high noise, as unmasked noisy channels add fake hits and increase the amount of data that has to be read out.

To check the capability of the chips to turn a mask on and turn a mask off all the channels on the chips, the trigger occupancy is measured using different settings of the mask register. During the test, the output is set such that any channel which is not masked returns a signal corresponding to “1”. The test starts with a mask register where all channels are unmasked. For each consecutive mask register in the test, one more channel on each chip is masked, until all channels are masked at the final mask register. The result of this test is a 2D projection of a 3D histogram, where the shade of color indicates the trigger occupancy as a function of the channel number and the mask register.

If there is a channel that will need to be masked due to high noise, which also had a masking defect, it will have to be masked offline.

6.1.3 Front-end calibration

The binary threshold must be set so that a channel can reliably distinguish between the signal and noise. This means that the response to different signals must be known and the noise must be low enough to be cut out. The testing of SVT modules is a check of their calibration and performance and also of the test system itself. The key to the characterization of the modules lies in reconstructing the analog response of the modules from the binary readout by first setting the optimal chip parameters for the charge injection, then injecting a set of charges into the front-end, and scanning through the threshold to map out the response curve. A full test sequence contains procedures that verify the digital performance of the chips. These exercise and test the channel mask registers and chip logic.

6.2 *Analog tests*

In the analog stage, the signal induced in the strip is amplified, shaped, and discriminated using a threshold setting. There are physics-driven requirements for efficiency of 99% per strip (low false negatives) and noise occupancy of 10^{-3} (low false positives) at the nominal threshold. For data taking, the default setting of the threshold is chosen such that it corresponds to the output signal as created by an input signal equivalent to about 1 fC charge induced on the strip. A signal of 1 fC is well above the expected noise, and well below the average induced charge from the passage of a charge particle. To find the threshold corresponding to 1 fC, the analog response needs to be reconstructed for each channel. The loss of information from the binary readout system implies that the threshold set on a chip must have a well-known correspondence to the charge deposited in the detector. There is also a need for the threshold charge to be the same across the channels in a detector - if different channels responded differently to deposition of the nominal threshold charge, the track-finding algorithms would be biased by the potential extra hits. Any spread in the response among the different channels of a chip results in a spread of the efficiency and noise occupancy, which degrades effective performance. This leads to a requirement that the channel-to-channel variations in threshold and noise are kept to a minimum.

The FSSR2 has a Base Line Restoration (BLR) circuit which can be turned on and off with BLR parameter. Typical pulse shape after the BLR is shown in Figure 68. To meet the specifications, the threshold dispersion of the FSSR2 chip has to be within 500 e for BLR ON setting (800 e for BLR OFF). A goal of the binary readout architecture is to keep the threshold spread negligible compared to the noise value for a full strip length. A comparison of the noise of 2000 electrons for 33 cm strips with the threshold spread of 500 electrons demonstrates that the threshold spread is negligible compared to noise and if such, it will not affect neither the efficiency nor the noise occupancy.

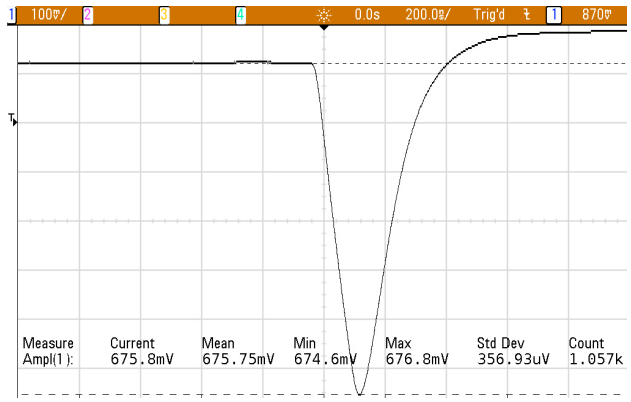


Figure 68 Single channel analog output pulse measured after the Base Line Restore circuit.

The active part of the SVT module is the silicon detector. It reacts to ionizing particles that pass through, generating a charge that is discriminated by the chips on the hybrid. The detector medium is a silicon crystal. The 320 μm substrate is over-doped n^+, covered with a thick layer of lightly doped n-type silicon. Strips of p^+ silicon at the surface are covered with aluminum tracks, which conduct the charge to the electrical read-out. A voltage around 80V is applied to the backplane, which fully depletes the n-type region and allows the collection of a minimum of ~2.4×10^4 electron-hole pairs, for a normally incident minimum-ionizing particle (MIP).

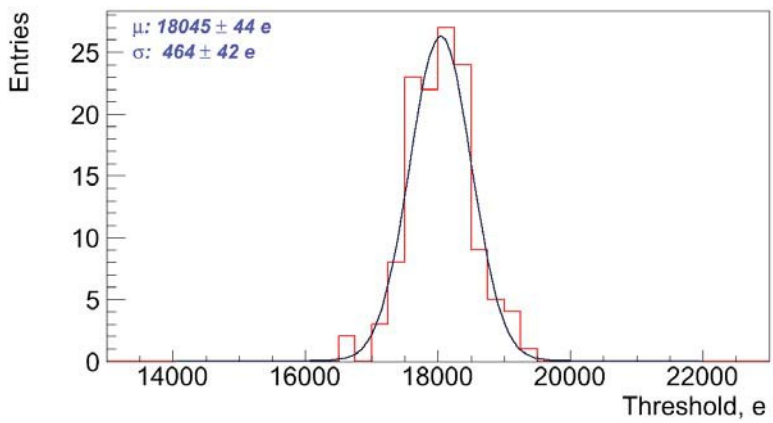


Figure 69. Example of the chip threshold dispersion measurement.

Measuring the analog response signal on the strips allows the determination of the input noise of the strips. One of the requirements of the silicon sensors is that the noise on the strips does not exceed 2000 electrons, which will guarantee noise occupancy on the silicon strips of less than 10^{-3}. The measurement of the input noise is also used to determine the total number of usable channels in the SVT, which is required to be greater than 99%. There is an allowance for bad channels during production. This is specified to be 1%, or five channels per module. As several bad channels in a row would reduce the sensitivity to multiple hits, a limit of four consecutive bad channels is applied.

6.2.1 Reconstruction of the analog strip response

Since the SVT modules are designed with a binary readout system, the analog channel

response cannot be measured directly. Instead, the analog response is reconstructed by injecting a calibration charge on the channel and measuring the corresponding occupancy over a range of threshold values. The calibration charge is produced by the charge injection circuitry of the readout chip.

The injected charge is shaped and amplified in the analog circuitry to form an output signal. The discriminator threshold determines whether or not the output signal corresponded to a hit. The probability that the injected charge produces a hit depends on the setting of the discriminator threshold. The average hit probability is measured by repeating the process of injecting charges and counting the fraction of readout triggers that produced a hit. This measurement is repeated over a range of threshold settings to produce an occupancy plot. The occupancy plot represents the probability *p* that a channel registers a hit at certain threshold voltage V_{thr}, given by:

$$p(V_{thr}) = \int_{V_{thr}}^{\infty} f(s)ds$$

where *f(s)* is the probability distribution function that gives the chance of measuring a signal with a signal height *s*. The signal height distribution is assumed to be Gaussian:

$$f(s) = \frac{1}{\sigma_s\sqrt{2\pi}} e^{-(s-\mu_s)^2/2\sigma_s{}^2}$$

where μ_s is the mean signal height and the width of the Gaussian σ_s is the RMS noise of the signal. In between the high and low threshold regions, the occupancy curve is described by an error function, or S-curve (see figure 3), which can be fitted to the occupancy histogram for each channel, producing a mean value (discriminator threshold) and standard deviation (noise). Recording about 1000 events per threshold setting allows the appropriate mean and sigma to be extracted. By fitting the S-curve, the data acquisition software can determine the ENC of the module. Problem channels, such as where the fit fails, are tagged with defects and the generated data are placed in the database.

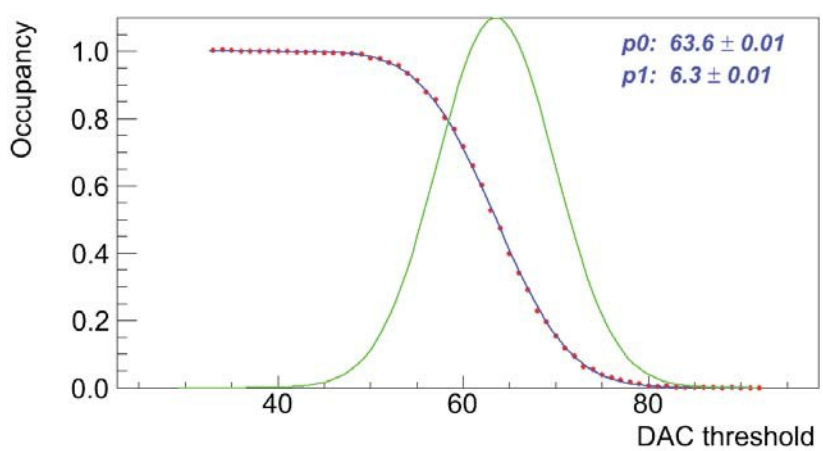


Figure 70. Typical example of an S-curve (red dots) as measured on SVT channel. The corresponding erfc fit (blue line) and signal response shape (green) as a function of signal height are also presented.

During the analog tests, S-curves are measured for all the chip channels over a range of values for the injected charge (Figure 70, Figure 71). The threshold setting at which the probability of getting a hit is 50%, corresponding to μ_s, is **defined as the V_{ts0}-point**. The value of the V_{ts0}-point for each channel should increase linearly with the value of the injected charge, while the output noise, σ_s, is expected to be approximately constant as a function of charge. In practice, the output noise of each channel on the module is determined as the value of σ_s from the S-curve, obtained with a 3 fC input charge. The scans with no charge injection are also part of the module characterization sequence.

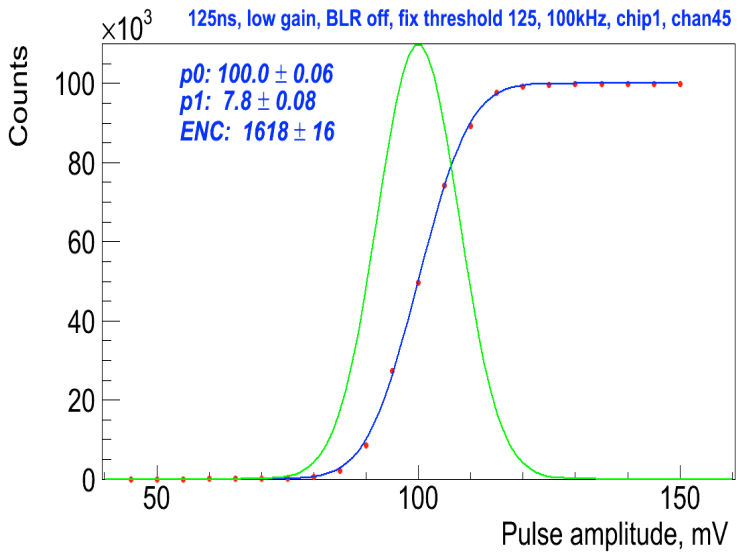


Figure 71. S-curve (red dots) measured with a fixed hit/no hit discriminator threshold and varying the amplitude of the injected calibration pulse. The corresponding erf fit (blue line) and signal response shape (green) as a function of signal height are also presented.

6.2.2 Noise and gain measurement

The S-curves that are measured for each SVT channel determine the output noise on the signal. By measuring the gain of the analog signal amplification, the input noise of each channel can be determined. The input noise can be used to identify several channel defects and helps to determine if the module is properly biased.

Response Curve: performs a 10-point gain scan. These data are then used to generate a response function, which maps injected charge to discriminator threshold (Figure 72).
Three Point Gain Test: the gain is determined for each chip by measuring S-curves at three different values of the injected charge: 3 fC, 4 fC, and 5 fC. One thousand events are sent for each bin and the range of threshold values is chosen according to the size of the injection charge. The gain (in mV/fC) then follows from the slope of a linear fit to the three V_{ts0}-points as shown in Figure 73. It is used to measure the noise of a module and the similarity of response across the channels of a module. The output noise of each channel divided by the gain-factor of the chip results in the measured value of the input noise.

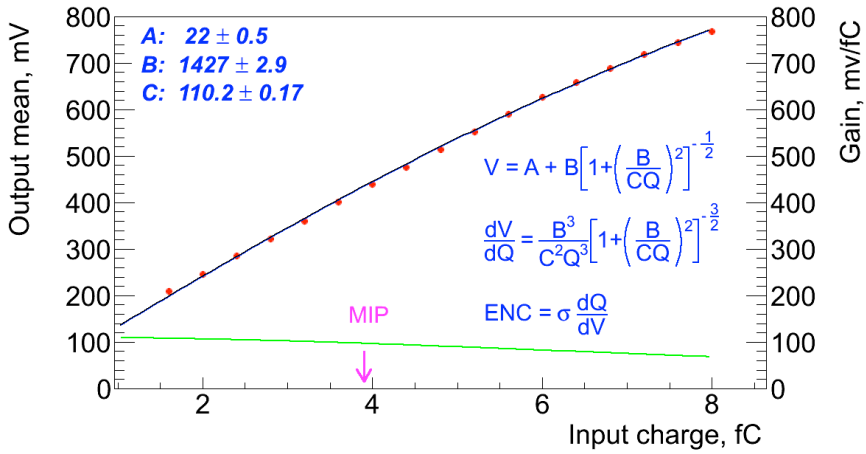


Figure 72. Response curve of the FSSR2 channel. Data (red) are fitted with a function (black) and gain is calculated at every point (green). Charge corresponding to the MIP is also shown.

Similar to the chip gain, to measure the channel gain, for each channel, a straight line is fitted to the mean and sigma parameters from the three scans in the test. The gradient of the slope represents the gain of the front-end amplifier at this point. This is used to translate the noise recorded at the output of the amplifier to that seen on the input. The onset of the straight-line fit is also recorded. Channels with too much noise are tagged as defective.

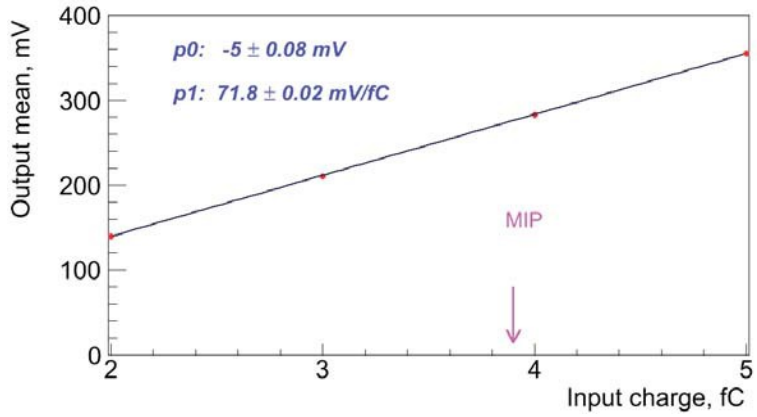


Figure 73. Example of fit to determine gain (in mV/fC) from measurements of the V_{50}-points at four different values of the input charge. The V_{50}-points represent the average value for all channels on the readout chip.

A summary of this data is recorded which includes the mean values per chip of the gain, offset, output noise, and input noise. Also recorded are the parameters for each chip of the straight line fit. During the calibration, a dedicated controller monitors the test results and when they are available, updates the configuration with the response curve parameters and masks channels that were recorded as defective.

One of the largest contributions to gain variation in the readout system is the chip-to-chip variation of gain. Changes in the chip LV or environmental temperature can also affect the gain of the readout channel. The response of all detector channels can be further

equalized during offline reconstruction by correcting the signal magnitude by the normalization factor. This procedure will be verified in further studies due to low granularity (3 bit) of FSSR2 Flash ADCs. Figure 74 shows the calibration plot for the flash ADC. Figure 75 shows gain dispersion in one of the chips of the module.

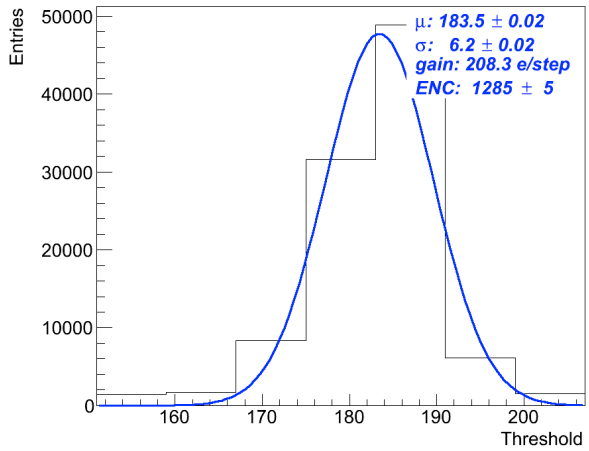


Figure 74. Flash ADC calibration.

The Calibration Client Graphical User Interface (GUI) monitors all of the information and stores and displays a view of selected data, for instance the noise figures for all of the connected modules, in a color-coded diagram.

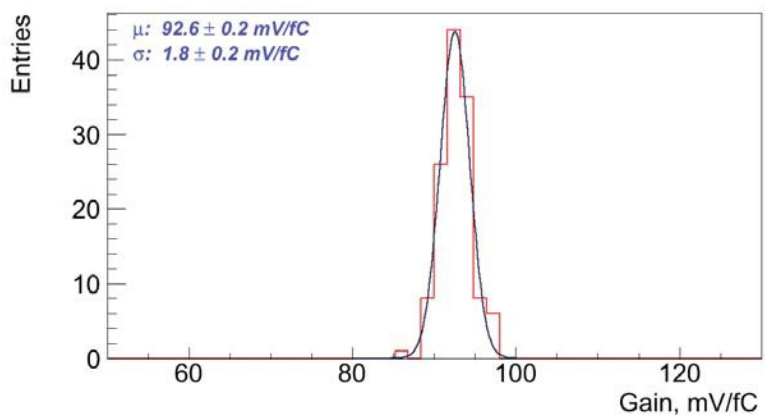


Figure 75. Example of the channel gain dispersion measurement.

From the measurement of the input noise, several channel defects can be identified. The main channel defects are defined as:

- **Dead:** measured input noise = 0, no hits are measured at any threshold for any injected charge.
- **Un-bonded:** measured input noise is < 800 e, most likely as a result of a broken bond between the FSSR2 and the first silicon strip sensor or the pitch adapter.
- **Partially bonded:** measured input noise is < 1500 e, a result of a broken bond between the daisy-chained silicon sensors (the threshold depends on the strip length of the tested channel).

- **Noisy:** the input noise is greater than 1.15 times the average input noise of all channels on the same chip.
- **Hot:** the input noise is greater than 1.25 times the average input noise of all channels on the same chip (the thresholds are defined experimentally).

The assumptions made for the input noise of partially bonded and un-bonded channels are based on the fact that the capacitive load on the channel is decreased when the silicon strip sensor is removed from the readout chain, resulting in a lower noise contribution, typically around 1000□1500 e.

The input noise also depends on the temperature of the silicon. The sensor temperature typically varies between modules and depends on the settings of the cooling used during the test. In the region of module temperatures during the assembly tests, the temperature dependence of the input noise can be approximated by a linear function. The slopes of the straight-line fits can be used to apply a temperature correction to the average measured input noise on each module, so that all results for the input noise correspond to a hybrid temperature of 25°C.

Noise Occupancy Test: one scan (occupancy histogram, see Figure 76) with no charge injection to find the noise value. This probes the tail of the noise distribution, which can show effects, which are masked by the higher occupancy at low thresholds. It also provides a crosscheck of the noise value obtained from the response curve measurement.

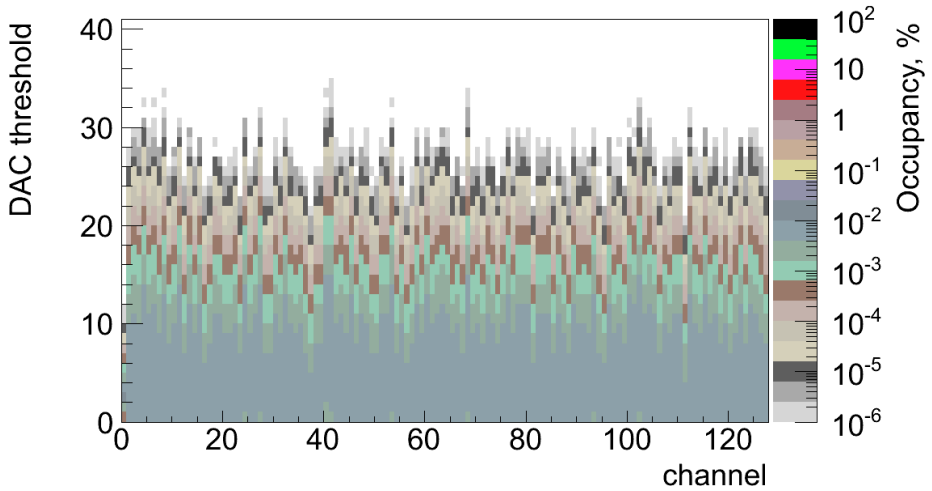


Figure 76. Channel noise occupancy vs. DAC hit/no-hit threshold (in DAC bins, One DAC bin corresponds to 3.5 mV).

It is important to ensure that the input noise of the modules does not increase with services successively added to the system, as that would indicate problems in the grounding scheme and common-mode noise has been introduced into the system.

6.2.2.1 Calibration of the detector channel noise

The noise and threshold dispersion constants for each individual detector channel must be measured, as these values are used by the zero-suppression algorithms implemented in the core logic of the FSSR2 and by calibration procedures to identify defective channels.

Noise is measured using external, low frequency calibration charge injected in the absence of signal. Longer silicon strips have higher capacitance and thus a higher expected value for the input noise. Noise calibration should account for the different strip lengths and pitch adapter layouts that affect the input capacitance of the preamplifier. Threshold dispersion is defined to be the standard deviation of the distribution of means obtained from the parameters of the complementary Erf fit as described in section 6.2.1. Fitting the mean noise versus silicon strip length, the following parameterization is obtained:

Noise (e) = A + B × length (cm),

which should be compatible with the measurements performed during the SVT integration period, prior to installation.

Figure 77 shows examples of the input noise measured for the 256 channels of the top side of the pre-production module. One can notice the channels with open inputs and noisy strips. These defects are identified during module QA procedure.

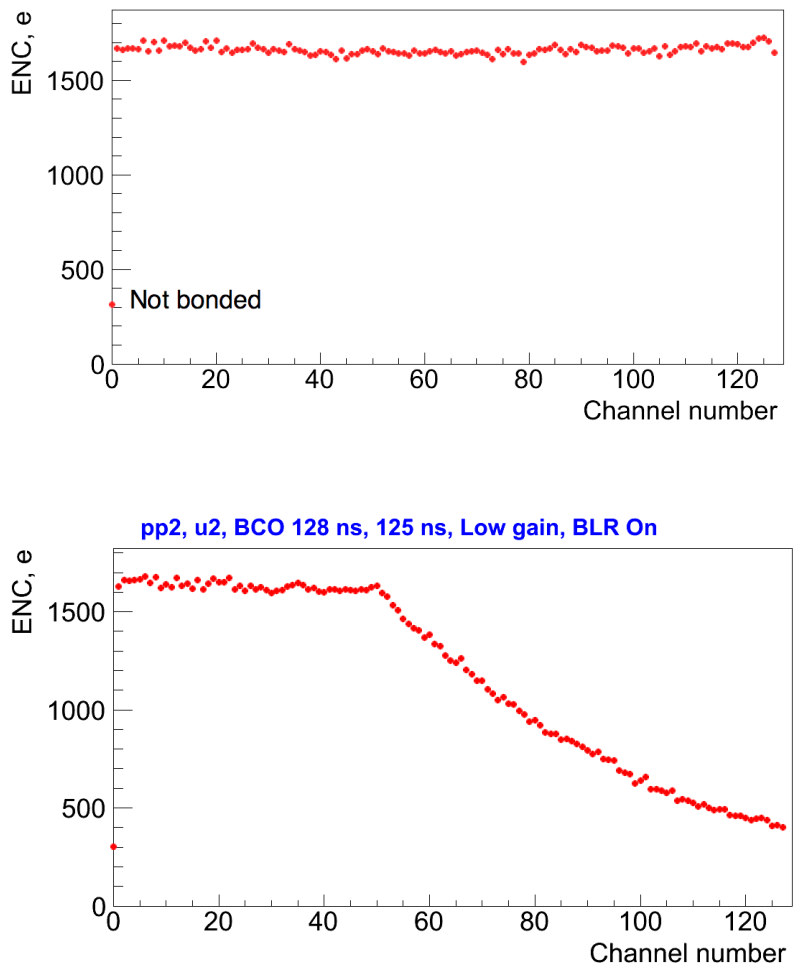


Figure 77. Example of the input noise measured on the top side of the SVT module. First readout chip (top plot) is connected to the longest strips (~33 cm) while part of the second chip (bottom plot) is wire bonded to the shorter strips due to variable pitch design of the sensors.

The average noise in these two chips is below 1700 electrons which is typical value for the module. The expected value of the input noise depends on the length of the silicon strips as shown in Figure 78.

The individual sources of noise on the detector module can be identified and measured by plotting the ratio of the minimum to the median noise value for each FSSR2. The ratio takes advantage of the fact that broken wire bonds on the detector modules effectively reduce the input capacitance to individual channels of the FSSR2 chips. Broken wire bonds can occur between (in ascending order of capacitance): the FSSR2 and pitch adapter, the pitch adapter and silicon sensor, and between the sensors. Fitting to these populations, corresponding to the previous broken wire configurations provides an estimate of different noise contributions.

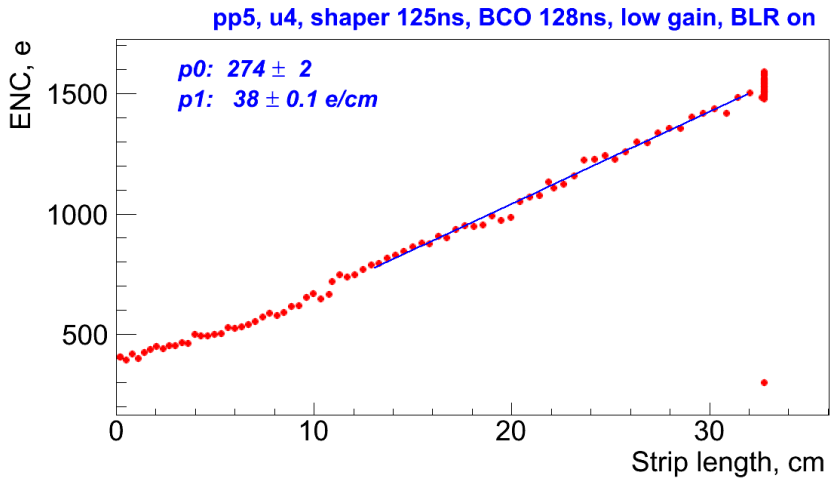


Figure 78. Input noise versus strip length showing the straight line fit as expected from the linear dependence of the channel noise on the preamplifier capacitive load.

6.2.3 Defective channels results

The number of channel defects found per module by measuring the input noise on the modules, is reported and recorded in the SVT conditions database, separated into the different types of channel defects. The data collected during module production, JLAB reception tests, SVT assembly, and final commissioning are analyzed to verify that no significant change in the number of channel defects is found between the different test stages. From the defective channel results, the percentage of operational channels is calculated.

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