Update/Status for NPS HV, Electronics, DAQ

Brad Sawatzky

NPS Collaboration Meeting

Feb 3, 2020

Needed Readout Hardware for NPS

- **NPS: 1080 $PbWO_4$ blocks**
  - → Readout consists of JLab F250 FADCs
    - » Full waveform for crystals of interest
    - » < 1ns timing res. is provided by F250s
  - → NPS trigger generated by JLab VTP modules in NPS F250 VXS crates
- **Hardware needed for NPS**
  - → 67x FADCs
  - → 5x VXS crates
  - → 5x SD + TI + Linux SBC / ROC
  - → 5x VTP modules
- **Firmware development**
  - → VTP firmware updated to provide required summing trigger
  - → TI/TM firmware modified to support full complement of 5 NPS crates + 3 HMS crates

- **NOTE: VTP firmware trigger latency is NOT a problem**
  - → All HMS modules (F250s, CAEN 1190s) have deep lookback buffers
  - → HMS pre-trigger(s) will be delayed to meet VTP trigger

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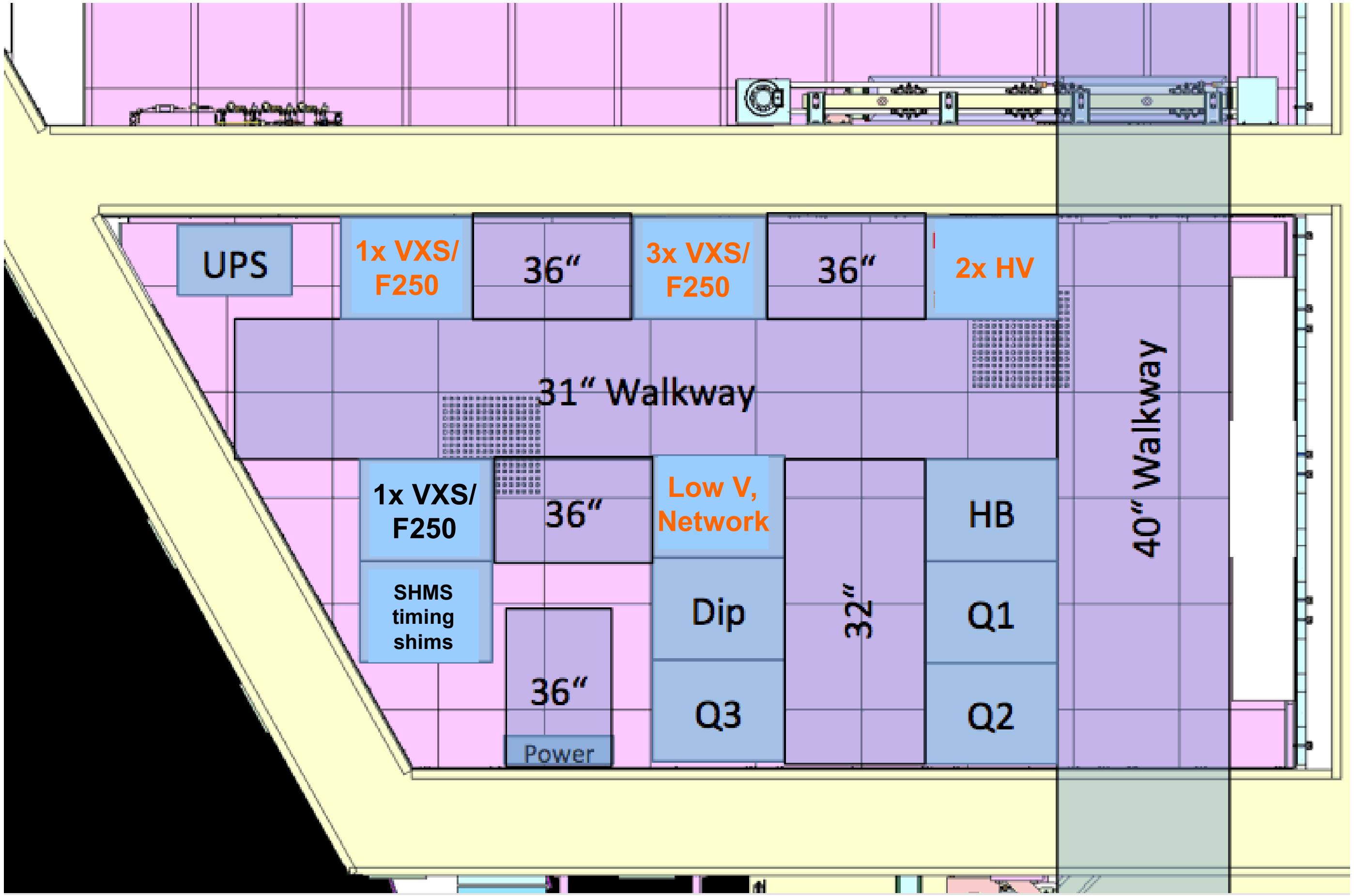
- **Still needed!**
  - → Energy / ADC / Timing:
    - » +51x FADCs (*)
    - » +2-3x VXS crates
    - » +5x SBC (+spare)
  - → FPGA NPS trigger
    - » +5x VTP (+ spare)
  - → Addl MTP fiber 'DAQ' trunk line SHMS ↔ CH (*if needed*)
  - → Upgrade network switches in SHMS and CH to 10 gigE (JLab CNI support)
- VXS Crates and support modules are in the Hall C purchase plan/schedule
- (*) F250s provided by Physics Division/ Fast Electronics group
  - → Pre-existing Lab inventory
  - → *Must ensure they are reserved for NPS installation+running*
    - » *Contention w/ SBS?*

Rackspace in SHMS hut

- 4+1 VXS crates + 2 High Voltage crates
  - → It's pretty snug, but it'll fit…
  - → Cables flow into crates via cable trays running above racks



NPS DAQ Challenges

- Most work driven by requirement to handle high-rate kinematics + waveform output
  - → 13 kHz HMS (DIS) triggers (+ background)
    - » need NPS trigger (→ VTP firmware)
    - » need 'Event-Blocking' enabled
  - → 'high' multiplicity in NPS (75+ crystals)
  - → waveform output for participating crystals is a 'Must' (~25 samples/ch)
- Pending issues
  - → VTP firmware development
    - » 3x3 crystal cluster triggers
    - » Emit logic-out for NIM trigger with HMS
    - » 'sparsify' F250 readout (only store waveforms from 5x5 clusters centered on 3x3 'trigger' cluster)
  - → Analyzer support for VTP payload
  - → Analyzer support for Event-Blocking mode
    - » 'Unblock' in secondary ROL?
      - – may be simplest? no analyzer changes needed [Moffit?]
    - » 'Unblock' at analyzer? [Bob M]

Updated (15 May 2019)

- Firmware questions *wrt* VTP/F250s
  - → Hall B firmware has compression, but removes features to achieve this
    - » need to ensure necessary timing, QDC, scaler(?) data still present
  - → May require upgrading HMS F250 firmware as well
    - » need to address knock-on changes to CRLs and analyzer assumptions for HMS
  - → *Or* lossless compression in 2nd stage ROL + libCoda mod?
    - » no F250 firmware change, no decoder changes
- Firmware / DAQ questions have been discussed with FE Group
  - → No "show-stoppers" but requires development resources be allocated to this project
- Updates to Hall C analyzer software
  - → Non-trivial work here!

VTP/F250/TM Firmware / Trigger

- VTP (5+1 modules attached to next FE order)
  - → Cluster trigger based on 3x3 groups, with 1 row shared between crates
  - → Logic signals emitted by each VTP will be OR'd in NIM to form NPS trigger
    - » CODA trig: HMS .AND. (.OR. of NPS)
    - » Timing latency on VTP triggers deterministic to <12ns
  - → Define/update VTP data payload
    - » cluster charge, timing?
    - » cluster crystal list to be used to sparsify F250 waveform readout
- F250 FADC (51 modules from FE/PD pool)
  - → Hi-res timing required (< 1ns)
    - » Preserve multi-hit/ch output
  - → QDC data, Scaler data
  - → Full waveforms (25 samples)
    - » Compressed?
  - → VTP info used to sparsify F250 readout channels to those in a 5x5 cluster(s) centered on the 3x3 'trigger' cluster(s)

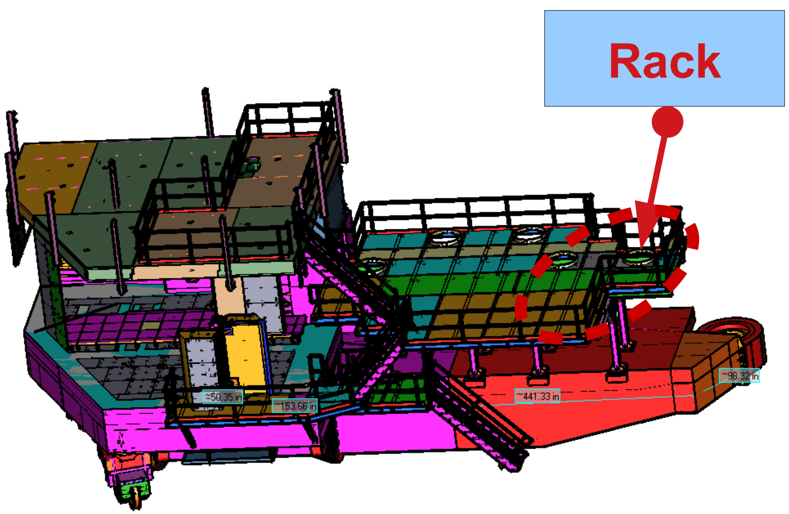
Updated (15 May 2019)

- TI/TM modifications
  - → must support 5 NPS crates + 3 HMS crates
    - » Modified layout with multiple TMs
  - → maintain six L1 trigger inputs on primary TM
- CODA assumptions
  - → Will need FE support for 'new' Vivo VME interface chip on Intel SBCs
    - » to be purchased for NPS crates
  - 'Standard HMS' NIM triggers will be available
    - » ¾, EL_{real}, EL_{clean}, ...
  - → NPS + HMS trigger made in NIM
    - » NPS + HMS {¾, EL_{foo}}
    - » NPS VTP latency is NOT a problem

FE development requests submitted to C. Cuevas for planning/approval

Signal/HV Cable Runs

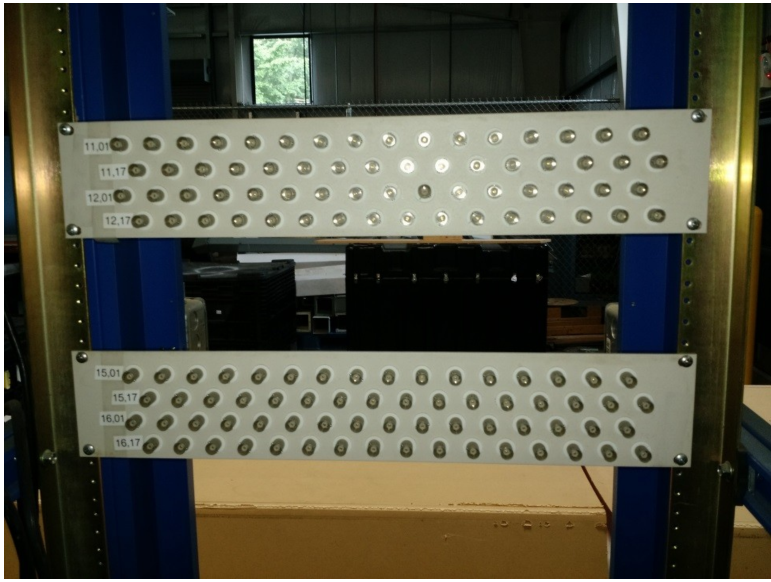
- Plan is for a single 84” tall, 19” standard width rack to be placed near the pivot
  - → Planned to go on the upper, power supply deck

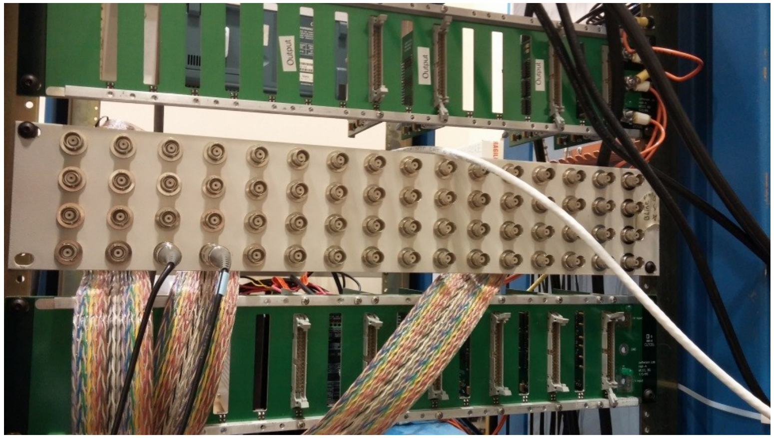


- The rack at the pivot will be “double sided”:
  - → One side will provide 1100 BNC connections
    - » BNC ↔ BNC feedthroughs
  - → Other side provides 30+2 high-density HV connections
    - » *Connector TBD*
      - – *$$/avail. issues*
    - » 36 ch/connector

BNC Patch Notes

- BNC patch panels must be 'high-density'
  - → Pre-existing layouts shown on right
  - → 64 isolated BNC feedthroughs per 3.5” tall panel
- 1100 RG-58 cables run from patch to five F250 VME/VXS crates in SHMS electronics hut
  - → BNC on patch panel
  - → LEMO in electronics hut
- Volume estimate for 1100 RG-58
  - → Penetration area
    - » 72 in^2 (min) + overhead
  - → Cable tray
    - » nominal 24” wide, 4–6” tall





HV / Slow Controls / Cabling Overview

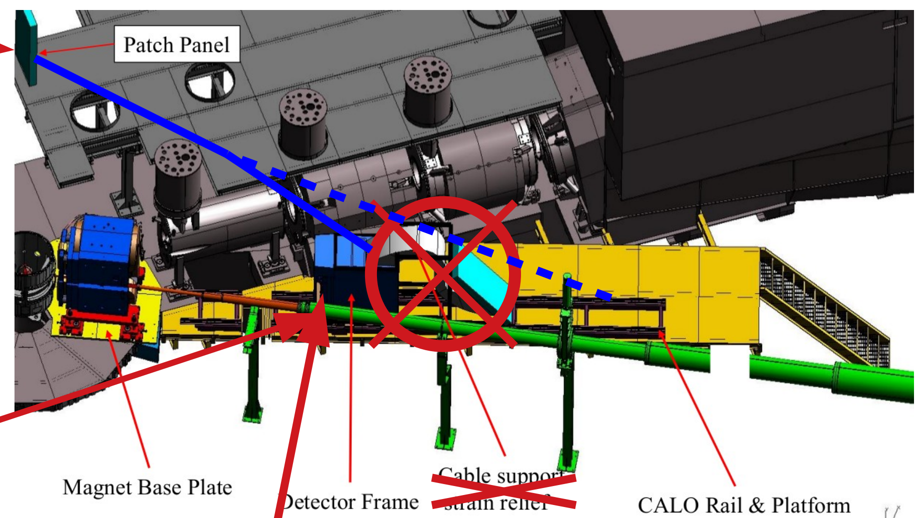
- High Voltage
  - → High Voltage (-1.6kV @ < 1 mA base draw)
    - » 30x CAEN 7030N Cards (36ch, 1mA max/ch)

- High Voltage Cables
  - → 2 cable runs:
    - » NPS roof patch → (~60-70 ' run) → Patch panel rack on SHMS carriage near pivot, and
    - » Patch panel rack → (~60-70' run) → SHMS detector hut (HV crates)

(Ignore the "Cable strain relief" concept below. It's being handled differently—*still in model though?*)

HV Crates inside Hut

Patch Panel Rack



NPS Detector on Beamline side

NPS detector can move on rails

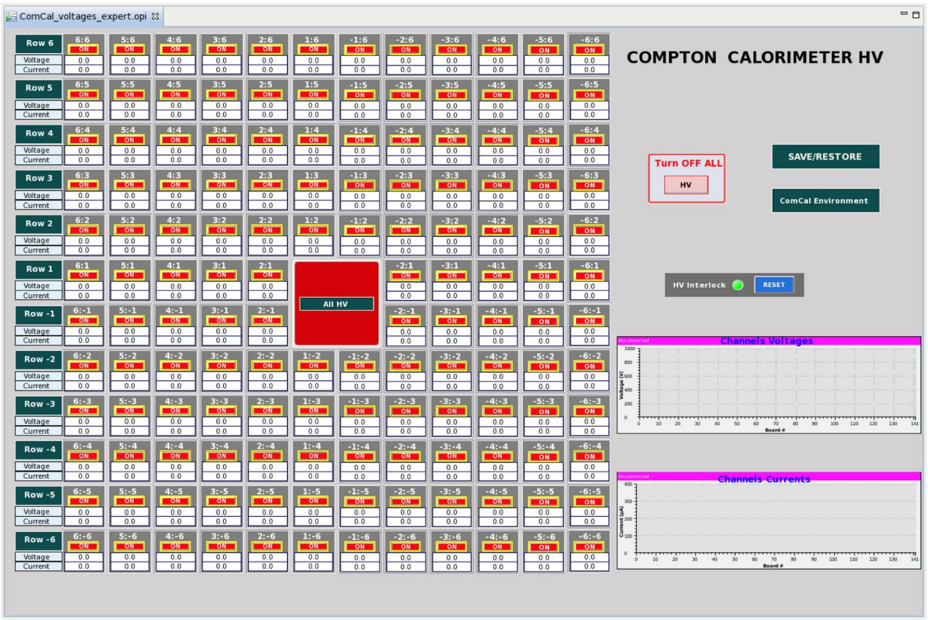
HV / Patch Panel / Cabling Summary

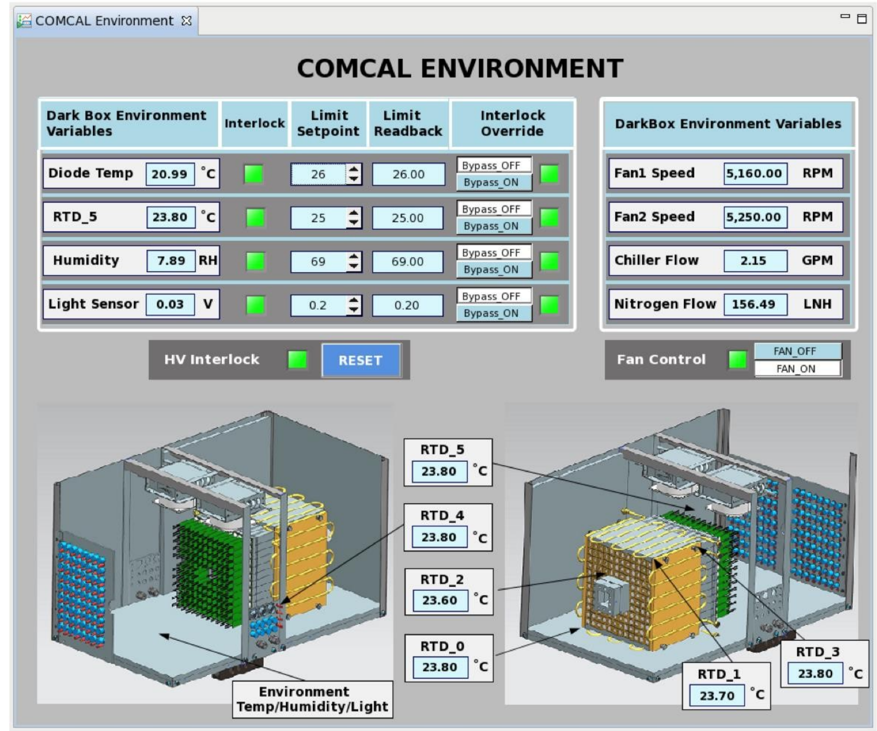
- High Voltage
  - → High Voltage (-1.6kV @ < 1 mA base draw)
    - » 30x CAEN 7030N Cards (36ch, 1mA max/ch)
    - » matches 36 crystal columns
  - → HV procurement complete
    - » Firmware debugging w/ CAEN underway, but no show stoppers
- HV Slow Controls
  - → HV monitoring and control already part of standard Hall C infrastructure, *but*
  - → Will likely roll into ComCal like screens (w/ DSG support)
- High Voltage Cables (2 sets) – TBP
  - → Multi-conductor cabling 48 ch/cable (NPS uses 36 ch/cable)
    - » NPS roof patch →
    - » Patch panel rack on SHMS carriage near pivot →
    - » SHMS detector hut (HV crates)
  - → *Work needed here!*
- Signal Cables (2 sets) – TBP
  - → RG58 / 50 Ohm
    - » NPS roof patch (LEMO) →
    - » Patch panel rack on SHMS carriage near pivot (BNC) →
    - » SHMS detector hut (LEMO)
      - – cables flow into crates from above via cable trays running above racks
- Cable run details (length) and costing in progress (Designers, A. Kenyon)

NPS Detector Slow Controls

- NPS detector will need additional instrumentation for **Thermal Monitoring/Control** and **LED system**
- Thermal Monitoring/Control
  - → Model after Primex/HyCal/ComCal
  - → Only local control needed
    - » Remote monitoring is straight forward
  - → Brad will be JLab point of contact for integration / EPICS
    - » DSG support required for ComCal-style GUI
- Existing EPICS Archiver and Alarm Handler software used for automatic signal logging/ monitoring
- Thermal Monitoring/Control Notes
  - → Rough Channel/Function List:
    - » Readbacks for chiller/air-handler at minimum
      - – Status, in/outflow temps, etc
  - → Internal air temp readback(s)
  - → Multiple detector temp readbacks (few dozen ch)
    - » Several locations in crystal mount / HV divider region
- LED controls (JLab FE Group)
  - → Controller design in progress...
    - » Custom control board
    - » Firmware development
  - → Spec documents delivered to FE group on Oct 2019
    - » Chris: Hall D DIRC LED pulser design may be good starting point

Extend Comcal (Hall D) Screens to NPS





- Prototype calorimeter installed in Hall D since mid-2018 is very similar to NPS.
  - → Existing control screens could be extended to provide front-end user interface for NPS
    - » DSG needed to take the lead on this (confirm)

Status/Schedule Summary

- Support hardware proc./staging
  - → Patch panel, NPS→DAQ cabling
    - » Design near complete, *procurement can begin anytime*
      (Joe, Andy, Jack, *DSG)*
  - → HV Crates
    - » Procurement complete
- Slow Controls
  - → LED Control (*DSG + FE Group*)
    - » Specs submitted to FE Group
      - – Confirmed w/ Chris C.
  - → "Integrated" NPS controls (*DSG*)
    - » ie. expand Comcal screens?
    - » Confirm/schedule with DSG!
- DAQ HW Procurement (Brad) (*Ongoing, complete by Fall 2020?*)
  - → Computer HW, Network upgrades are ongoing
  - → Single board computers (5+1)
  - → VTP boards (5+1)
  - → VXS crate purchases ongoing (2/5 in-hand, 3 to purchase)
  - → F250s available but *must*
    - » Reserve when dates known!
- DAQ Firmware/SW Devel. (*Should begin in 2020?*)
  - → 3.5 person-months (FE Group)
    - » Confirmed w/ Chris C.
- Analyzer (Hall C) mods
  - → *Should begin in 2020?*
  - → *Who (decoding + NPS specific)?*

“To Do”

Summary Slides

"Todo List" Summary (HW)

- **Remaining Procurements**
  - → Compute HW (Brad) (ongoing)
    - » Disk, 10 gigE, *DAQ MTP trunk fiber* (*TBD, few $k*)
  - → VXS crates (Brad) 3 $17k/ea
  - → Modules (Brad)
    - » VME computers 5+1 $5k/ea
    - » SD boards (Awaiting arrival)
      - – 4 SD boards ordered Aug '19
    - » VTP 5+1 $10k/ea
    - » F250s (Phys Div) (Need to 'reserve')
  - → Patch Panel hardware (Joe, Jack, DSG)
    - » HV cabling/connectors ($$$)
    - » BNC:LEMO cables
      - – coax purchased, connectors TBP ($$)

"Todo List" Summary (FW, SW)

- DAQ firmware development
  - *(FE/DAQ Group)*
  - →VTP firmware (clusters)
  - →F250 firmware (sparsified waveform readout)
  - →TI/TM firmware (to readout all NPS crates + HMS)
  - →CODA ROC driver dev. (Intel 'Vivo' VME interface)
- LED control system
  - *(FE/DAQ Group)*
  - →HW interface board
  - →Firmware control + SW
- Slow controls SW
  - →Comcal GUI → NPS
    - *(DSG, confirm!)*
    - » HV, temp displays
- Analyzer development
  - *("Hall C SW" + NPS)*
  - →Analyzer decoder
    - » multi-block decoding and potential related integration issues ('scaler' events, etc)
  - →High-level NPS class integration → hcana

Backup Slides

FE Group Work Commitment

Neutral Particle Spectrometer Experiment

DAq Hardware/Firmware Development Work Commitment

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2019-May-14 [Chris Cuevas]

Hardware: [B. Raydo, C. Cuevas]

- Manage procurement for five (5) new VXS crates and six (6) VXS Trigger Processor[VTP] modules

--> Includes time/resources for acceptance testing of new items

- Order and plan for installation of new MTP fiber optic trigger cable from the Hall C counting house to SHMS

- Locate and test at least fifty-one(51) Flash ADC-250 modules from the Fast Electronics/Physics 'pool'

--> Includes time/resources for testing

- TI/TM modifications

--> William Gu has reviewed the requirements for the NPS DAq crate configuration and has a plan to support the 5 new VXS crates for the NPS calorimeter plus the 3 HMS crates.

--> This work includes modifications to support multiple Trigger Interface "Masters"

Firmware/Simulation/Verification [B. Raydo, H. Dong, Ed J., W. Gu]

- 5 x 5 cluster based trigger development for VTPs

--> Significant development has been completed for the Heavy Photon Search experiment, so large portion of firmware can be re-used

--> Test and verify that the proper logic levels and timing latency meet the requirements to be combined with the HMS NIM trigger

--> Develop new firmware to create a sparsification list that will be sent from the VTP switch slot to the FADC250 [payload slots] The sparsification firmware is new, but the hardware path exists on VXS back-plane from the VTP to the FADC250 boards

-- FADC250 firmware [H. Dong, Ed J., B. Raydo]

--> The good news is that the firmware exists for modes that the NPS experiment requires

--> Features of High Resolution timing, QDC and scaler data, and raw waveform sample mode (25 samples == 100ns) exist, plus firmware to compress the readout data has been tested/used on other experiments.

--> Merging existing firmware from other experiments and functional verification/testing will be the significant activities for the FADC250 development.

Procurement support:

- VXS crates [Estimate $13K/Crate] - Long lead item ~12weeks/After Receipt of Order

- VTP modules [Estimate $8700/Module] - Long lead item ~10weeks/ARO

- MTP Fiber Optic trunk line + Installation: $4500 - 4 week delivery ARO

Resource commitment:

- After significant discussions with Ben Raydo, Hai Dong, Ed Jastrzembski and William Gu I estimate that 3.5 man-months will be needed to complete the activities listed. Keep in mind that this time allocation may indeed be integrated over several months, but there are significant sections of new firmware that will need to be tested well in advance of the experiment installation period. If the experiment begins in 2020-Sept, then this development work must be started as early as spring 2020.

- Long lead hardware procurement should be started as soon as funds are allocated in FY2020. This will allow for vendor fabrication time and acceptance testing.

Some details updated since May 14, 2019
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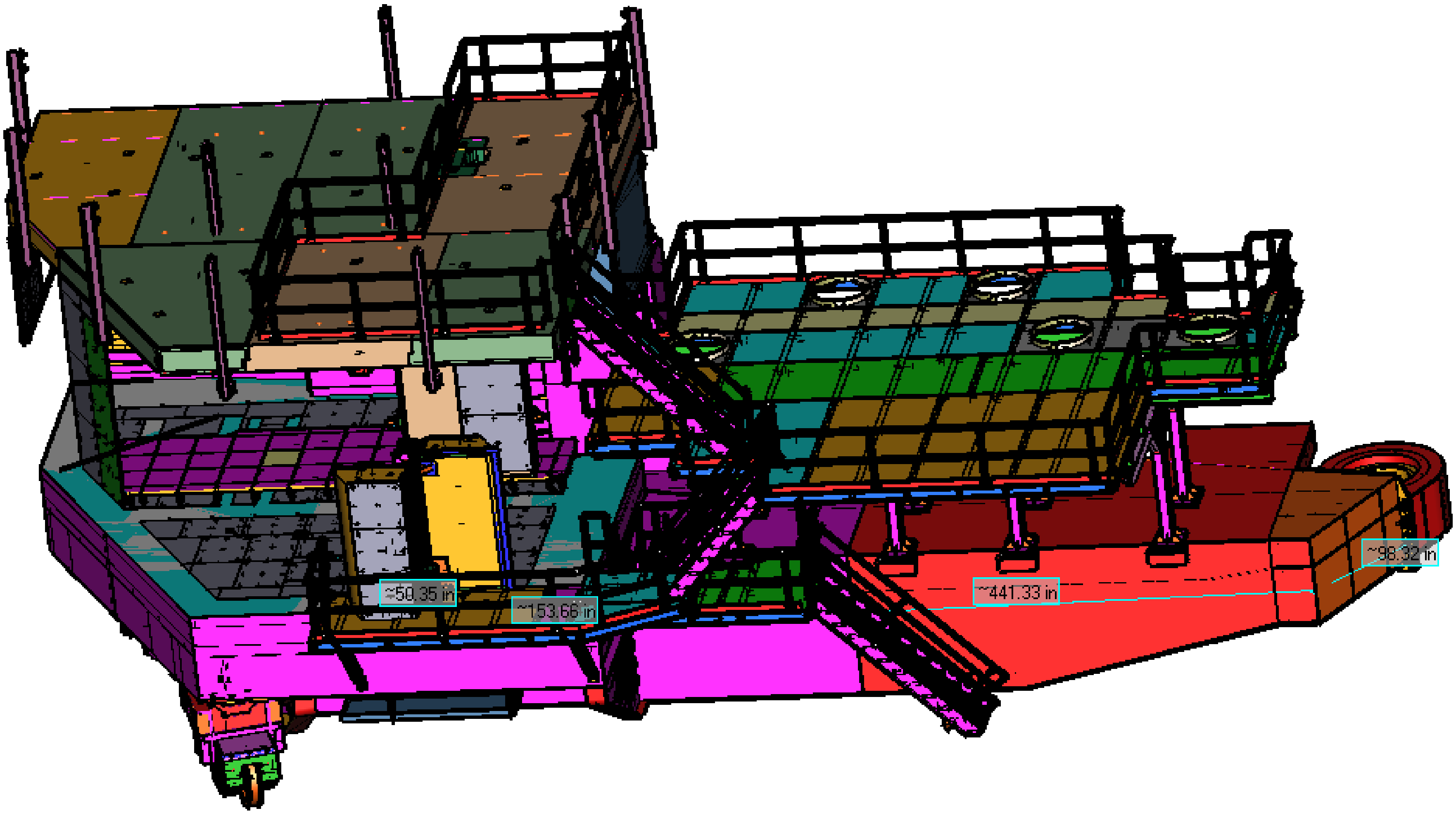
SHMS Carriage w/ Distance Annot.



NPS High Voltage Supply

- High Voltage Requirements
  - → 1100 channels
  - → -1.6kV @ < 1 mA base draw

- Supplied by 2 CAEN SY4527 HV Chasses w/ Booster
  - →16x CAEN 7030TN Cards each
    - » Each card: 36ch, 1mA max/ch (matches 36 crystal columns)
  - →576 ch/crate; 1152 ch total
- HV procurement complete
  - →2 Crates + 34 cards on-site
  - →DSG working with CAEN on firmware issues since Fall '19

HV Patch Notes

- HV patch panel will accept a 'Radiall 52' male connector
  - → The connector has common ground for 48 independent channels (of which we use 36)
  - → The connector ground must be isolated from the rack
- Other end will plug into CAEN 7030 cards
  - → Connector map follows CAEN pinout as shown on left (from CAEN 7030 manual)
- Cables 'reversible' and reusable
- Multi-conductor cable identified
  - → Teledyne Reynolds in Torrance, CA.
    - » Part# 178-5790
- HV patch panel components TBP

https://www.datasheets360.com/pdf/8778225758601965736

https://www.caen.it/products/a996/

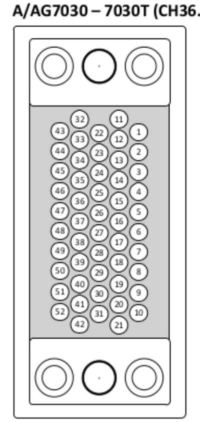
https://userweb.jlab.org/~brads/Manuals/Hardware/CAEN/A730_HV_Boards-Apr2016.pdf

CAEN Electronic Instrumentation

Multipin connector pin assignment

Table 2 – 52 pin connector assignment

A/AG7030 – 7030T (CH36..47 N.C. on A7030T & AG7030T)



#	function	#	function	#	function	#	function	#	function
1	CH02	11	RETURN	22	CH01	32	RETURN	43	CH00
2	CH07	12	CH04	23	CH06	33	CH03	44	CH05
3	CH12	13	CH09	24	CH11	34	CH08	45	CH10
4	CH17	14	CH14	25	CH16	35	CH13	46	CH15
5	CH22	15	CH19	26	CH21	36	CH18	47	CH20
6	CH27	16	CH24	27	CH26	37	CH23	48	CH25
7	CH32	17	CH29	28	CH31	38	CH28	49	CH30
8	CH37	18	CH34	29	CH36	39	CH33	50	CH35
9	CH42	19	CH39	30	CH41	40	CH38	51	CH40
10	CH47	20	CH44	31	CH46	41	CH43	52	CH45
		21	RETURN			42	SAFETY LOOP		

Radiall HV Connector

HIGH VOLTAGE MULTIPIN CONNECTORS

- High voltage connectors (breakdown voltage 12,5 kVdc).
- High density rectangular connectors for 23 or 52 high voltage contacts.
- Braid to braid electrical continuity achieved once plug & receptacle are mated.
- Rear release, rear removable size 23 crimp contacts.
- Interlock contacts.

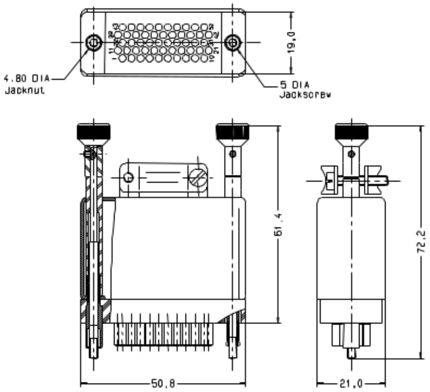
These connectors have been designed for high voltage applications on four CERN experiments (ATLAS, CMS, ALICE, LHC-B) of the LHC (Large Hadron Collider) particle accelerator. For connectors with 23 or 52 contacts (size 23 crimp), there are five configurations available (see table on reverse side). The connectors can be fitted with two interlock pin contacts that switch off the power supply before unmating the standard contacts . Both interlock and standard contacts are rear release rear removable crimp contacts. The electrical continuity between the plug and the receptacle is provided by the connector pin guides.

TECHNICAL CHARACTERISTICS :

- Material insulator : Thermoplastic UL94V0 - halogen free - tensile strenght reduction does not exceed 6% after a cumulative exposition to 5 10^{5}Gy at a rate of 1 to 2 Gy / h.
- Backshell & shroud : Aluminium alloy nickel plated.
- Locking device : Stainless steel and nickel plated copper alloy.
- Contacts : Copper alloy gold over nickel plated.
- Breakdown voltage : 12,5 kV dc.

ISO 9001 APPROVED

DIMENSIONS :
The drawing below shows the dimensions (mm) of the plug for cable and for 52 socket contacts.



CERN / RADIALL CROSS REFERENCES :

CERN P/N	RADIALL P/N	Designation
09.41.34.700.2	691802002	Plug for cable and for 52 socket contacts
09.41.34.720.8	691802004	Plug for cable and for 52 pin contacts
09.41.34.705.7	691803002	Receptacle for cable and for 52 pin contacts
09.41.34.710.0	691803004	Receptacle for front panel and for 52 pin contacts
09.41.34.730.6	691803006	Receptacle for front panel and for 52 socket contacts
09.41.34.500.8	691802003	Plug for cable and for 23 socket contacts
09.41.34.520.4	691802005	Plug for cable and for 23 pin contacts
09.41.34.505.3	691803003	Receptacle for cable and for 23 pin contacts
09.41.34.510.6	691803005	Receptacle for front panel and for 23 pin contacts
09.41.34.530.2	691803007	Receptacle for front panel and for 23 socket contacts
09.41.33.840.5	691804200	Size 23 pin contact for 0,12mm² cross section cable
09.41.33.820.9	691804201	Size 23 pin contact for 0,02mm² cross section cable
09.41.33.830.7	691804300	Size 23 socket contact for 0,12mm² cross section cable
09.41.33.810.1	691804301	Size 23 socket contact for 0,02mm² cross section cable
09.41.33.890.5	691804230	Size 23 interlock pin contact for 0,12mm² cross section cable
09.41.33.880.7	691804231	Size 23 interlock pin contact for 0,02mm² cross section cable
T.B.D	282281	Crimping tool
T.B.D	282585001	Positioner
T.B.D	282549024	Insertion / extraction tool

For further information please contact your nearest Radiall representative :

radiall.com

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RADIALL Elettronica S.R.L. (Italy)	+39 2 48 85 121	NIHON RADIALL KK (Japan)	+81 3 3866 2390
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This information is intended as a guide only. To ensure a continuing policy of product improvement, Radiall reserves the right to modify its specifications without prior notification.

https://www.datasheets360.com/pdf/8778225758601965736
https://www.caen.it/products/a996/

Multiconductor HV Cable

- Multiconductor cable recommendation
  - →Teledyne Reynolds
    - – Part# 178-5790
      - » Ph: (310) 823.5491
      - » Em: tr_sales@teledyne.com
  - →Used by CERN, CAEN

FEP
FEATURES AND PROPERTIES

Heritage
Quality
Performance

Extruded, FEP insulated, high voltage wire and cable offers exceptional dielectric strength without the disadvantages common to equally rated silicone rubber insulated cables. As a result, cable assemblies or cable bundles are smaller in diameter, volume and in bend radius thus allowing the system designer to better utilize space within their system. Also, its molecular structure gives it excellent durability and resistance to dielectric/cooling fluid degradation.

FEP insulation, being a harder material than silicone rubber, is not prone to "pin-holing" and high voltage "punch-thru" when the cable surface is abraded or when strands break during in-field servicing. FEP is also more resistant to damage when making contact with sharp edges. Even so, sharp edges should always be avoided.

Although FEP is generally difficult to bond to, Teledyne Reynolds, has developed a Ready-to-Bond™ product line that is manufactured using proprietary abrading and surface preparation techniques that enable excellent silastic bonds. Teflon® tape wrapped cable, which is similar to FEP in dielectric strength and corona inception, is difficult to bond to because of its multiple spiral cross section, irregular surface and variations in diameter. Therefore, FEP cable should not only be considered for use in cable assemblies, but as high voltage hook-up wire within encapsulated high voltage power supplies, TWTs and transformers.

PROPERTIES OF FEP FLUOROCARBON RESIN

Physical, Thermal and Electrical Properties	Typical Values
Specific Gravity	2.14
Tensile Strength (PSI)	3500
Elongation (%)	.325
Flexual Modules (PSI)	90,000
Thermal Conductivity (cal/sec-cm °F)	$6x10^{-4}$
Thermal Expansion (in/in/ °F)	$7.5 x 10^{-5}$
Continuous Use Temperature (°C)	204
Melt Temperature (°C)	255-265
Low Temperature Limit (°C)	-240
Hardness Durometer	D56
Water Absorption (%)	<01
Flame Resistance	Excellent
Dieletric Constant, $60\text{-}10^6$ Hz	2.1
Dissipation Factor, $60\text{-}10^6$ Hz	<.0007
Volume Resistivity (Ohms-cm)	$<10^{18}$
Surface Resistivity (Ohm/square)	$<10^{16}$
Resistance to:	Rating
Cold Flow or Cut Through	Fair
Ultraviolet Radiation	Excellent
Electro-Mechanical Stress Cracking	Excellent
Chemical-Mechanical Stress Cracking	Excellent

Conductor Material: Copper

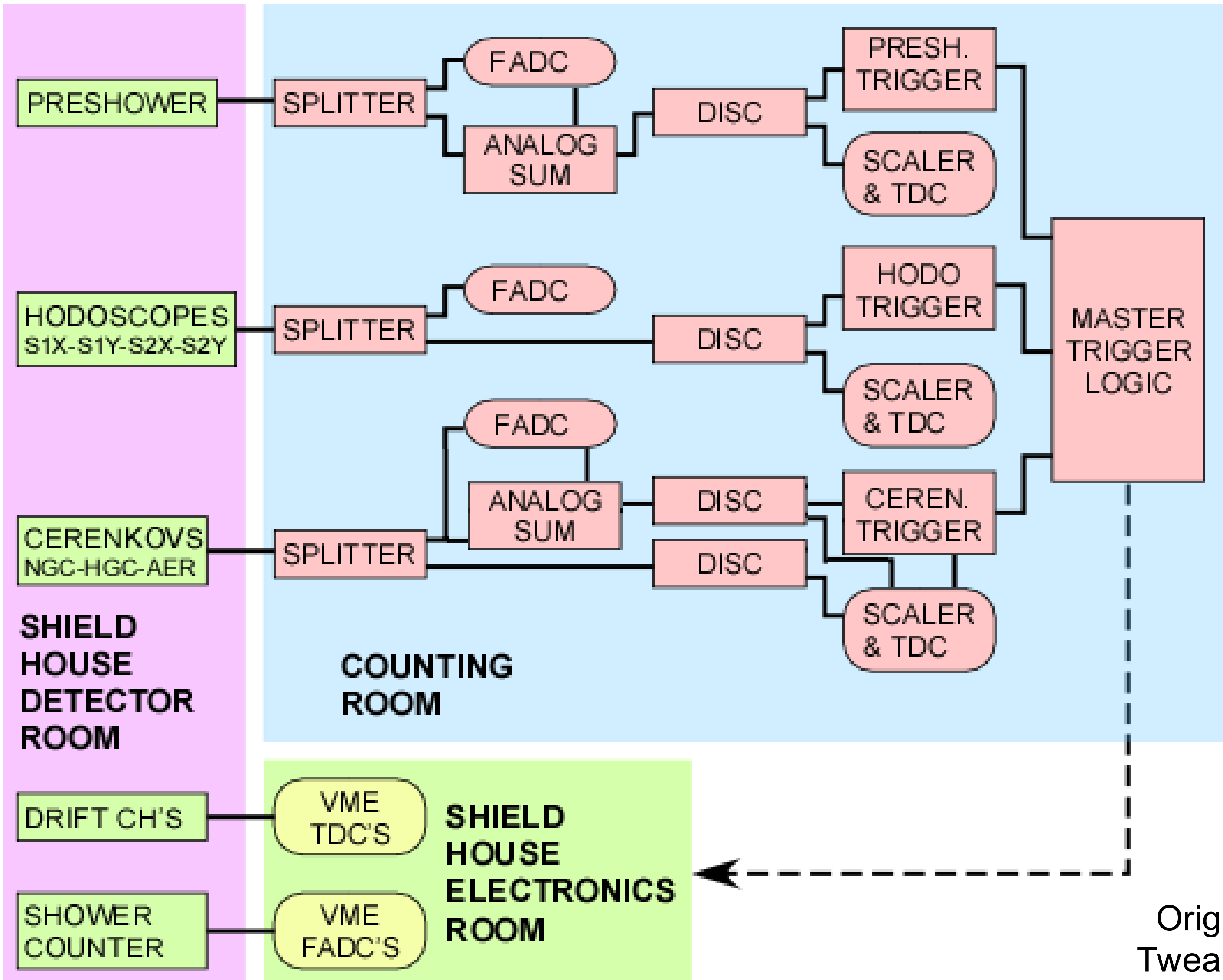
Conductor Finish: Silver plated per test requirements of ASTM B298. Meets solderability per MIL-STD-202.

Note: Pre-conditioning of FEP cable after cutting to length is recommended because FEP cable will shrink when exposed to temperature cycling. Pre-conditioning should be conducted in an air circulating oven at 204°C (400°F) for one hour. No attempt should be made to condition wire or cable in bulk form or while spooled.

Approved for Public Release: MP/022/15
Rev. 092515
TELEDYNE REYNOLDS
Everywhereyoulook™

Existing SHMS + HMS Standard DAQ Triggers and Hardware

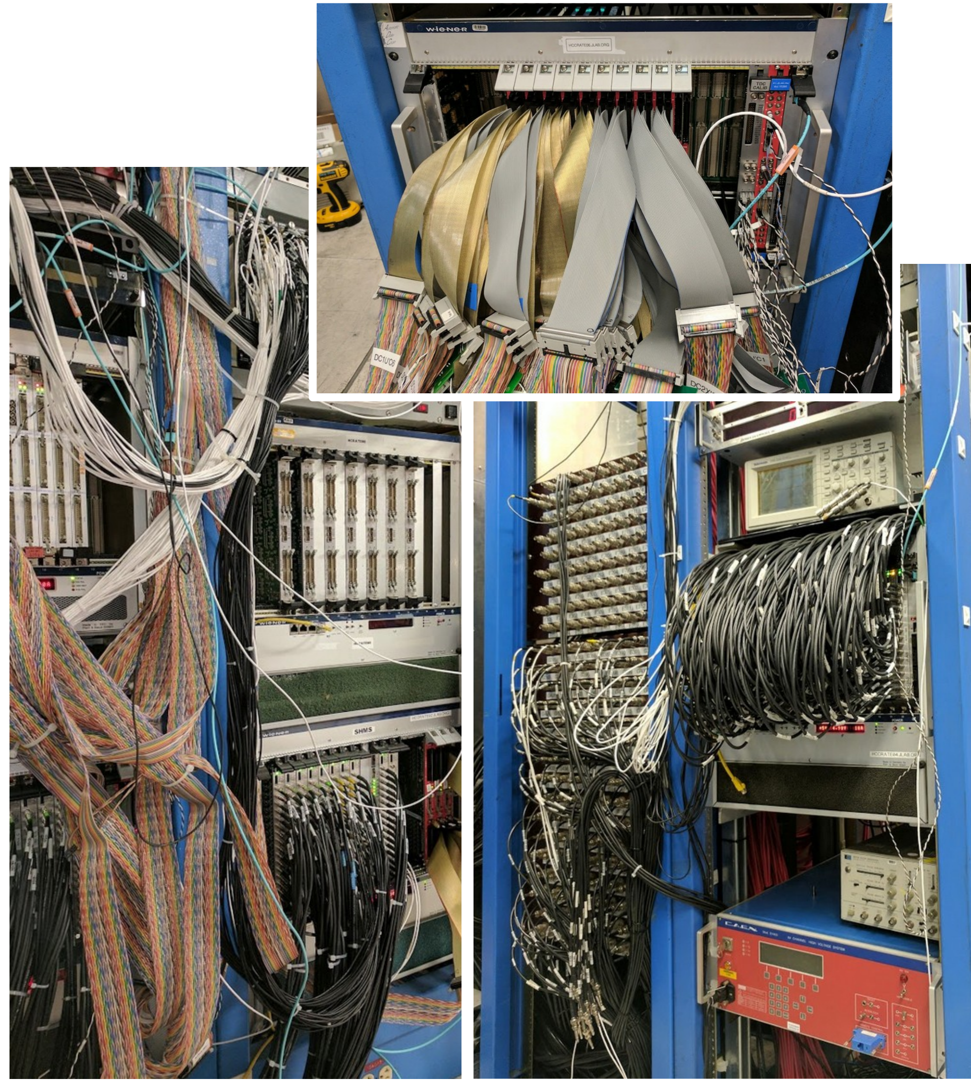
SHMS/HMS Trigger/Electronics



Orig by H. Fenker
Tweaked by Brad S.

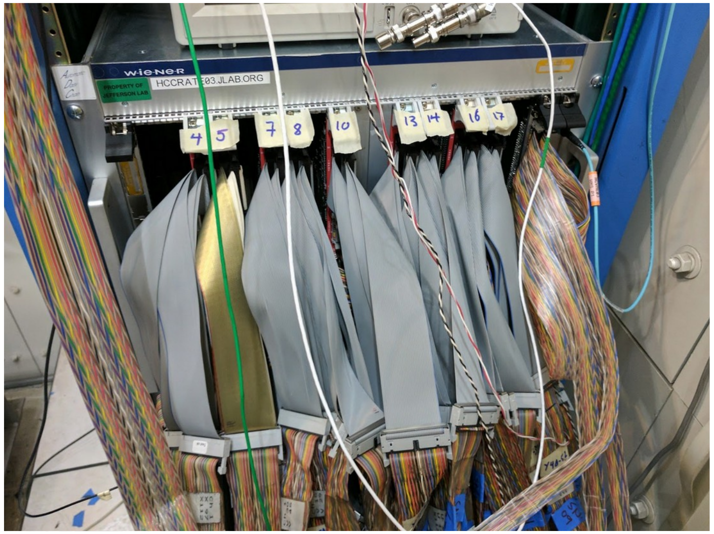
SHMS Instrumentation

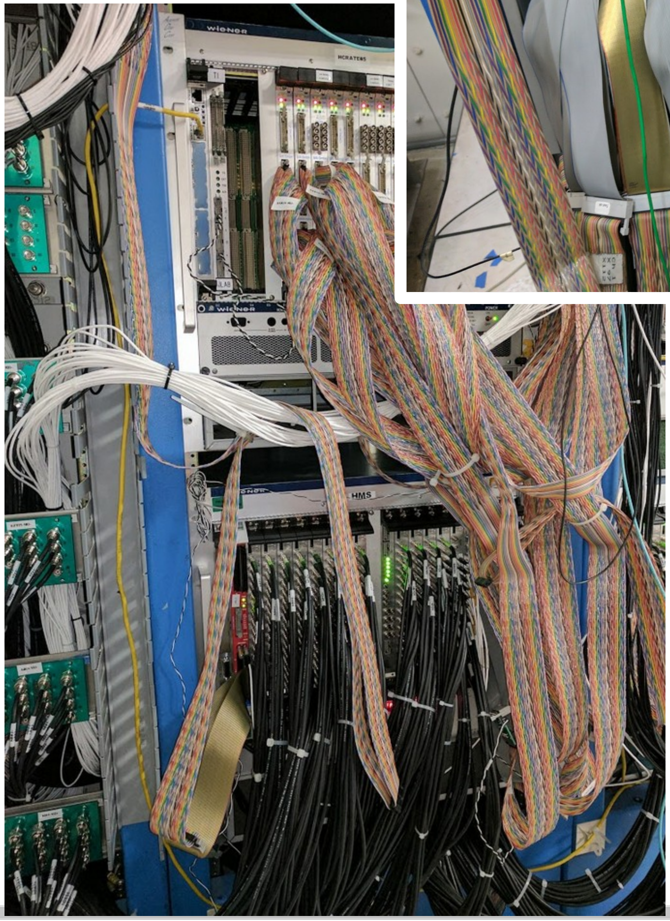
- **SHMS**
  - → ROC2: CH
    - » Hodoscopes, Cerenk.
      - – FADC + 1190s
    - » Misc. Signals
      - – *ie*. Triggers, Hel
  - → ROC4: SHMS hut
    - » Shower + Preshower
      - – FADCs
  - → ROC6: SHMS hut
    - » Drift chambers
      - – 1190 TDCs
  - → ROC8: CH
    - » Hardware scalers
    - » BCMs, Helicity gated scalers



HMS Instrumentation

- **HMS**
  - → ROC1: CH
    - » Calor, Hodoscopes, Cerenk.
      - – FADC + 1190s
    - » Misc. Signals
      - – *ie*. Triggers, Hel
  - → ROC3: HMS hut
    - » Drift chambers
      - – 1190 TDCs
  - → ROC5: CH
    - » Hardware scalers
    - » BCMs, Helicity gated scalers

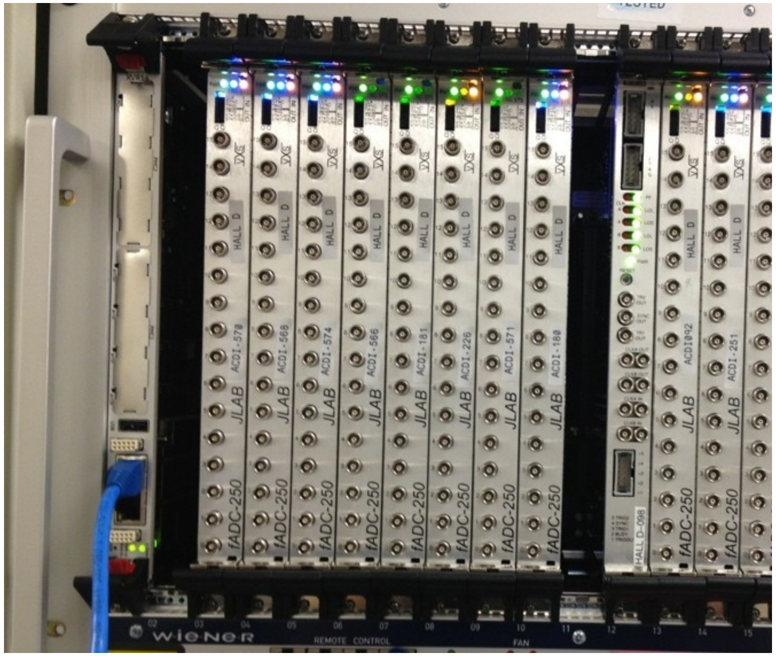




JLab F250 FADCs

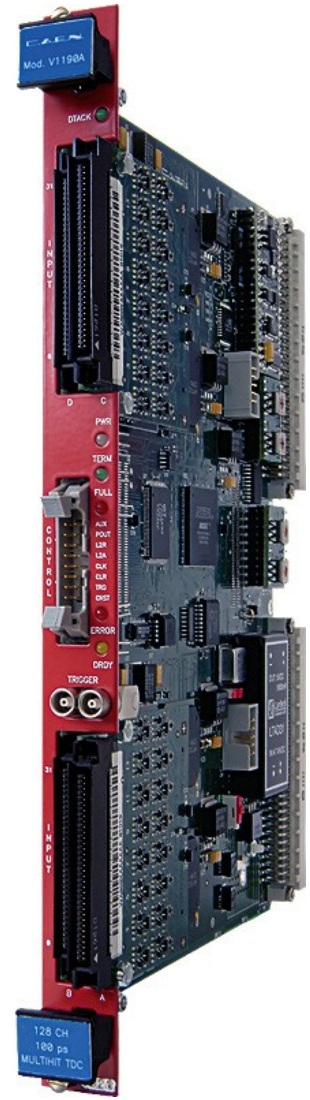
- JLab FADCs
  - → Constantly digitizing input voltage every 4ns
  - → Multi-hit 'ADC'!
    - » Can readout anything within an ~8 usec ring buffer
  - → Each 'Hit' contains
    - » Integrated charge
    - » Peak Amplitude
    - » Timing (~ 1 ns)
    - » Pedestal meas.
    - » Pulse profile / 'Scope trace' (*)
  - → Scaler data too
  - → Pipeline capable, deep buffer, etc..

- Differences from older QDCs
  - → Multi-hit!
    - » Must identify the 'good' hit using, for example, a timing cut

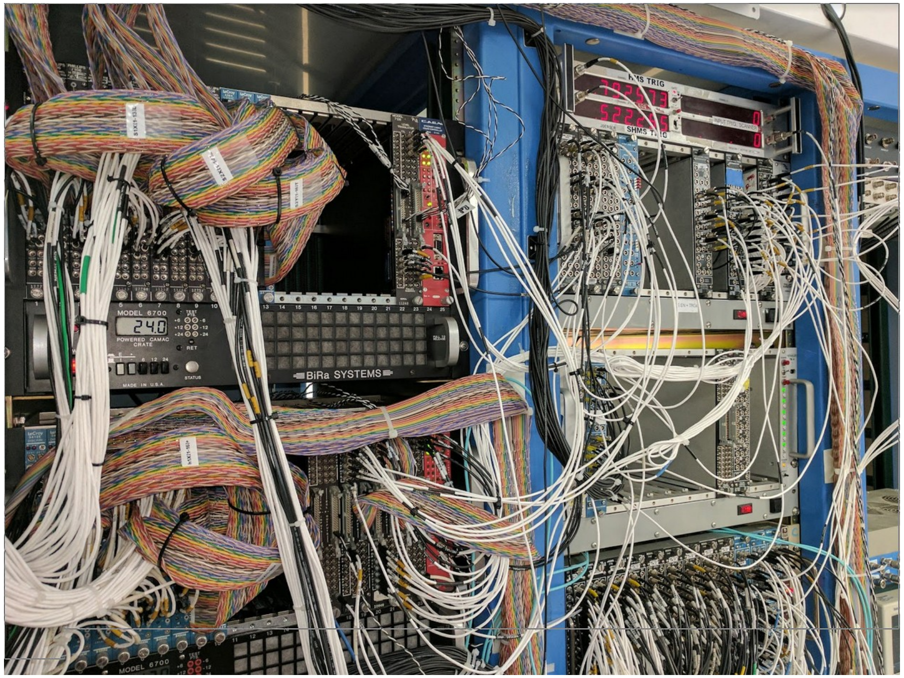


CAEN 1190 TDCs

- CAEN 1190
  - → Multi-hit TDC
  - → 128 channels/module
  - → ~100 ps resolution
  - → Pipeline capable, deep buffer, etc...
- Differences from older TDCs:
  - →Module's “Common Stop” is not a good timing reference!
    - » Primary function is to initiate a “Read” in the module.
  - →Requires a “reference time” to measured in one of the 128 inputs



Available SHMS / HMS Pre-Triggers



- Scintillator Planes: S1x, S1y, S2x, S2y
- SCIN = 3/4 { S1x, S1y, S2x, S2y }
- CER = Cerenkov Sum
- STOF = [S1x.OR.S1y] .and. [S2x .OR. S2y]

- PSh_Hi = Preshower sum, 'high-threshold'
- PSh_Lo = Preshower sum, 'low-threshold'

- EL-Hi = SCIN .and. PSh_Hi
- EL-Lo = 2/3{SCIN, STOF,PSh_Lo} .and. CER

- EL-Real = EL-Hi .or. EL-Lo
- EL-Clean = EL-Hi .and. EL-Lo

- Pulser/Random trigger
  - → EDTM injection for deadtime monitoring, trigger setup, etc
  - → EDTM should always be ON and set to nominal 10 Hz
- Each arm has its own Trigger Master (behaves like a TS)
  - → Maximum of 6 trigger inputs on Trigger Master modules
  - → Both coincidence and independent/parallel-arm operation available
- We use TM module for trigger prescaling
- NOTE: There is *no* Calorimeter Sum for SHMS trigger
  - → SHMS Pre-Shower sum *does* exist

Coincidence Mode Triggers

- SHMS Trigger Master controls all SHMS + HMS crates in 'Coin. Mode'
  - → Still a single TM, so still maximum of 6 triggers for SHMS_singles + HMS_singles + and Coin. triggers
  - → For example, these are the current triggers:
    - » T1: SHMS 3/4
    - » T2: SHMS EL_real
    - » T3: HMS EL_real
    - » T4: HMS 3/4
    - » T5: (COIN) SHMS 3/4 .AND. HMS EL_real
    - » T6: (COIN) SHMS 3/4 .AND. HMS 3/4