DSG NPS Collaborator's Meeting Update

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10/29/2020

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- Cable Fabrication/Procurement
- CAEN HV Module Testing
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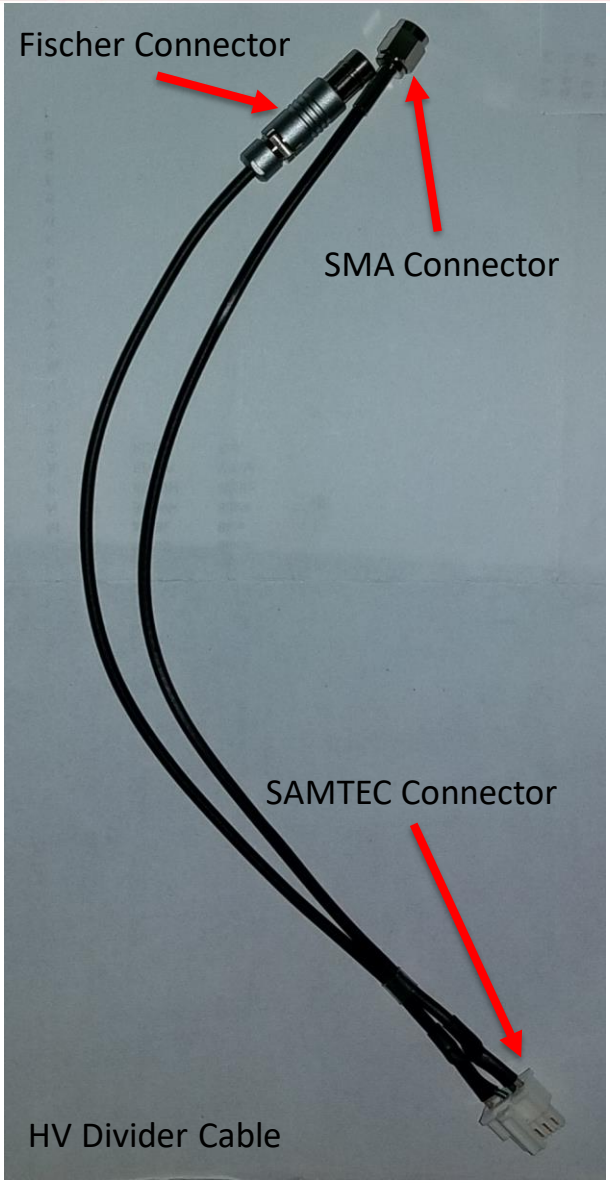
Cable Fabrication/Procurement

- HV divider cable status
  - 950 of 1100 fabricated (86% completed)
- 142’ HV cables
  - 42 cables ordered on 09/28/2020
  - ETA: December 2020
  - Status: Unchanged
- SAMTEC connectors (IPBD-15-D-K)
  - 100 8-pin and 50 15-pin ordered on 09/17/2020
  - ETA: November 2020
  - Status: Unchanged
- Radiall Connectors
  - 40 connectors ordered on 08/26/2020
  - ETA: November 2020
  - Status: Unchanged



CAEN HV Module Testing

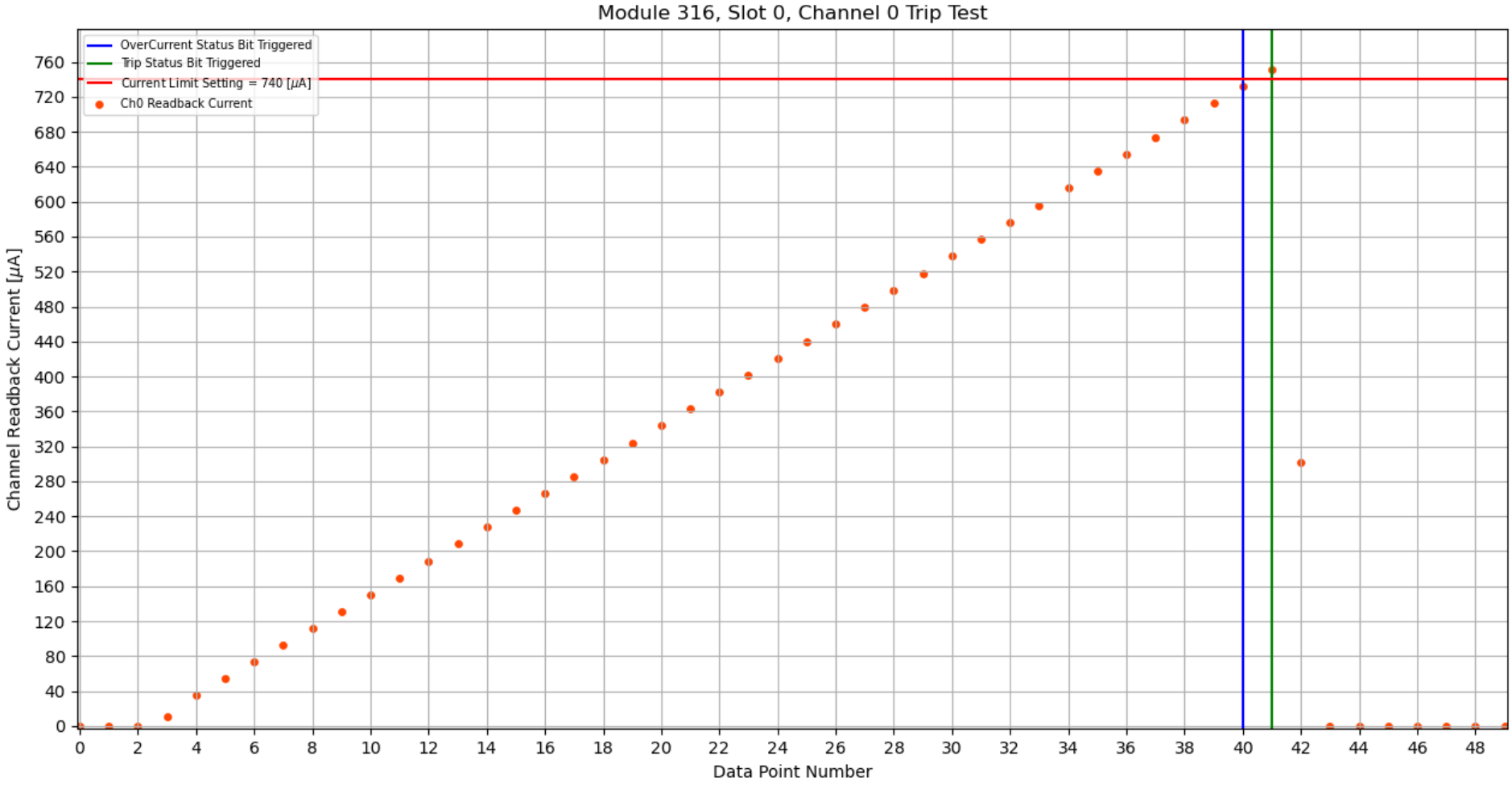
- All stability and current trip testing completed
  - Voltage and current stability analysis plots have been uploaded to the NPS section of the DSG technical documentation website
- EPICS software for ramp testing completed
  - Starting ramp tests

```
for (var jboardch=0; jboardch<boardch.length; jboardch++)
{
pv = prefix + boardch[jboardch] + ":" + "V0Set";
PVUtil.writePV(pv,1500);
wait(40000);
PVUtil.writePV(pv,0);
wait(40000);
```

Code snippet for EPICS-based ramp test

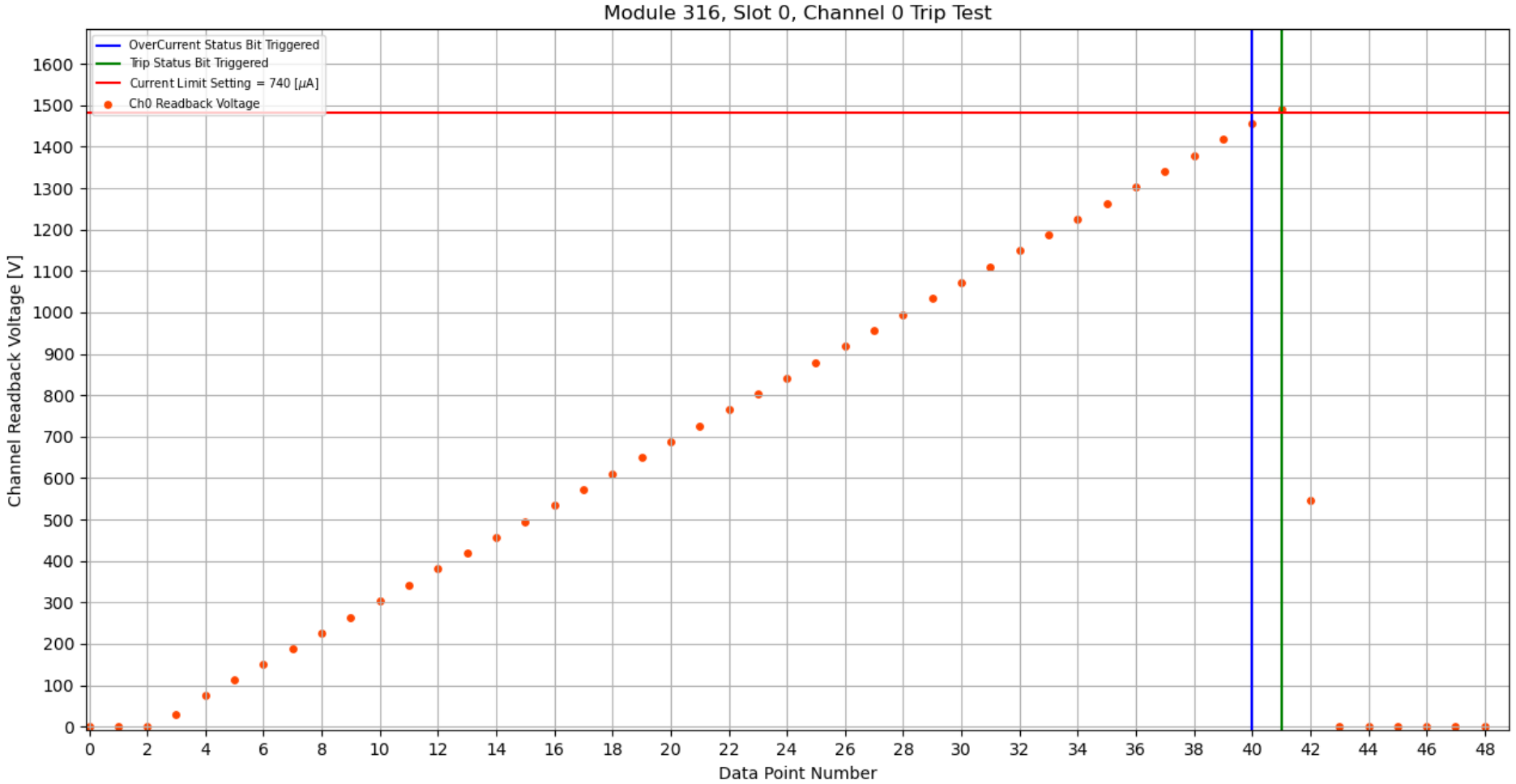
CAEN HV Trip Testing

- Current limit set to 740 µA
- Time over threshold set to 1 s
- Ramp rate set to 50 V/s



CAEN HV Trip Testing

- Voltage ramped to 1500 V
- Ramp rate set to 50 V/s
- Time over threshold set to 1 s



CSS-BOY Screens Development

- Scheme 2 has been selected as the numbering scheme for PMT position and crystal numbers
- PMTs are numbered as viewed from rear of detector (PMT side)
- PMT Settings screen and main NPS screen being redone to reflect new scheme

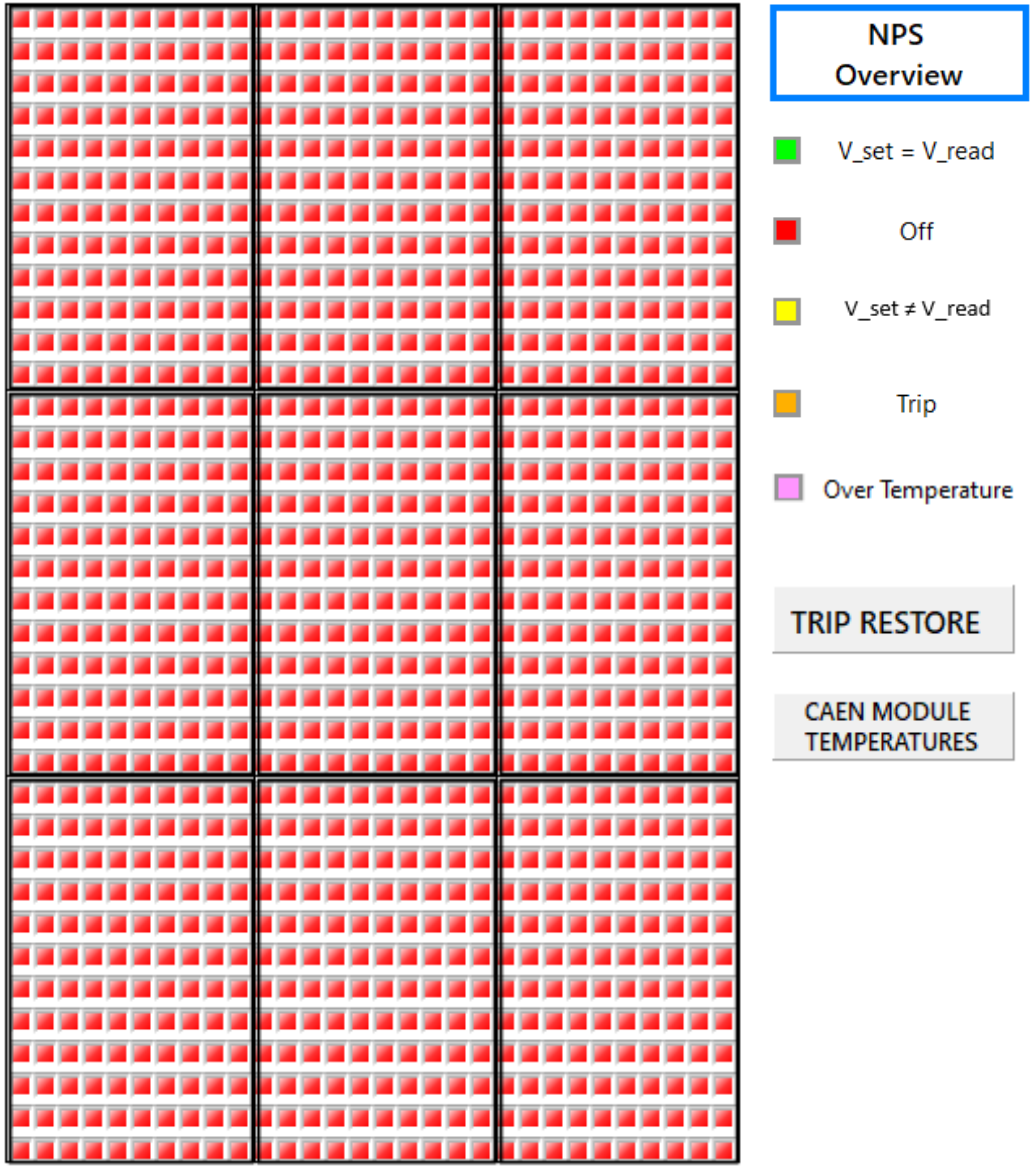
00:35	01:35	02:35	.	.	.	**29:35**
.	.	.				.
.	.	.				.
.	.	.				.
00:02	01:02	02:02	.	.	.	29:02
00:01	01:01	01:01	.	.	.	29:01
00:00	01:00	02:00	.	.	.	**29:00**

mm:nn ⇔ slot#:ch # ⇔pmt col # : pmt pos # (in column)

PMT pos # $\vee$ Crystal # = n x 36 + m; $n \in [0,29] \wedge m \in [0,35]$

where n is slot number and m is channel number

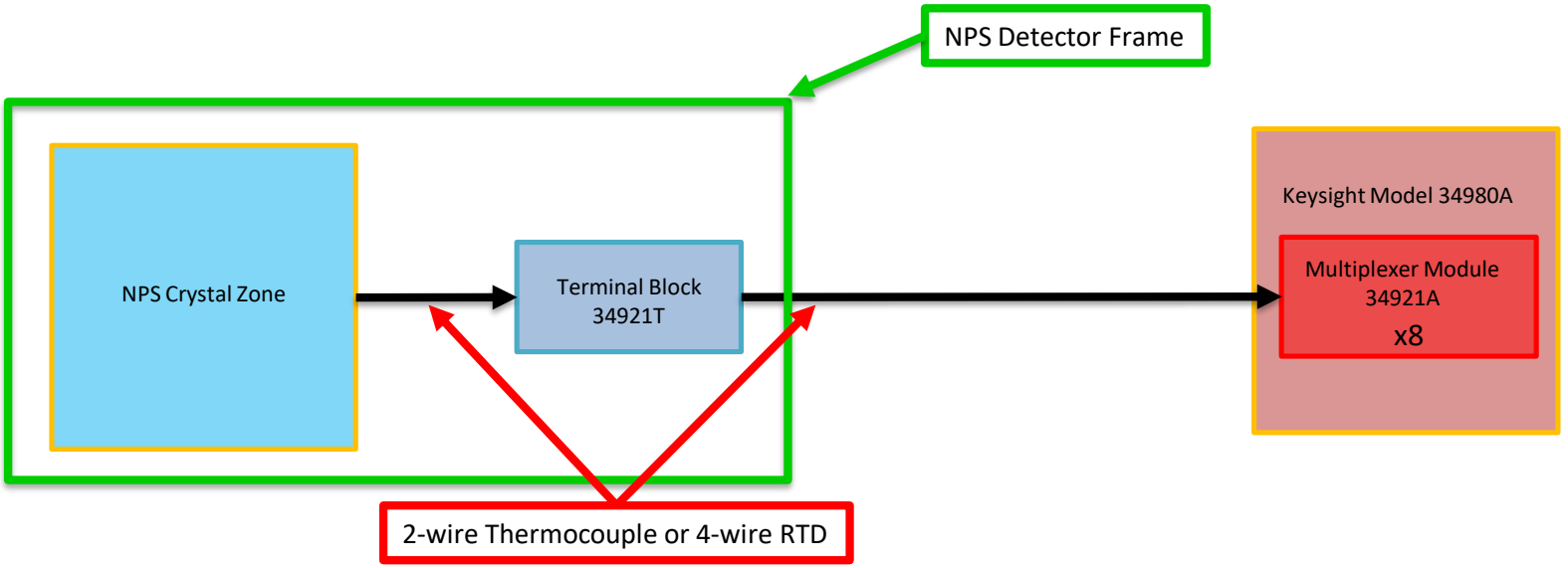
CSS-BOY Screens Development



- Overview screen with LED indicators for each PMT/channel
  - Green: $V_{set} = V_{read} \pm 10$ V
  - Red: PMT/channel is OFF
  - Yellow: $|V_{read} - V_{set}| > 10$ V
  - Orange: Trip (OFF)
  - Pink: module temp. > 65°C

Interlock System

- Researching temperature scanning systems for crystal array and electronics zone
- A Keysight 34980A mainframe can accommodate up to 160 4-wire RTDs or 320 2-wire thermocouples
- Available modules can measure AC/DC voltage, resistance, frequency, current, and period



Conclusions

DSG is making good progress in all areas

Thank You