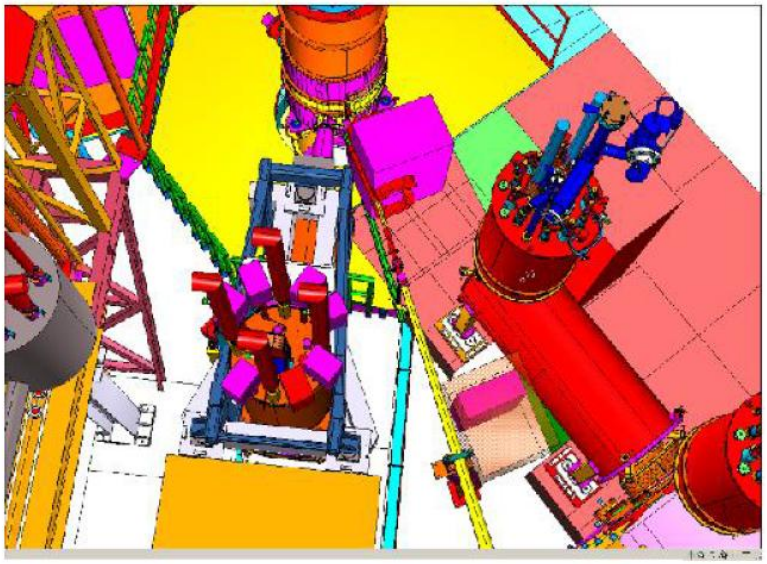
# NPS FADC and Trigger test plan

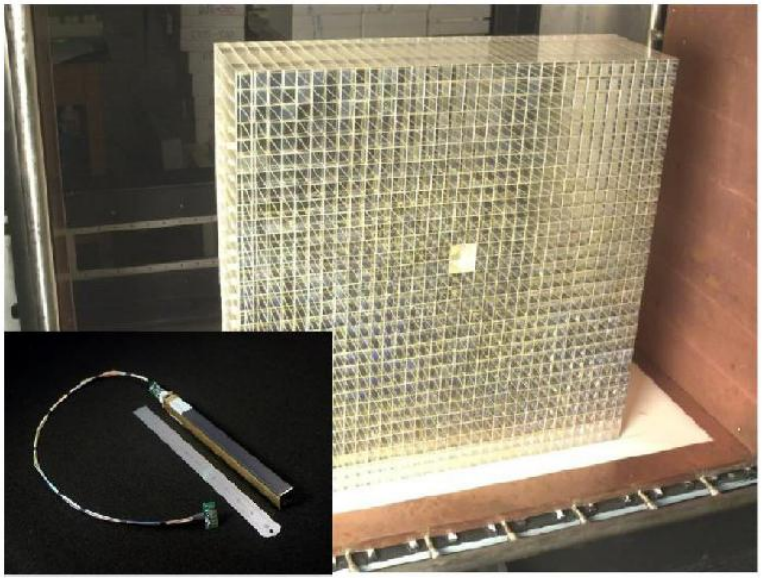
# Outline

- NPS calorimeter
- JLAB pipeline electronics
- Test plans
  - FADC test with PbF2
  - Calorimeter trigger test
  - Full setup
- Possible developments
- Conclusion

# NPS calorimeter



(a)

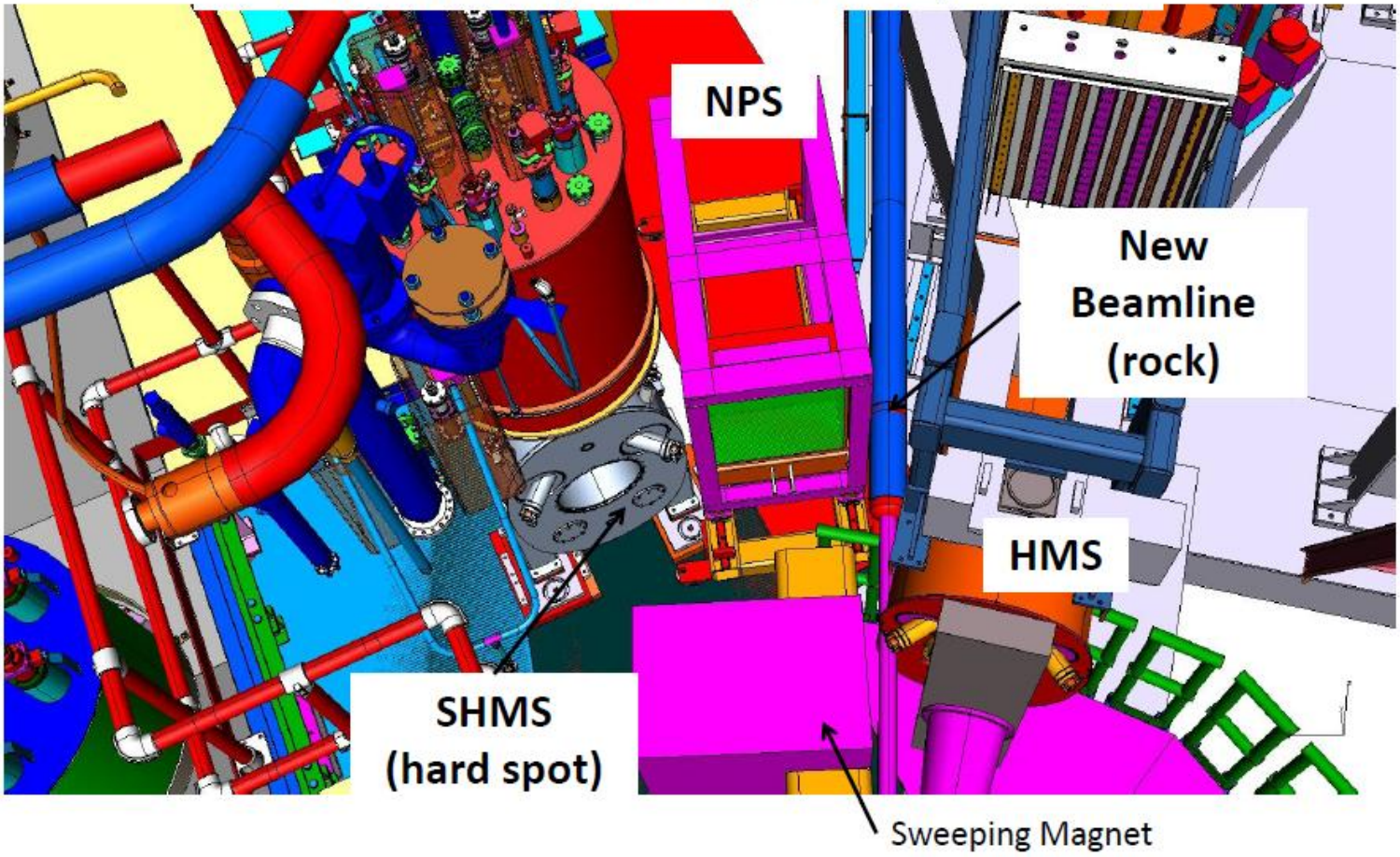


(b)

# NPS calorimeter

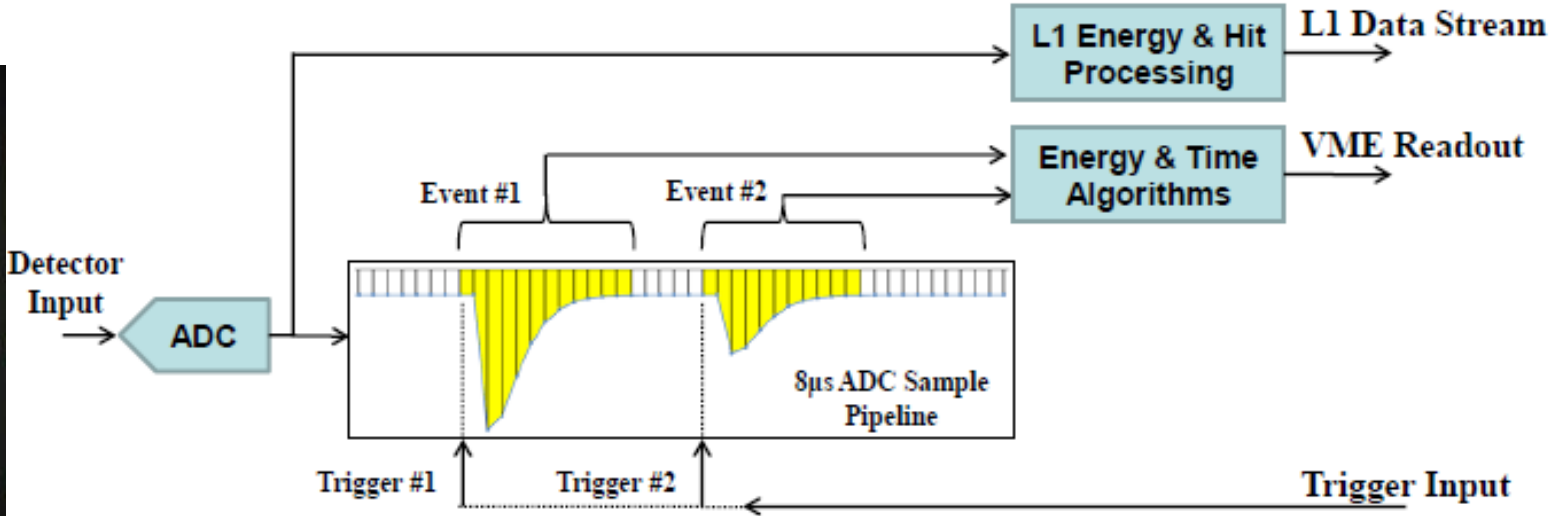
- 31x36 array of calorimeter blocks
  - 208 $PbF_2$
  - $PbWO_4$
- Sweeping magnet
- Small angle , high rate , high radiation capability

# NPS: 3 meter position, Birds Eye View



# JLAB FADC

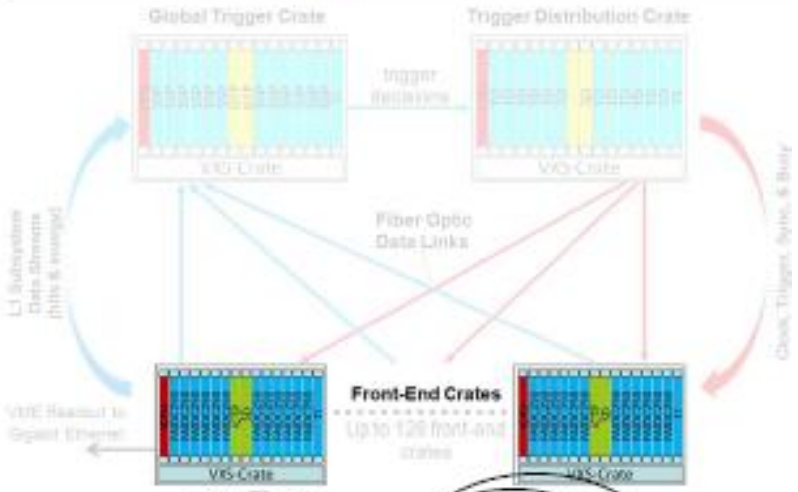
Pipelined electronics 250 MHz sampling rate 12 bit
On board FPGA processing : pedestal subtraction, thresholds , integral and time
and summing of channels for triggering purpose




Can record complete waveform but large amount of data
Can record time and integral of pulse : improve rate but no information on pile up
Looking into dealing with pile-up at FADC level

# Front-end Crates: Level 1 Trigger

- Each FADC250 stream L1 board energy sum/hit to Crate Trigger Processor (CTP) residing in VXS switch slot A
- Crate Trigger Processor computes a crate-level energy sum (or hit pattern)
- Computed crate-level value sent via 10Gbps fiber optics to Global Trigger Crate (32bits every 4ns)

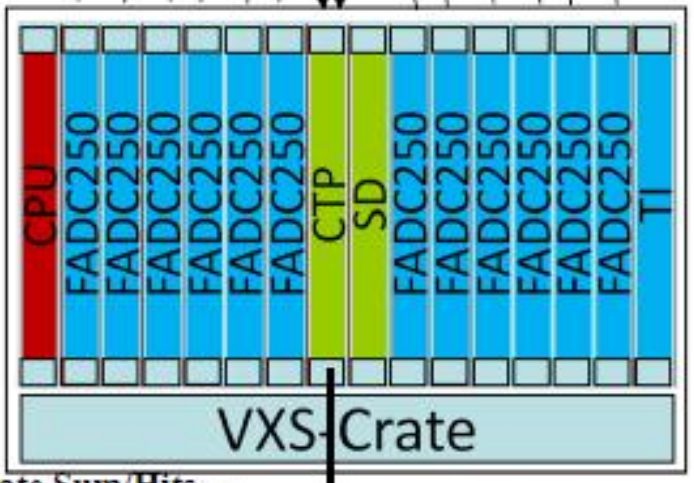



**CTP Prototype:**


Fiber Optics Transceiver

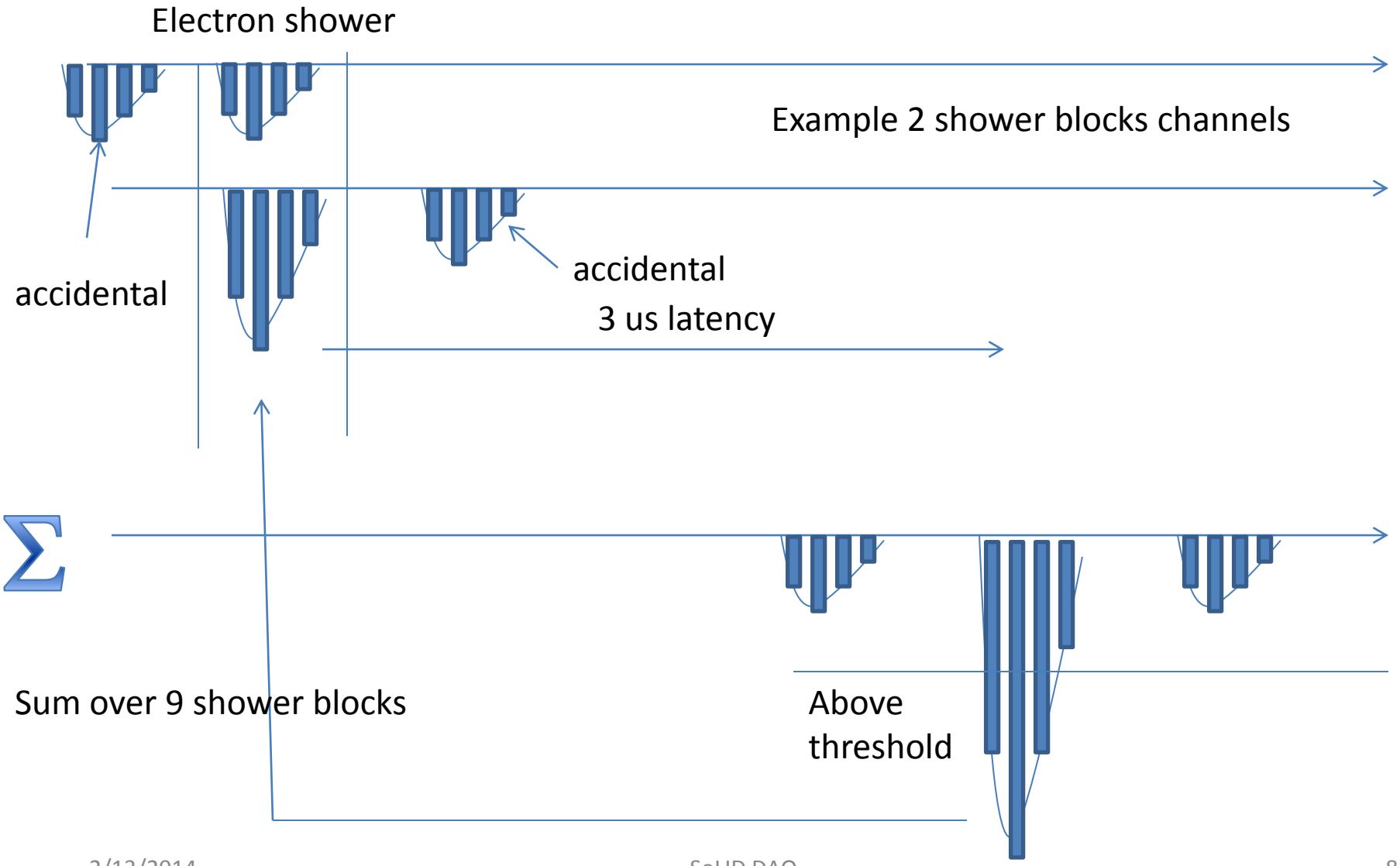
VXS Switch Connector

**Board Energy/Hits 5Gbps to CTP**



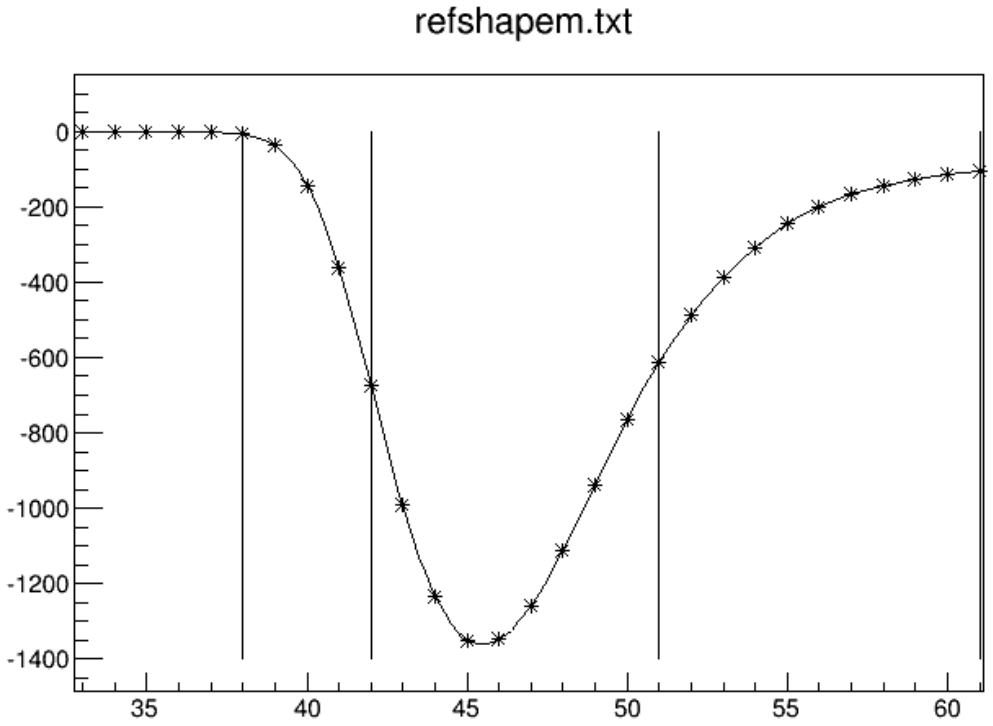

**Crate Sum/Hits 10Gbps Fiber to Global Trigger Crate**

# Calorimeter trigger example of CTP sum



# Test

- 1 VME64X
- 1 CPU
- 1 SD
- 1 TI
- 1 FADC



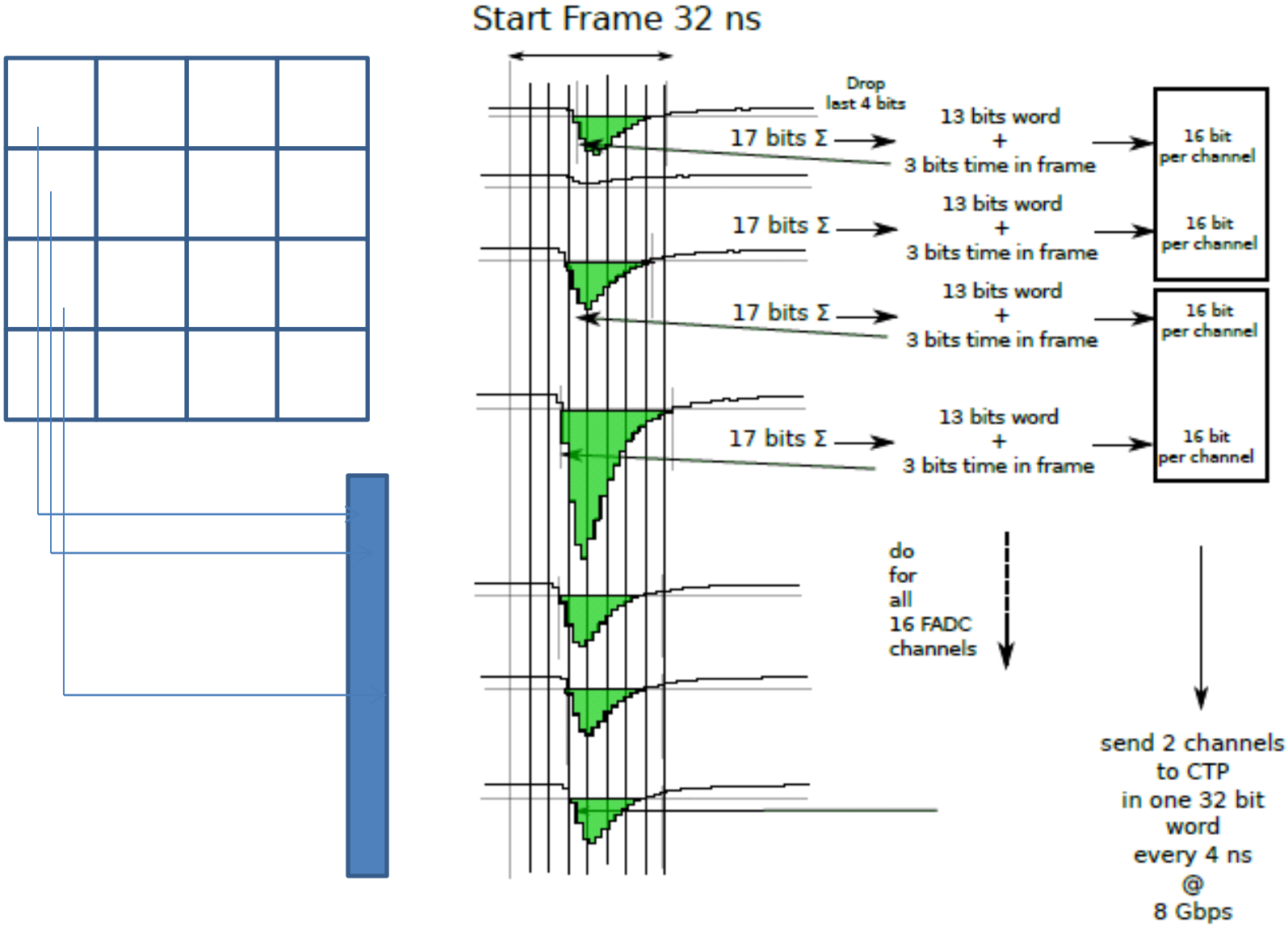

- Can test transfer
- Effect of the 250 MHz sampling on signal with 12 ns FWHM ( might need to optimize signal shape/integration)

# Test triggering

- 1 VXS
- 1 CPU
- 1 SD
- 1 TI
- 13 FADC
- 1 CTP

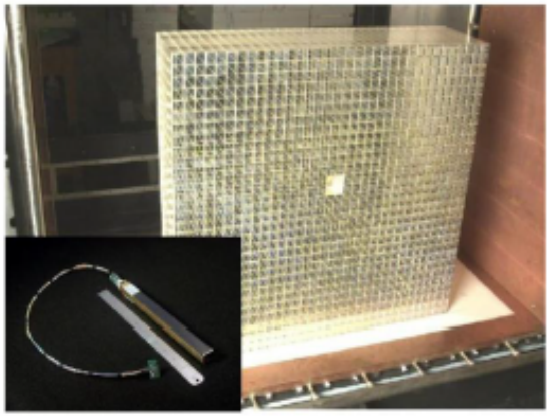
- Can test triggering on DVCS calorimeter ( 208 channels ) with cosmics and in beam in Fall 2014

# Clustering HPS like

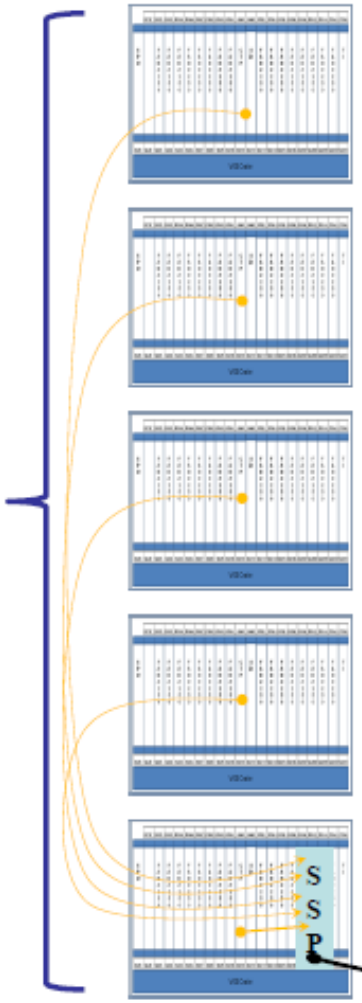


# Pipeline DAQ/Trigger for NPS (Low $Q^2$ )

31 x 36 2D Array
1116 - PMT Channels (R4125)
Coaxial output to FADC250



PrimEx PbWO crystals




Trigger from Calorimeter
Distributed to other Detector DAQ crates

- 256 channels/crate
- 5 VXS crates needed
- Need Crate Trigger Processors
- One VXS crate would need a SubSystem Processor

- SSP will need to combine clusters across 256 channel boundaries for final trigger
- Experiment trigger would be generated from the SSP and distributed to the other detector DAQ crates.

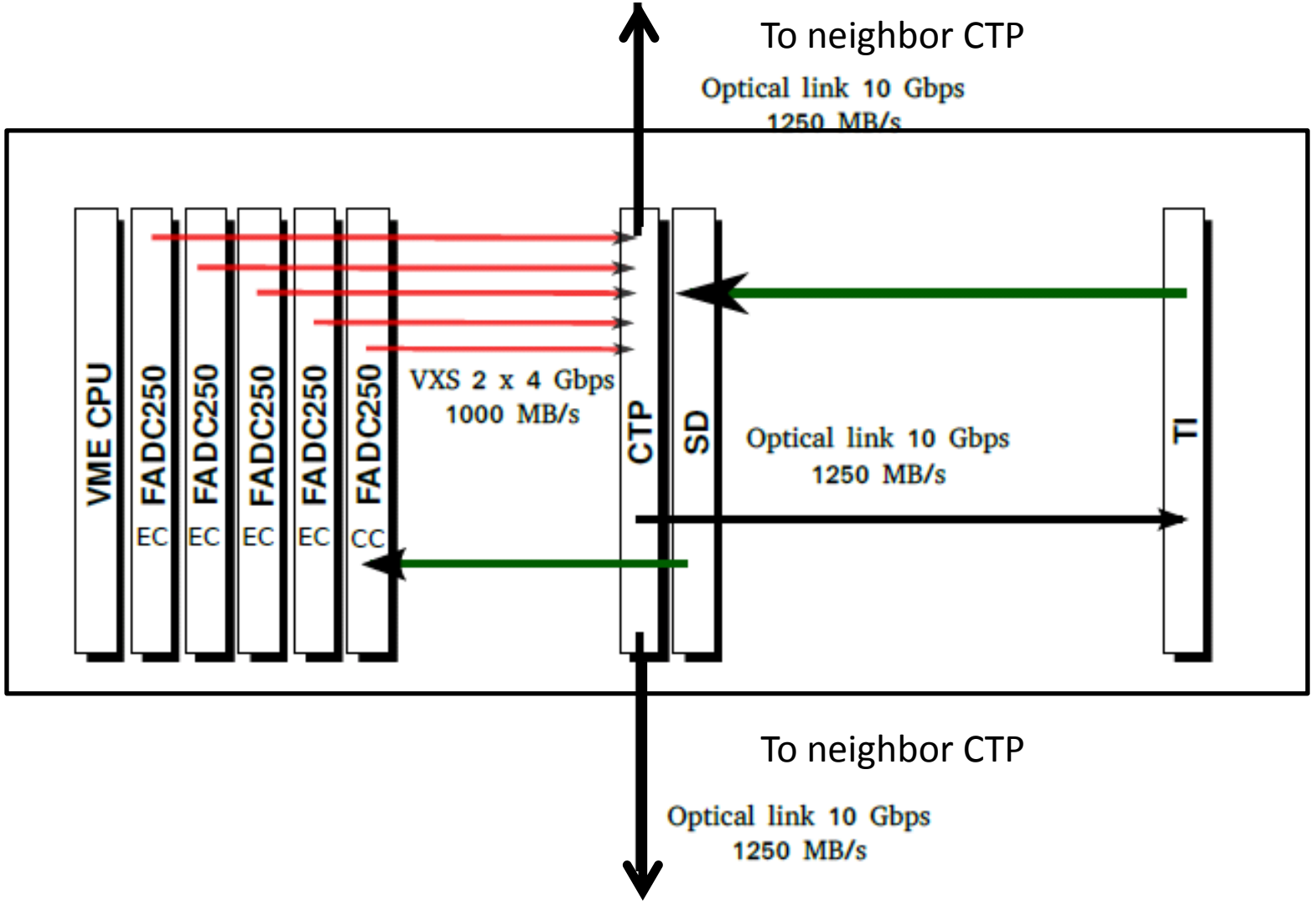
- Many details not shown but this type of Cluster finding trigger will require significant hardware cost commitment.
- Good news is that a good deal of firmware effort has been completed for the HPS cluster functions, so in principle these firmware features can be reused for NPS.

# Possible development

- Readout depending on pulse “goodness”
  - Integral and time only if pulse looks standard
  - Full waveform

- Selective FADC channel readout

# CTP connections



# FADC readout

- Only want to readout FADC channel in the cluster to reduce number of channels readout because of background
- CTP generates a 1116 bit pattern for channels to be read
- Send pattern to TI or FADC directly to trigger FADC
- Only channels from pattern are put in buffer
- Would introduce dead time but would be fine at low rate : 1116 assume 1 Gbit/s : 1.116 us additionnal latency ( FADC max latency 3.2 us )

# Conclusion

- Can start testing now with simple setup to check response of FADC with PbF2 signal and PbWO4
- If find VXS and CTP, can test triggering using Hall A DVCS calorimeter ( cosmics and maybe in beam in Fall 2014) : would be useful to study effect of background
- New development of FADC capabilities could benefit NPS