Electronics
Status and Upgrade Opportunities
for
Flash ADC and 12GeV Trigger Hardware

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Group Leader – *Fast* Electronics

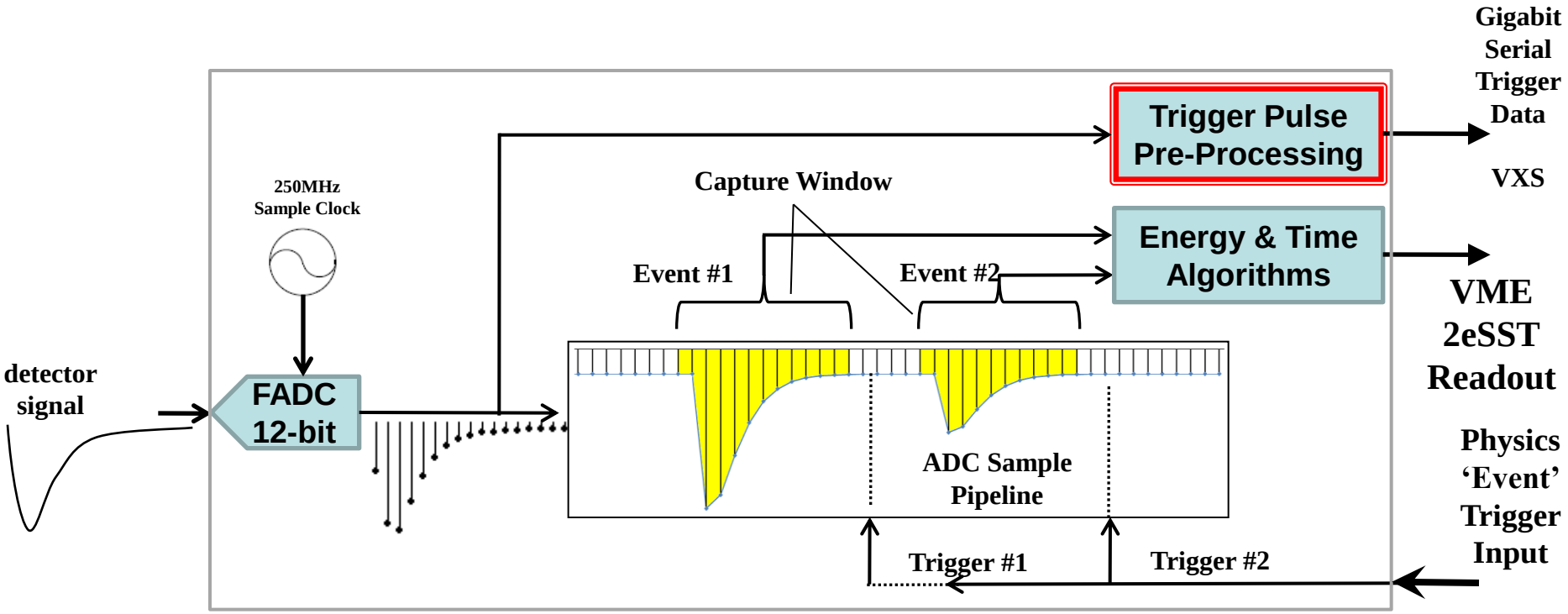
NPS Collaboration Meeting
Jefferson Lab
14-November-2013

OUTLINE

- **Brief Overview**
  - Pipeline DAQ
  - The Trigger information path
    - Use extension of VME with high speed Gigabit Serial (VXS or VITA-41)
  - Hardware Acronym Definitions
  - Trigger System Hardware, Methods and Examples

- **Hardware Status**
  - Production Board updates
  - System Test Activities, Results and New Applications
    - New DAQ hardware successfully used for Heavy Photon Search beam test → June 2012
    - Using pipeline DAQ/Trigger for NPS at high e^- (Cluster finding)
  - **Summary**

Pipeline Method of Signal Capture



- 250MHz Flash ADC stores digitized signal in 8μs circular memory
- "Event" trigger extracts a window of the ADC data for pulse sum and time algorithms
- Trigger data contains detailed information useful for cluster finding, energy sum, etc.
- Firmware algorithms provide a huge data reduction by reporting only time & energy values for readout instead of raw samples

Acronym Definitions

- **VXS => VME with Serial Extensions (VITA 41.0)**
- **VITA => VME International Trade Association**

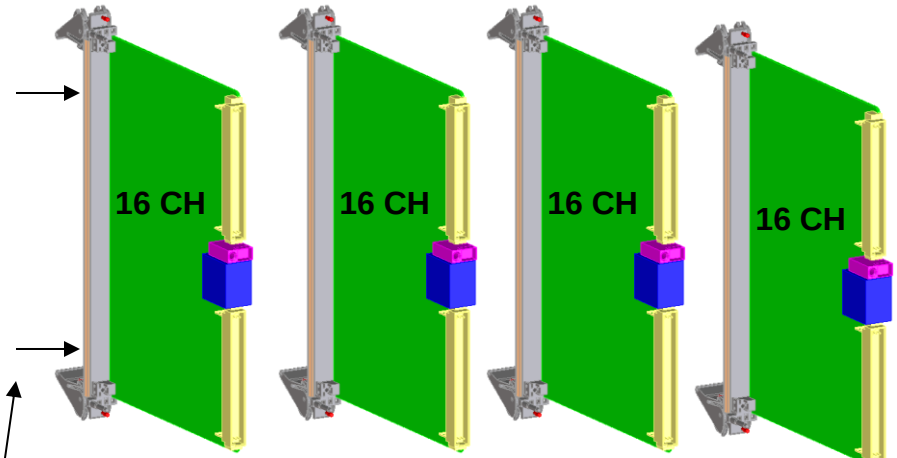
- **FADC250 => Flash Analog to Digital Converter 250MHz**
- **CTP => Crate Trigger Processor**
- **TI => Trigger Interface**
- **SD=> Signal Distribution**

- **SSP=> Sub_System Processor**
- **GTP=> Global Trigger Processor**
- **TS=> Trigger Supervisor**
- **TD=> Trigger Distribution**

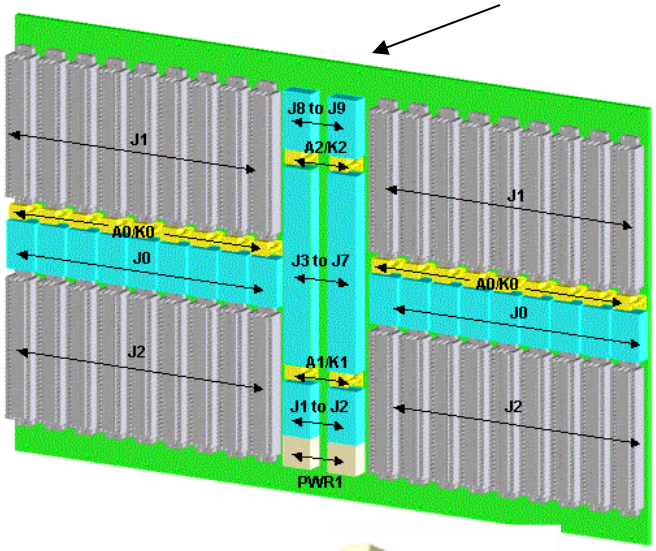
Quick VITA 41 *VXS Review

VXS "Payloads" (JLAB FADC)

(*VME with Serial Extensions)



VXS Backplane

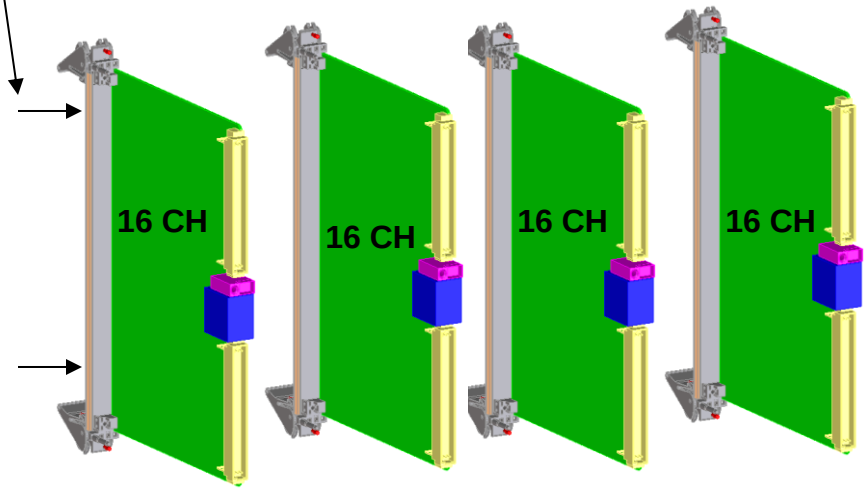


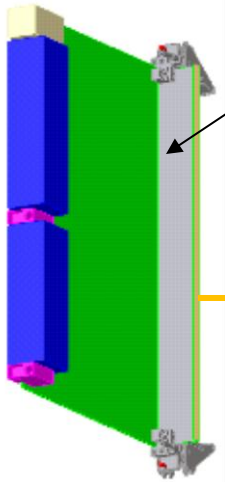
VME64

High Speed Serial

VME64

Detector Signals

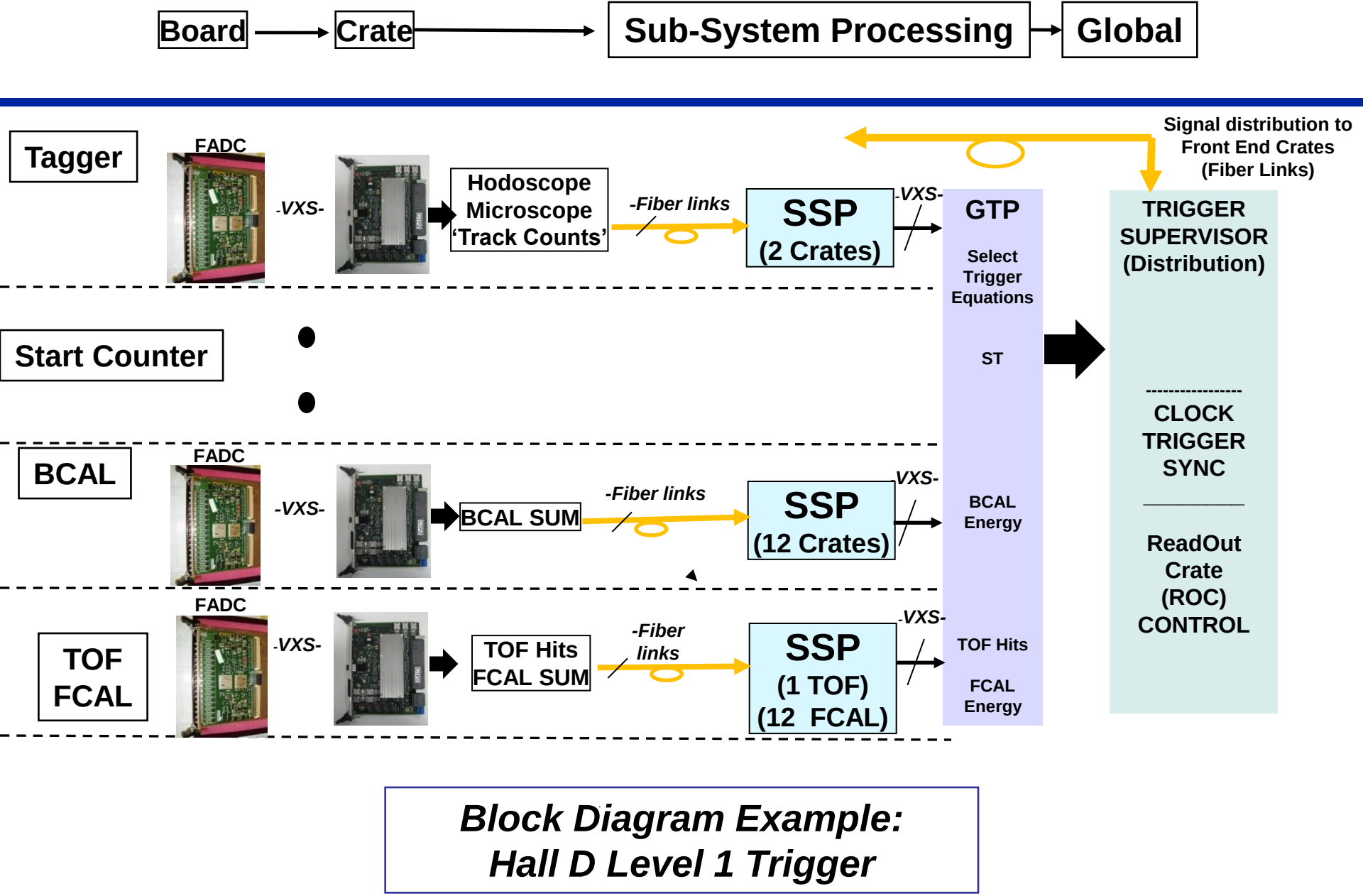




VXS "Switch" Card
Crate Trigger
Processor

8Gb/s
Fiber

Energy Sum
to Trigger



Block Diagram Example:
Hall D Level 1 Trigger

All Trigger Modules Delivered!

L1 Trigger 'Data'
MTP Ribbon Fiber

Global Trigger Crate
- Sub-System Processor
- Global Trigger Processor

Trigger 'Link" Contro
Clock, Sync
MTP Ribbon Fiber

Front End Crate
- FADC250, (FADC125), (F1TDC)
- Crate Trigger Processor
- Signal Distribution
- Trigger Interface

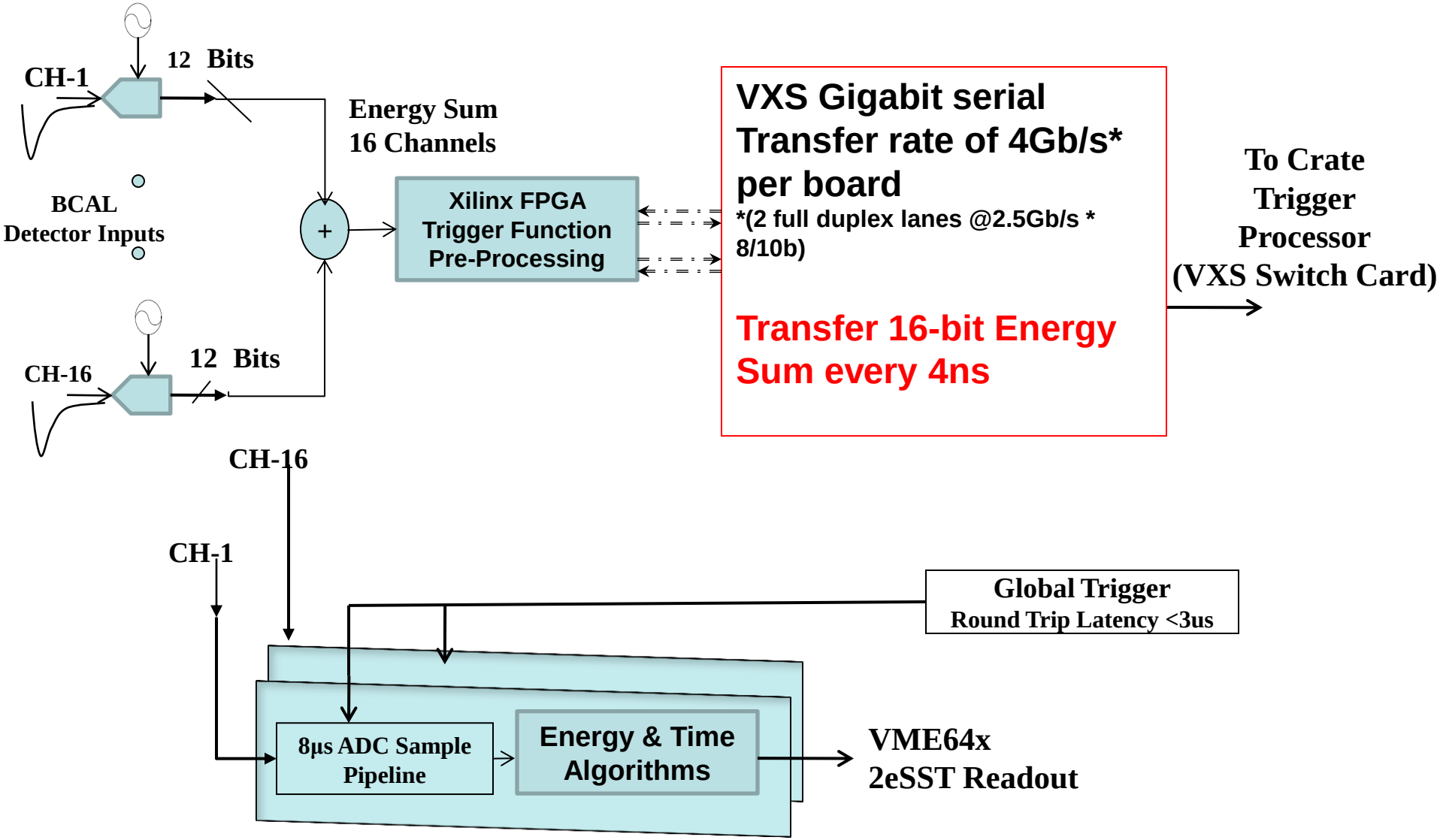
Trigger Control/Synchronization
- Trigger Supervisor
- Trigger Distribution

Production Board Quantities

60 more due 21-Nov

Board ID	Hall D	Hall B	Halls A & C	Total
FADC250	350	310	66	726 + 60
Trigger Interface	64	82	12	158
Signal Distribution	60	53	2	115
Crate Trigger Processor	30	21	2	53
Sub-System Processor	10	15	2	27
Global Trigger Processor	2	2	2	6
Trigger Distribution	8	8	2	18
Trigger Supervisor	2	2	2	6

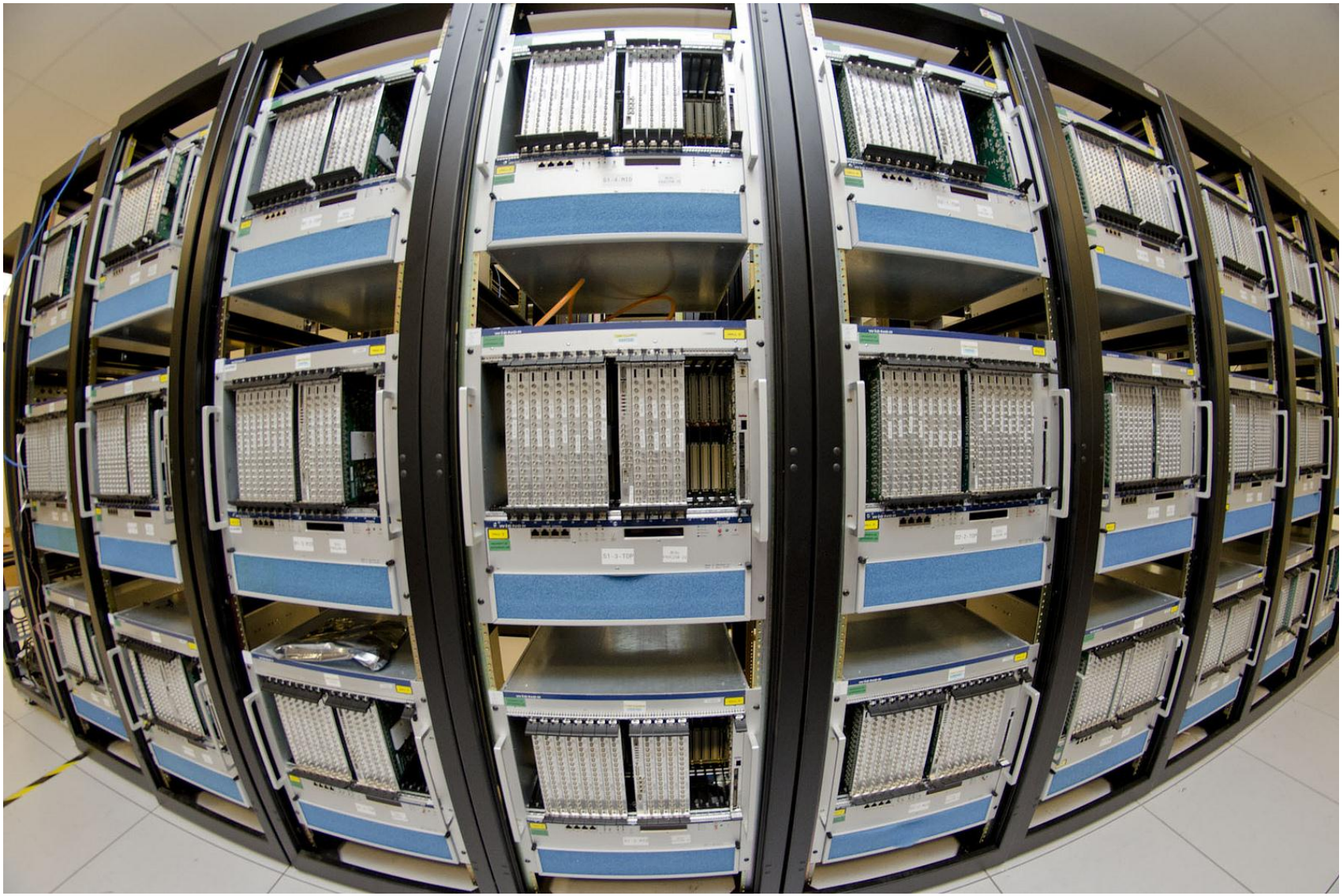
Present Flash ADC Implementation
Energy Sum Trigger (Present implementation for Hall D)



Flash ADC 250MHz

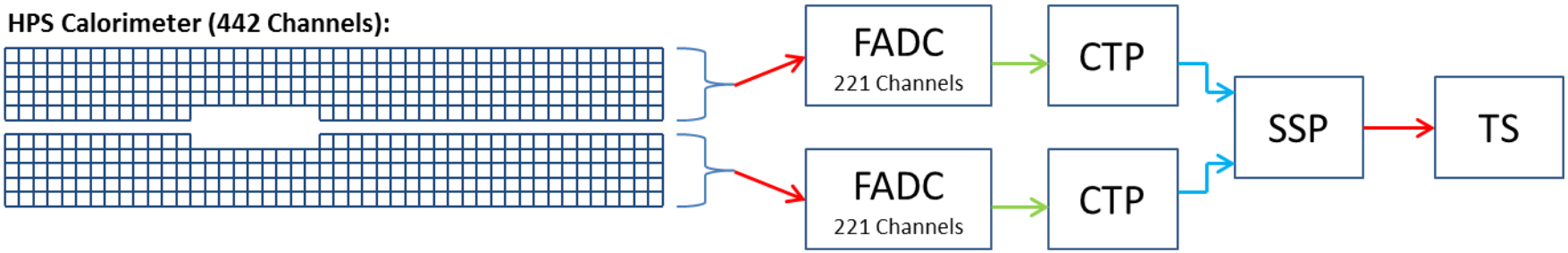
- 16 Channel, 12-bit
  - 4ns continuous sampling
  - Input Ranges: 0.5V, 1.0V, 2.0V (user selectable via jumpers)
  - Bipolar input, Full Offset Adj.
  - Intrinsic resolution – σ = 1.15 LSB.
  - 2eSST VME64x readout
  - Several modes for readout data format
    - Raw data
    - Pulse sum mode (Charge)
    - TDC algorithm for timing on LE
  - Multi-Gigabit serial data transport of trigger information through VXS fabric
  - On board trigger features
    - Channel summing
    - Channel coincidence
    - Hit counters (Scalers)
  - Used for HPS Test run
  - Installed in Hall D
    - Crates fully tested
  - Some Hall B crates populated tested (PCAL)

Flash ADC 250MHz



HPS ECAL Trigger Example

B. Raydo
S. Kaneta



FADC (Flash Analog-to-Digital Converter)

- 250Msps, 12bit pulse digitizer for: Readout & Trigger (energy, timing)
- Sends pulse energy & times to CTP for trigger processing

CTP (Crate Trigger Processor)

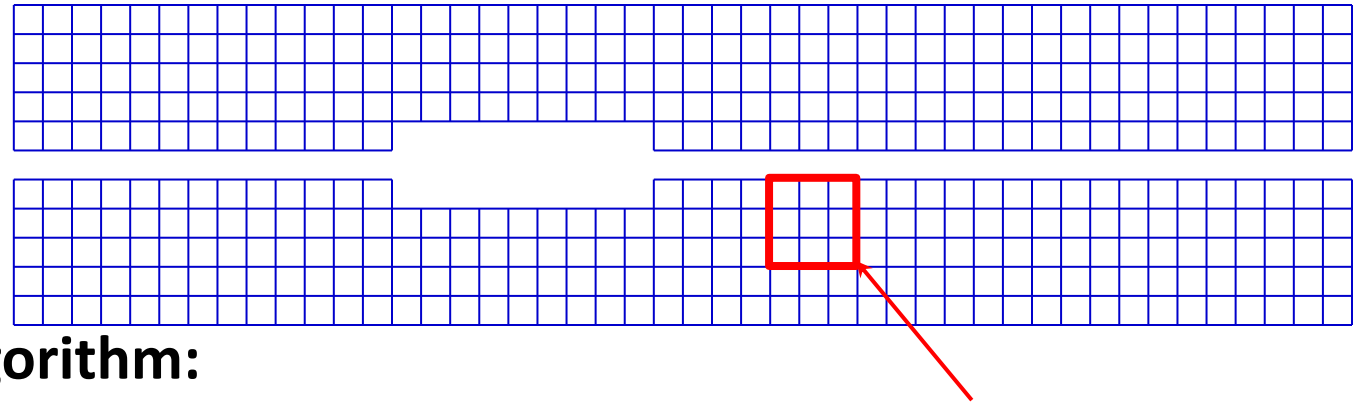
- Collects pulse data from all FADC channels in crate
- Searches for clusters on half (top or bottom) of the ECAL
- Sends cluster energy, time, position to SSP for trigger processing

SSP (Sub-System Processor)

- Collects cluster data from top & bottom halves of ECAL from CTP
- Performs cuts on individual clusters: energy
- Performs cuts on paired clusters: energy sum/difference, coplanar, distance energy
- Delivers Yes/No trigger signal(s) to TS (Trigger Supervisor) for readout

Cluster Finding - CTP Data Path

B. Raydo
S. Kaneta



CTP Algorithm:

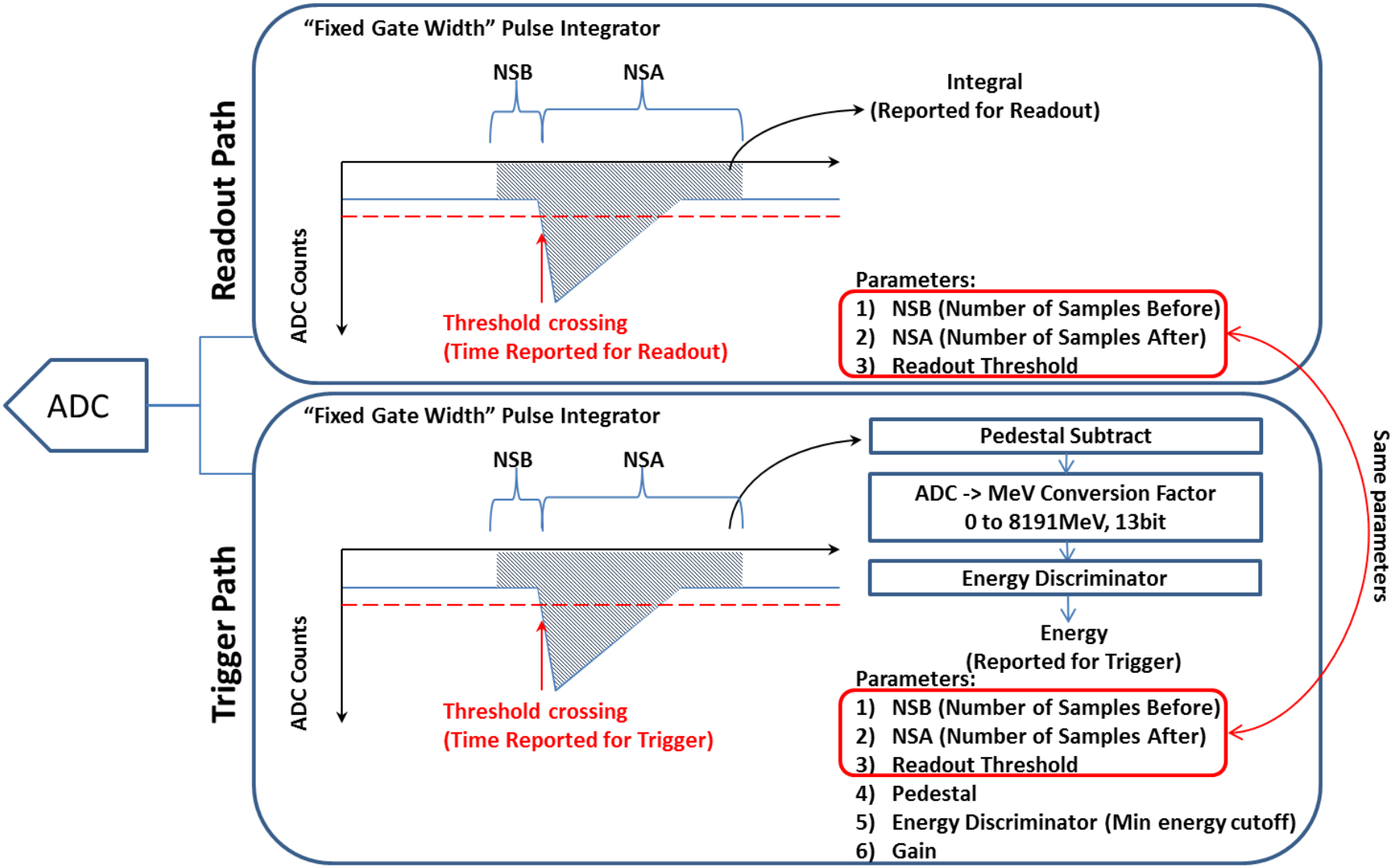
1. **Add energy from hits together for every 3x3 square of channels in ECAL**
2. **Hits are added together if they occur (leading edge) within a programmable number of clock cycles (4ns ticks)**
3. **If 3x3 energy sum >= cluster energy threshold, report cluster to SSP (time, energy, position and 3x3 hit pattern)**

Notes:

1) **Reported cluster information has 4ns timing resolution based on when cluster condition is satisfied**
2) **Reported cluster position is not centroid – it is within +/-1 crystal index of centroid**

FADC Data Paths

B. Raydo



FADC Charge Resolution

B. Raydo

- **FADC is: 12bit 250Msps, 50Ω Termination**
- **Front-end input range: -0.5V, -1V, -2V**
- **Set input range above maximum pulse height to ensure no signal clipping (-1V used in HPS test run)**

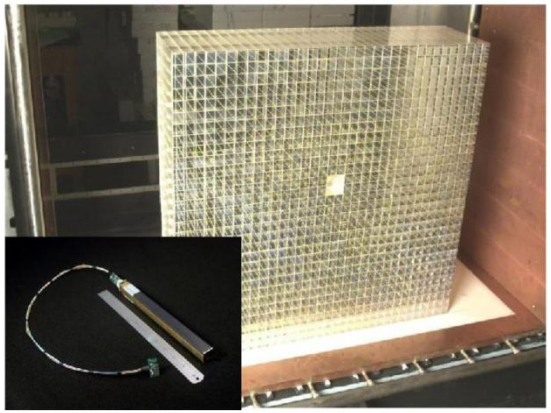
Noted that R4125 PMT with 'Active' Base has -4V (-80ma/50 Ohm) MAX Need to verify signal range for NPS

Charge resolution is:

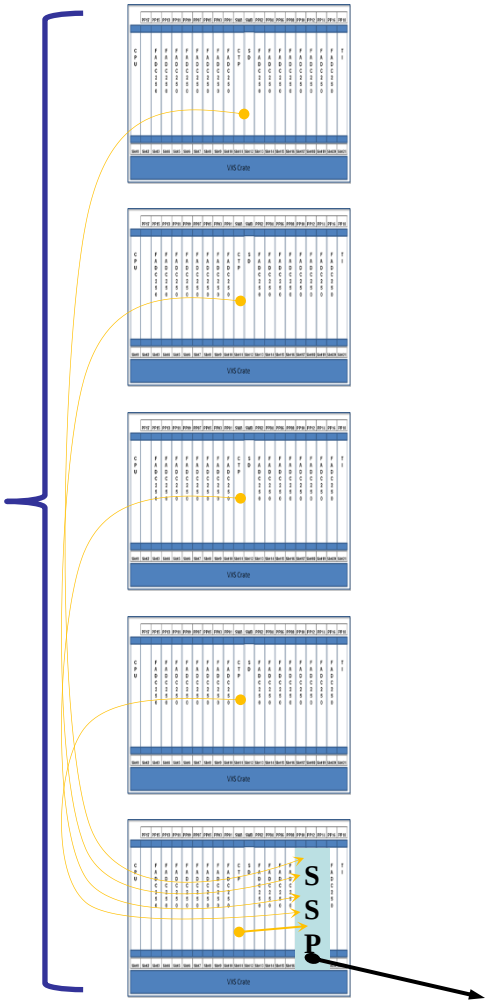
Input Range	Nominal Charge Resolution
-0.5V	9.76fC per ADC count
-1V	19.53fC per ADC count
-2V	39.06fC per ADC count

Pipeline DAQ/Trigger for NPS (Low Q^2)

31 x 36 2D Array
1116 - PMT Channels (R4125)
Coaxial output to FADC250



PrimEx PbWO crystals



- **256 channels/crate**
- **5 VXS crates needed**
- **Need Crate Trigger Processors**
- **One VXS crate would need a SubSystem Processor**

- **SSP will need to combine clusters across 256 channel boundaries for final trigger**
- Experiment trigger would be generated from the SSP and distributed to the other detector DAQ crates.

- Many details not shown but this type of Cluster finding trigger will require significant hardware cost commitment.
- Good news is that a good deal of firmware effort has been completed for the HPS cluster functions, so in principle these firmware features can be reused for NPS.

H/W Histograms

FADC

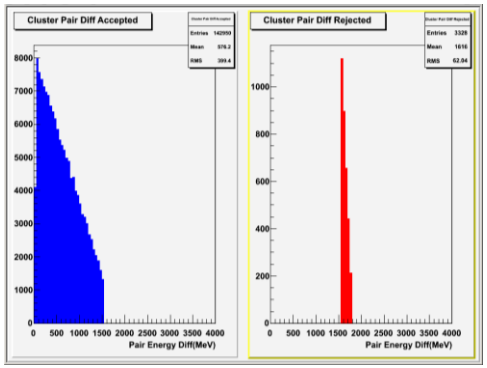
1. Scalers per channel (readout threshold based)

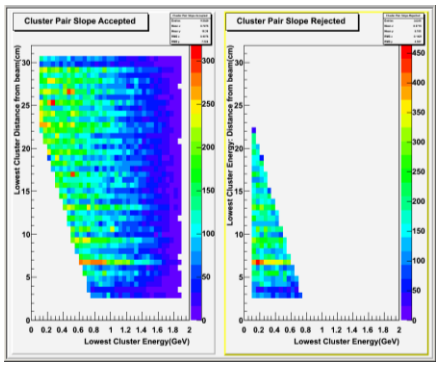
CTP (or FADC)

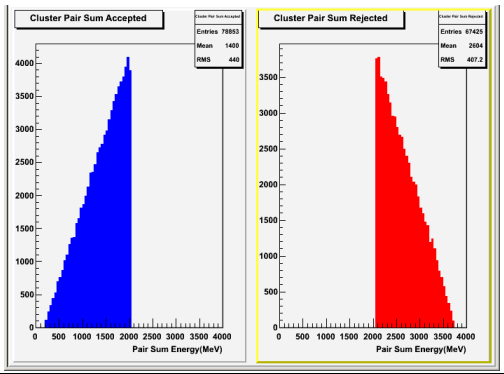
1. Individual ADC channel pulse energy histograms

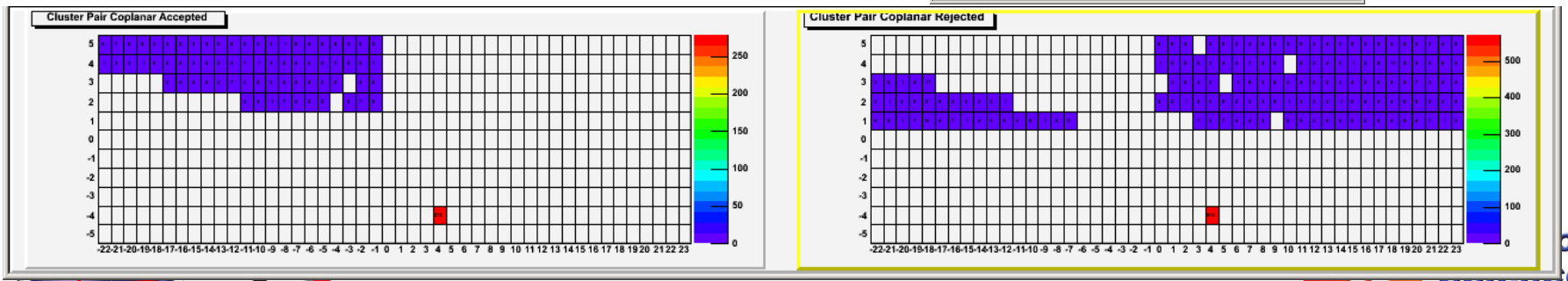
SSP

1. Cluster Hits (Position)
2. Cluster Hits (Position+Energy) - Depending on resources in SSP
3. Trigger cut accept/reject:

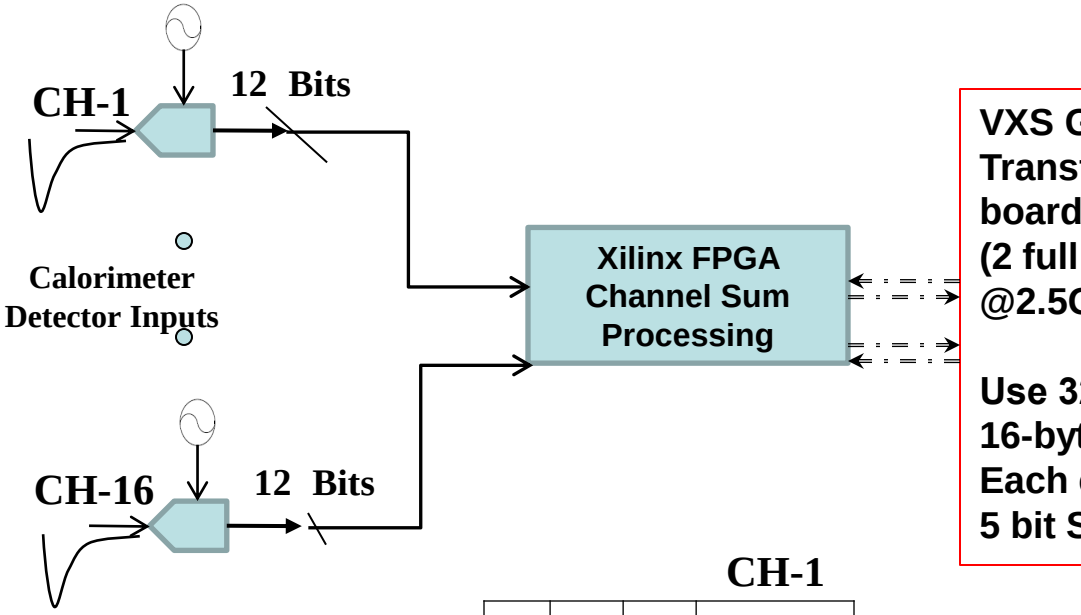








Trigger Data Encoding Format
HPS Test Run – May 2012



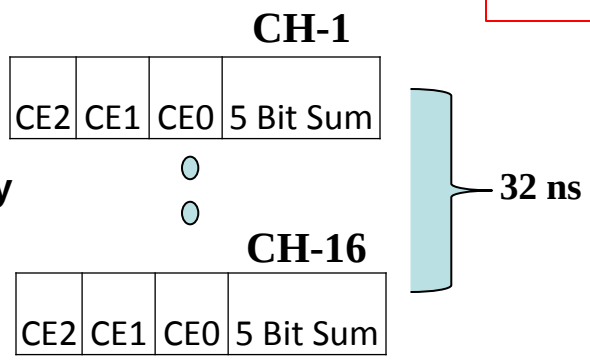
Xilinx FPGA
Channel Sum
Processing

VXS Gigabit serial fabric
Transfer rate of *4Gb/s* per board
(2 full duplex lanes @2.5Gb/s)

Use 32ns 'frame' to Transfer 16-bytes
Each channel is 1 byte:
5 bit Sum + 3 bits for timing

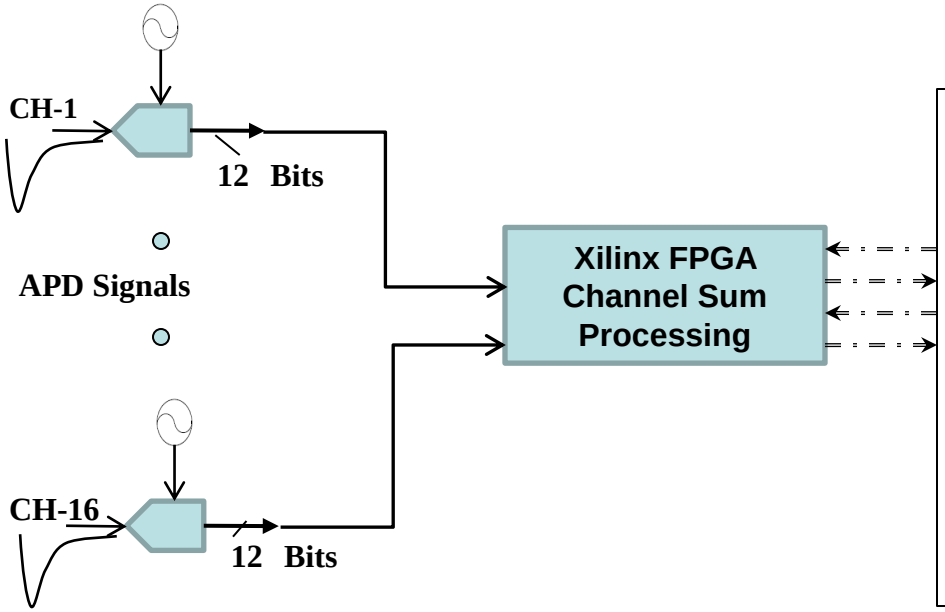
To Crate Trigger Processor (VXS Switch Card)

3 bit clock encoding
Allows 4ns clock recovery in 32ns 'frame'



16 Bytes in 32ns
Meets the *4Gb/s* transfer bandwidth
Per board

HPS Firmware Upgrade Notes
New FADC250 Firmware and New CTP Design



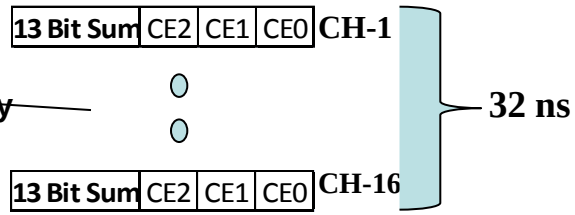
VXS Gigabit serial fabric
Transfer rate of *8Gb/s** per board

*(2 full duplex lanes @5Gb/s =10Gb/s * 8/10b encoding)

Use 32ns 'frame' to Transfer 16-bytes
Each channel is 16 bit word:
13 bit Sum + 3 bits for timing

→ To Crate Trigger Processor (VXS Switch Card)

3 bit clock encoding
Allows 4ns clock recovery in 32ns 'frame'

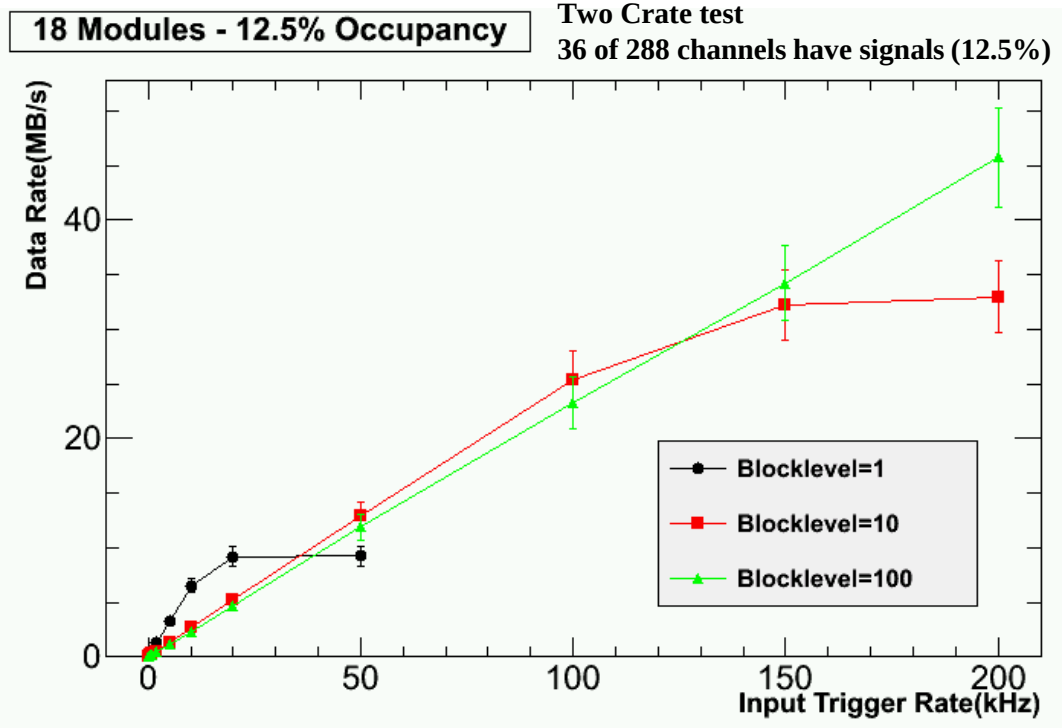


32 Bytes in 32ns
Will require that the FADC250 transfer bandwidth doubles to *8Gb/s*

- Existing CTP used close to 70% of FPGA resources For HPS Test Run Trigger Application
- CLAS12 will use CTP for three plane calorimeters
  - PCAL, ECAL
  - Possibility for more complex trigger algorithms
- Proposal for CLAS12 wire chambers to use CTP
- Output Fiber Transceiver will be upgraded
- Requirements document complete
- New hardware design

DAq Trigger & Readout Performance

- System testing includes:
  - Gigabit serial data alignment
    - ✓ 4Gb/s from each slot
    - ✓ 64Gb/s to switch slot
    - ✓ Crate sum to Global crate @8Gb/s
  - Low jitter clock, synchronization
    - ✓ ~1.5ps clock jitter at crate level
    - ✓ 4ns Synchronization
  - Trigger rate testing
  - Readout Data rate testing
  - Overall Trigger Signal Latency
    - ✓ ~2.3us (Without GTP and TS)



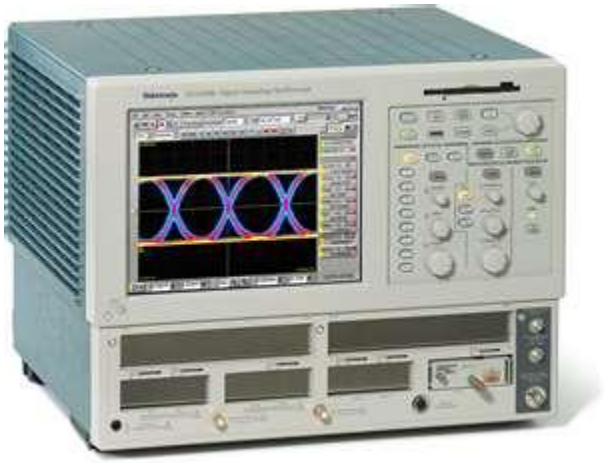
200KHz Trigger Rate!

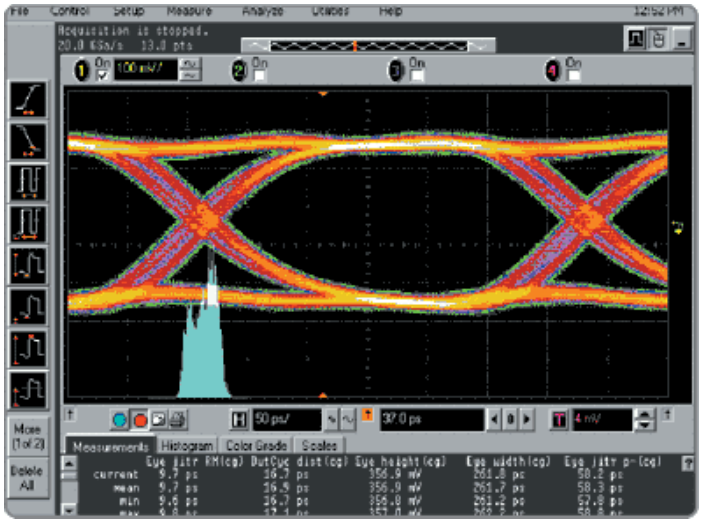
Readout Controller Capable of 110MB/s
- Testing shows we are well within limits

Summary

- **All production boards delivered**
  - **Repair/rework for boards that did not pass testing is progressing**
  - **Hall C Crate Trigger Processors will need rework**
    - **Production CTP to Hall D to meet schedule**
  - **Fiber and patch panels/cable have been ordered and received for Hall C**
- **Two full crate DAQ system used successfully for the Heavy Photon Search test in Hall B. (May 2012)**
  - **Excellent test foundation for software drivers, new calorimeter trigger algorithms and detector commissioning tools.**
  - **Cluster finding Trigger application performance exceeds Energy summation function required for other experiments.**
  - **Similar functions/features for NPS calorimeter array can be reused**
- **Need to begin detailed specifications for trigger functions/monitoring ASAP for NPS**
- **<u>Infrastructure and Engineering support/expertise exists for custom trigger algorithms. Plan for firmware development and test verification time.</u>**

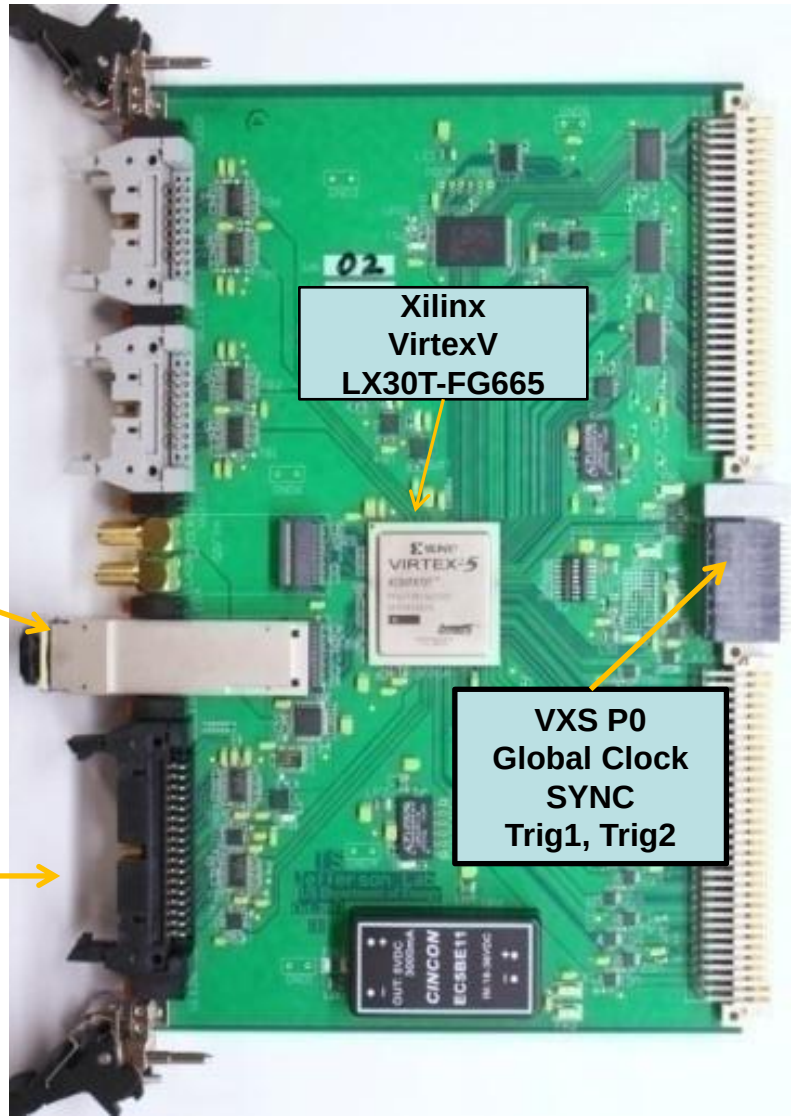
Backup slides





Trigger Hardware Status - TS

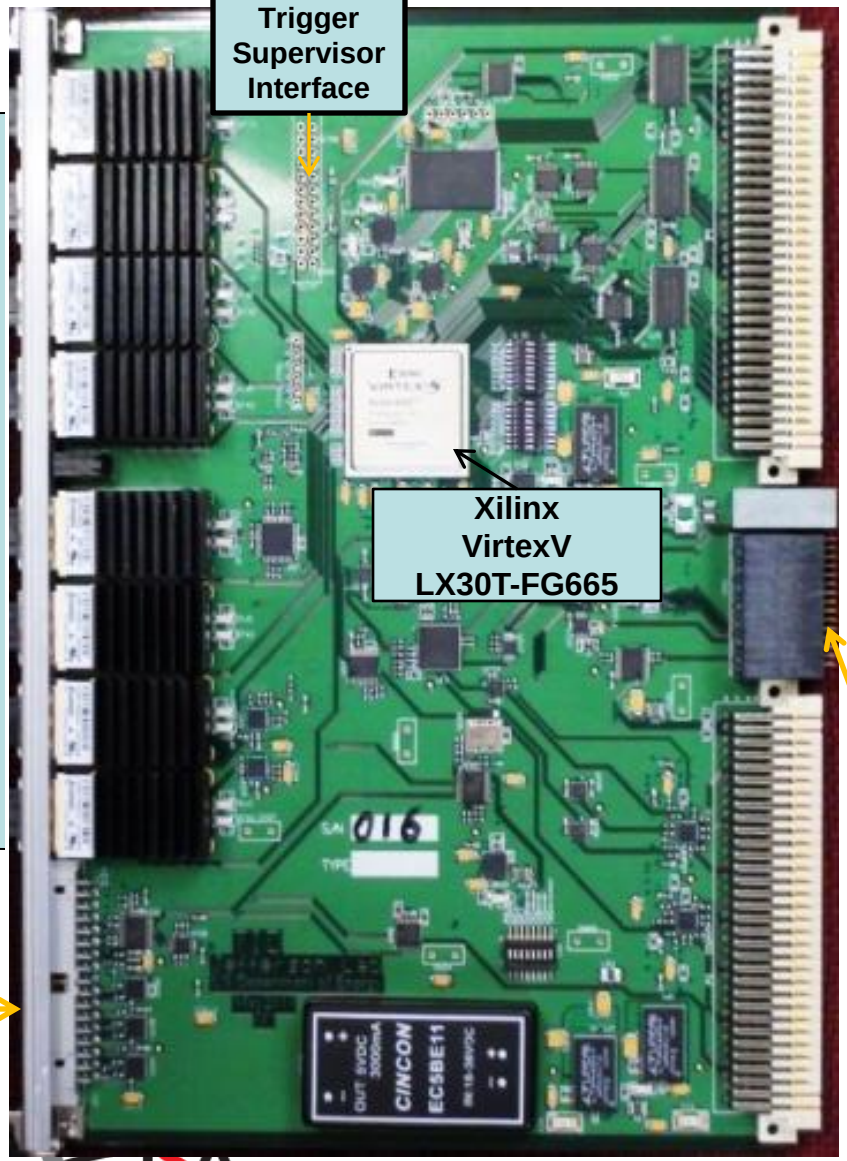
W. Gu
DAQ Group



- Receives 32 trigger ‘Bits’ from GTP on P2 via RTM
- Global precision clock source connected to SD on VXS backplane
- Synchronization and Trigger Word distributed to crate Trigger Interface boards via parallel fiber.
- Manages global crate triggers and ReadOut Controller events
- VXS “Payload’ module

Trigger Hardware Status - TD

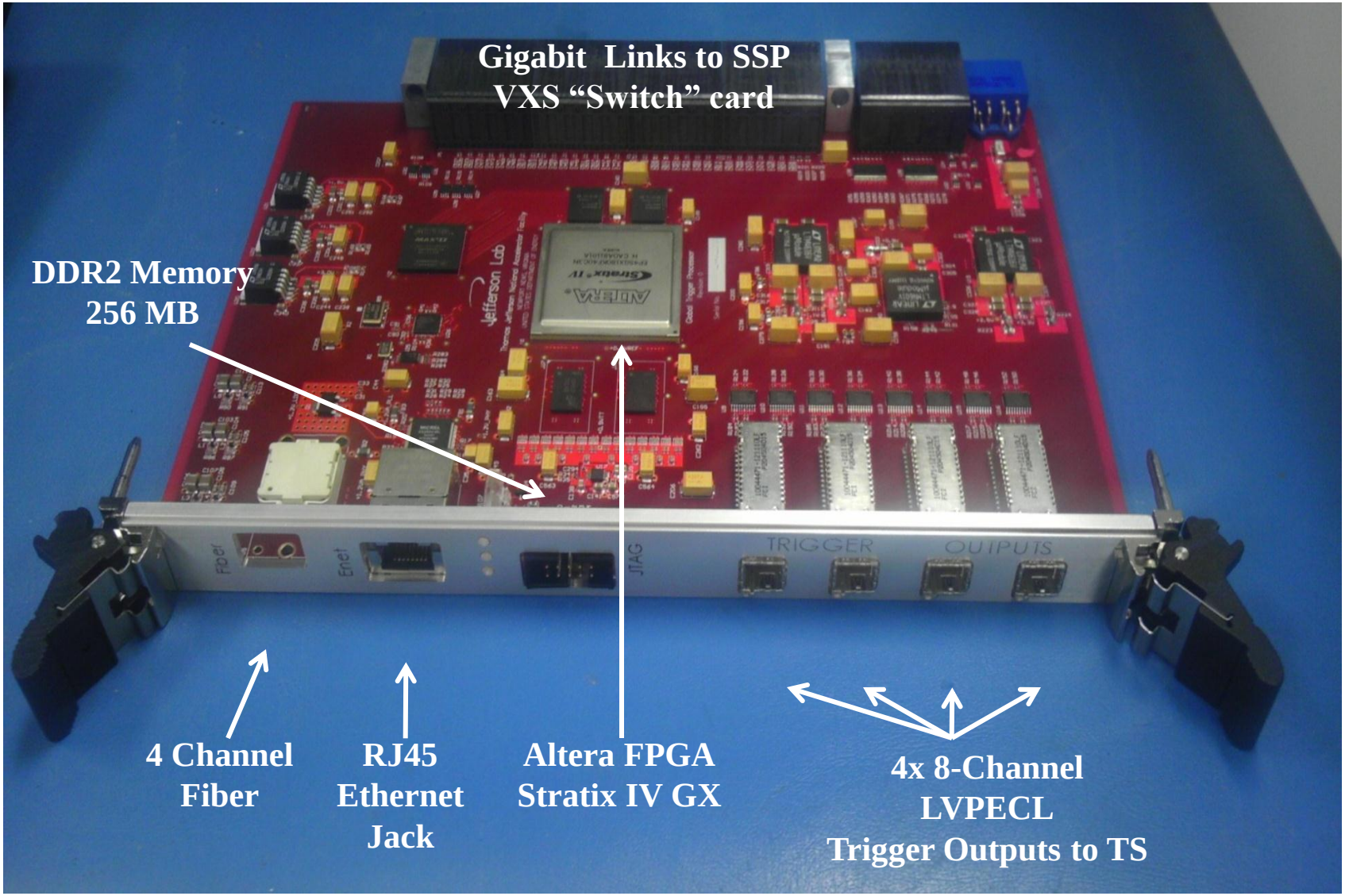
W. Gu
DAQ Group
23-Sept-2011



- Distributes from Trigger Supervisor crate to front end crates (TI)
- Distributes precision clock, triggers, and sync to crate TI modules
- Board design supports both TI and TD functions, plus can supervise up to eight front end crates.
- Manages crate triggers and ReadOut Controller events

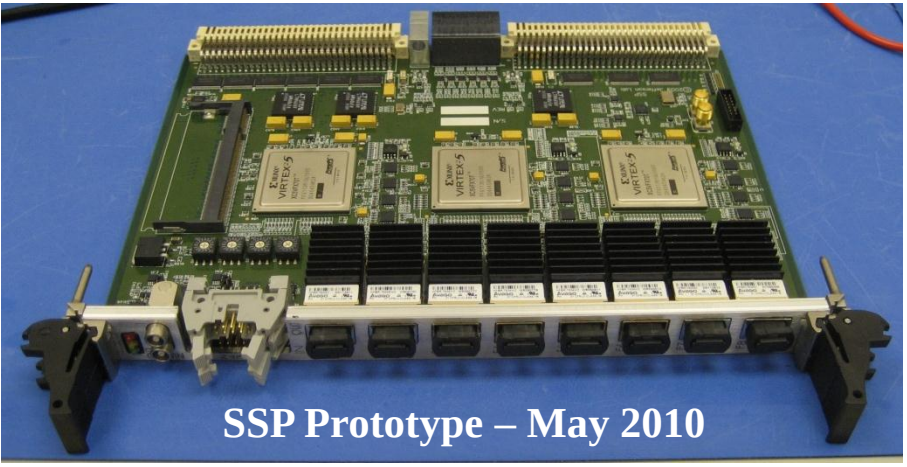
GLOBAL TRIGGER PROCESSOR
1st Article Board

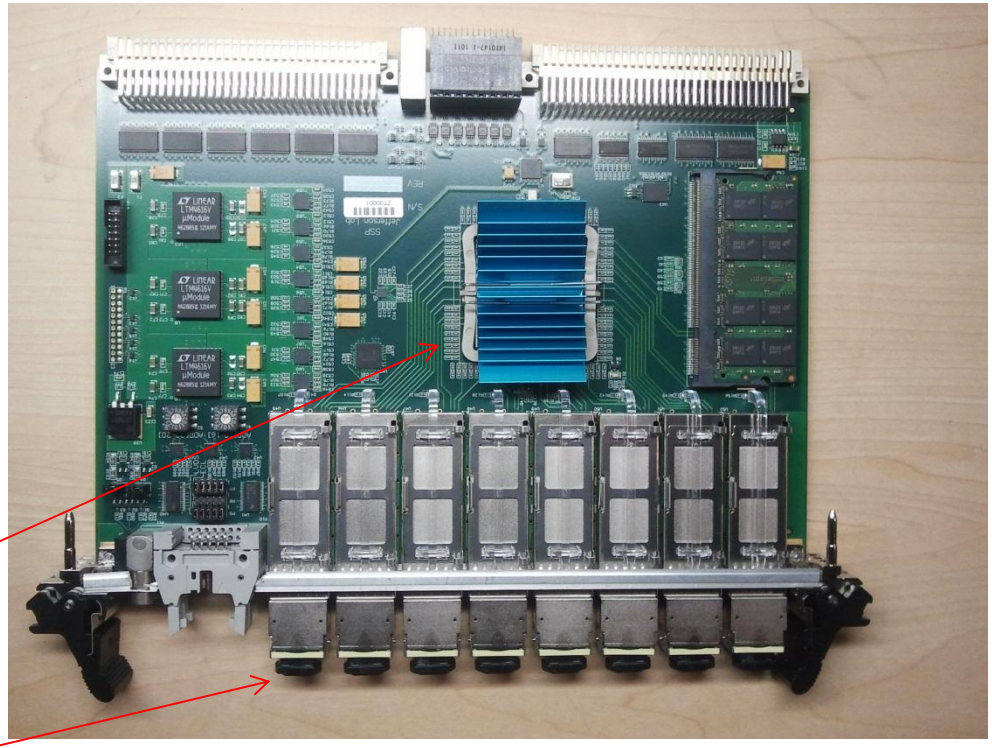
S. Kaneta
2011



Sub-System Processor Status

Ben Raydo





Production Status:

1) **Schematics & BOM complete**

→ **Single FPGA Virtex 5 TX150T**

→ **New Fiber Transceivers**

-- **Support 10Gb/s (4 'Lanes')**

-- **Significant cost savings ($40K)**

A. **Assembly contract awarded**

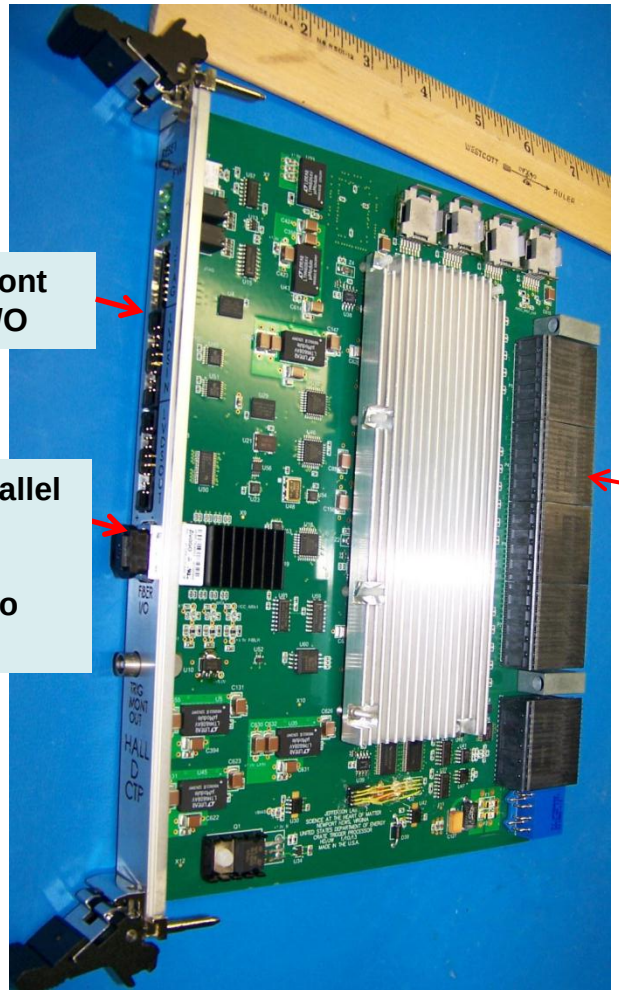
B. **Gerbers are ~100% complete, expecting delivery to vendor by Nov 1st.**

C. **Parts for 1st article arrive Oct 17, 2012…1st article shipment in December**

ALL Production SSP Delivered and tested

Crate Trigger Processor

Hai Dong
Jeff Wilson

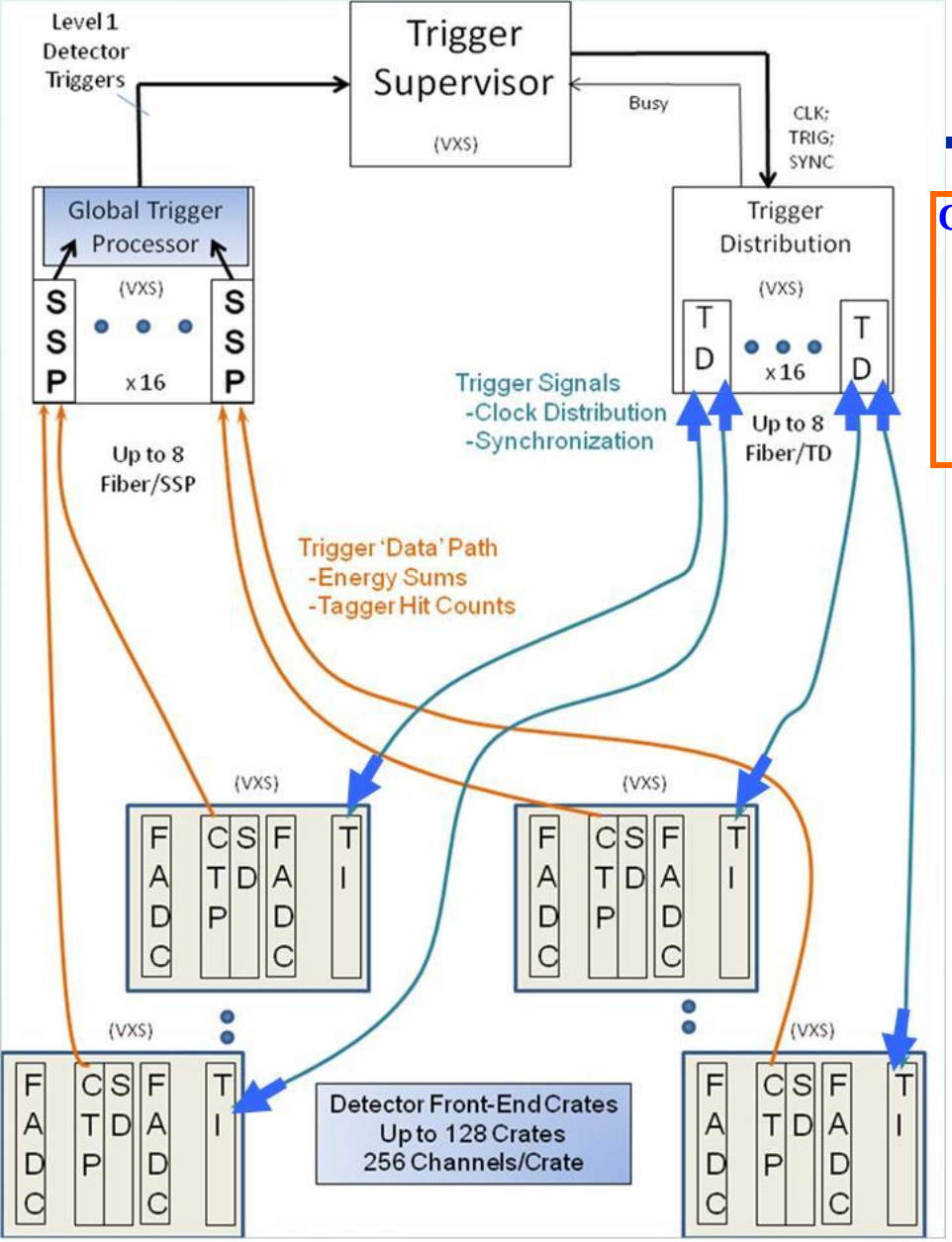


2013 Production CTP

- Crate Trigger Processor (CTP)
  - ✓ Hall D production quantities (32) awarded to MTEQ in Virginia!
  - ✓ 1st Article board passes acceptance testing!
    - Production boards expected delivery 22July2013
      - Latest Virtex V FPGA parts will support 5 Gbps transfer speed with FADC250 and provide additional FPGA resources for future L1 algorithms

- ✓ Successful operation with HPS calorimeter beam test with latest cluster finding algorithm!!
- ✓ Sixteen FADC250 boards successfully tested in full crate with FCAT application

Trigger System Diagram

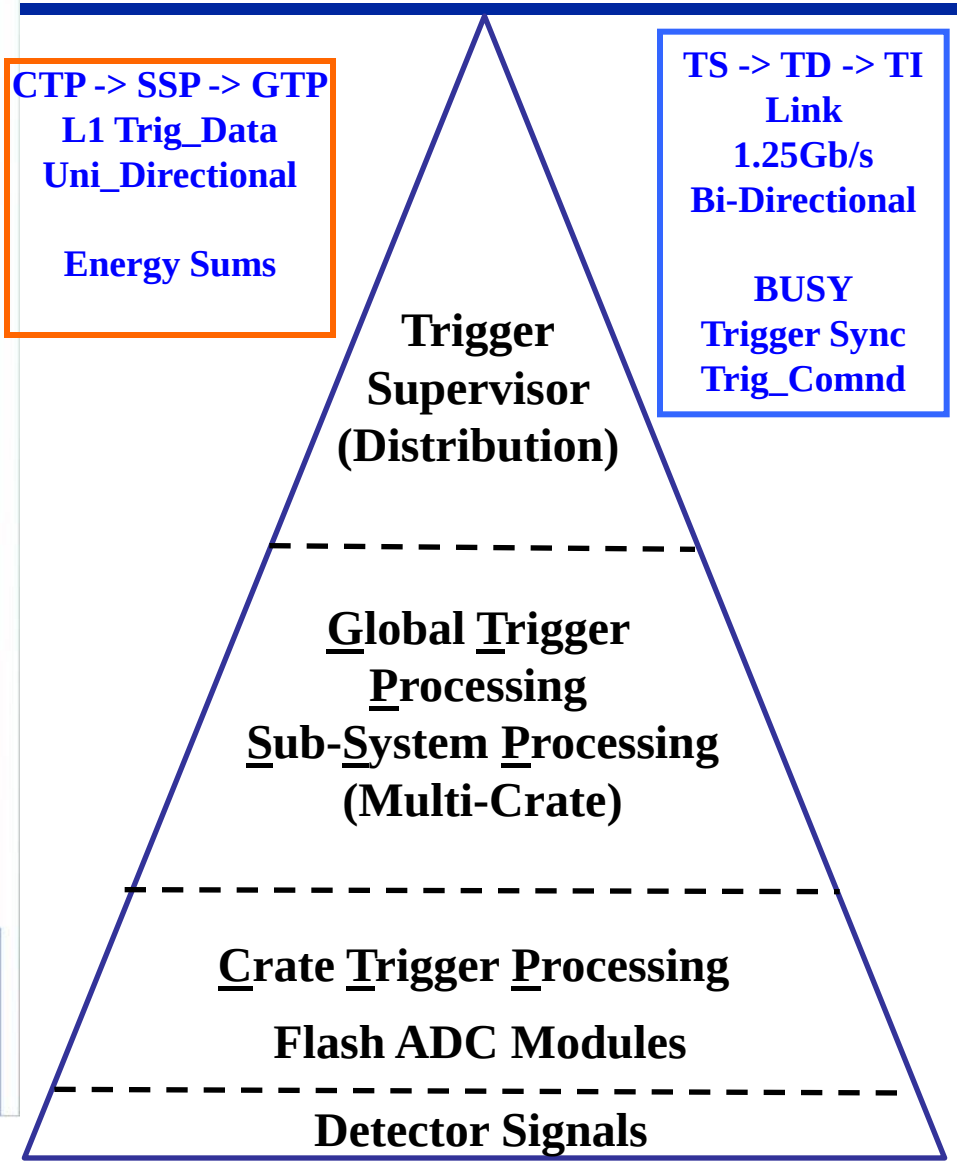


CTP -> SSP -> GTP
L1 Trig_Data
Uni_Directional

Energy Sums

TS -> TD -> TI
Link
1.25Gb/s
Bi-Directional

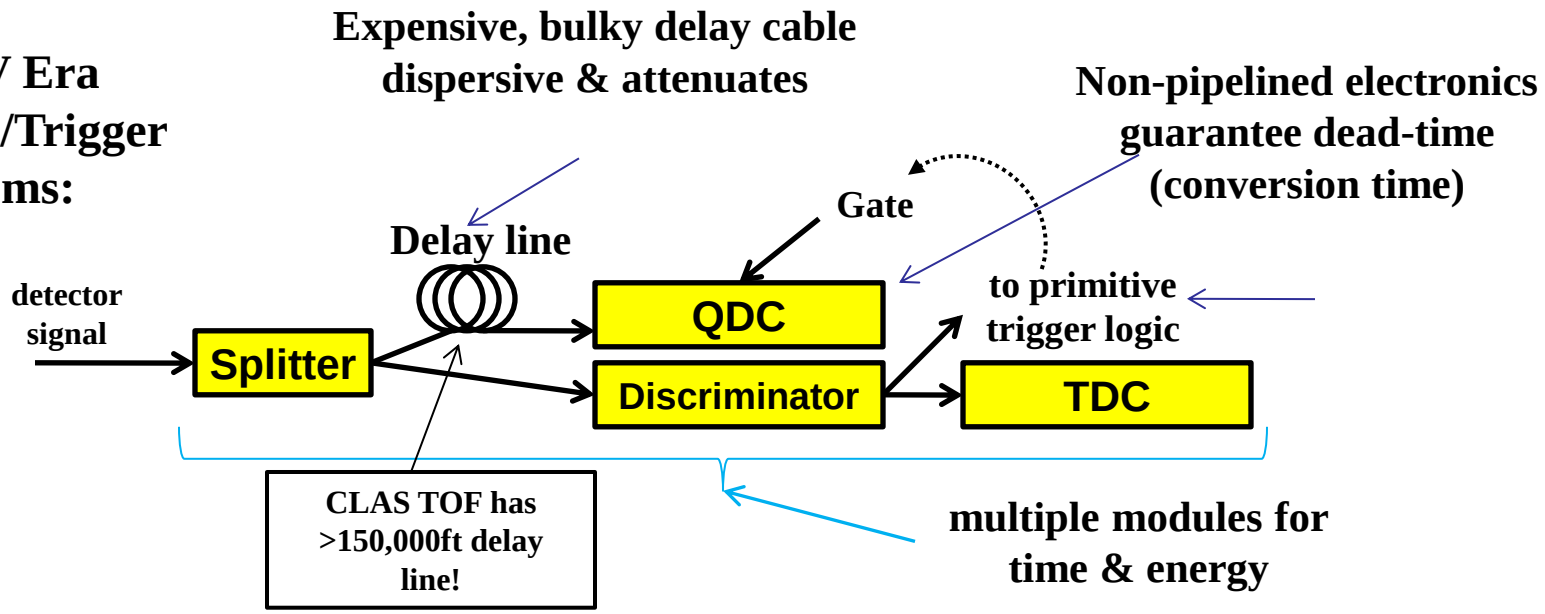
BUSY
Trigger Sync
Trig_Comnd



Triggers Arrive Simultaneously on Different Crates with Different Length Fiber Cable

The "Classical" method to capture detector signals

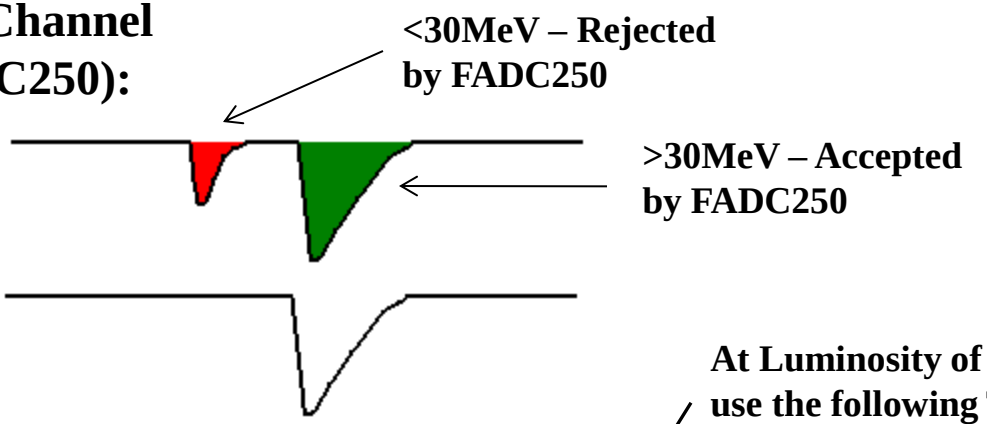
6GeV Era DAQ/Trigger Systems:



"Classic" DAQ Electronic examples:
FastBus 1881 QDC
FastBus 1887 TDC
Many NIM modules for Trigger Logic

GlueX Example L1 Trigger

BCAL & FCAL <30MeV Channel Suppression (done at FADC250):

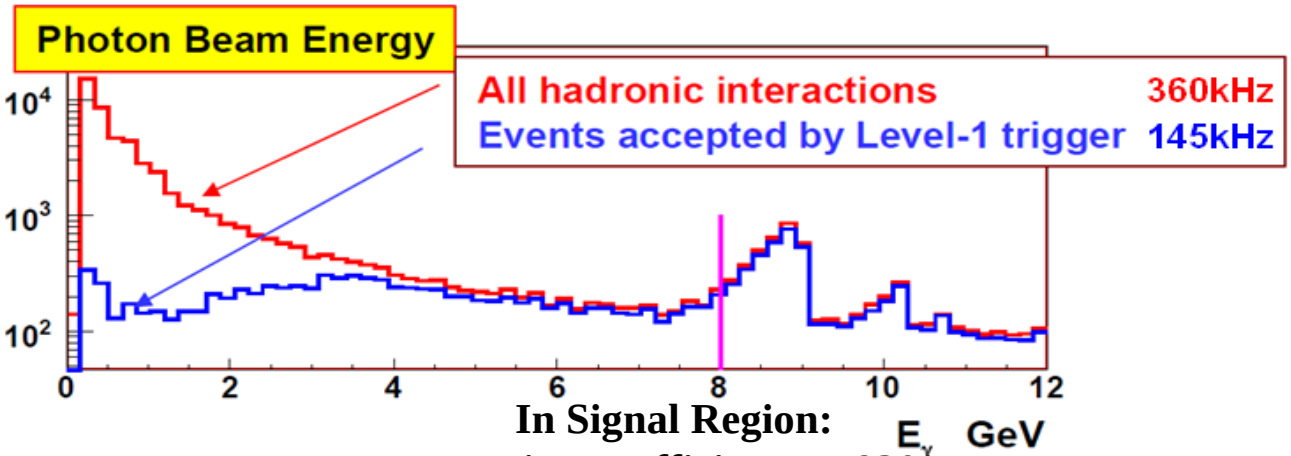


GTP Trigger Equation:

At Luminosity of $10^8\gamma$/s use the following Trigger equation

$$\sum_{t}^{t+100ns} ST_{hits} > 0 \;\&\&\; \sum_{t}^{t+100ns} BCAL_{energy} + 4 * FCAL_{energy} > 2GeV$$

Resulting L1 Acceptance Spectrum:



In Signal Region:
L1 Trigger Efficiency > 92%

At Luminosity of $10^7\gamma$/s Tagger hit counts & Start Counter will be used: L1 Rate ~10KHz

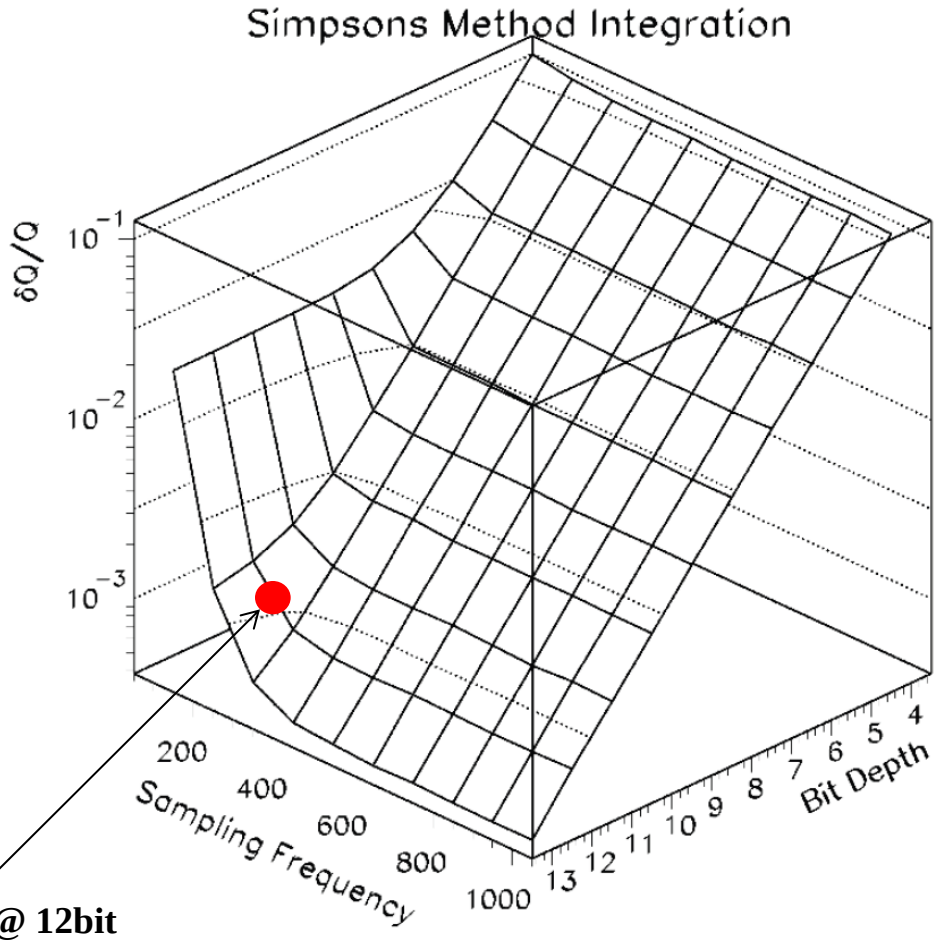
3.4 FADC Sampling – Charge Accuracy

Hall D FCAL PMT: FEU 84-3

-10,000 Random height pulses 10-90% full scale of ADC range simulated

- Sampling frequency makes little difference beyond 250MHz at 12bit, providing ~0.1% charge resolution

- PMT pulse shape dominates sample frequency and bit depth of ADC

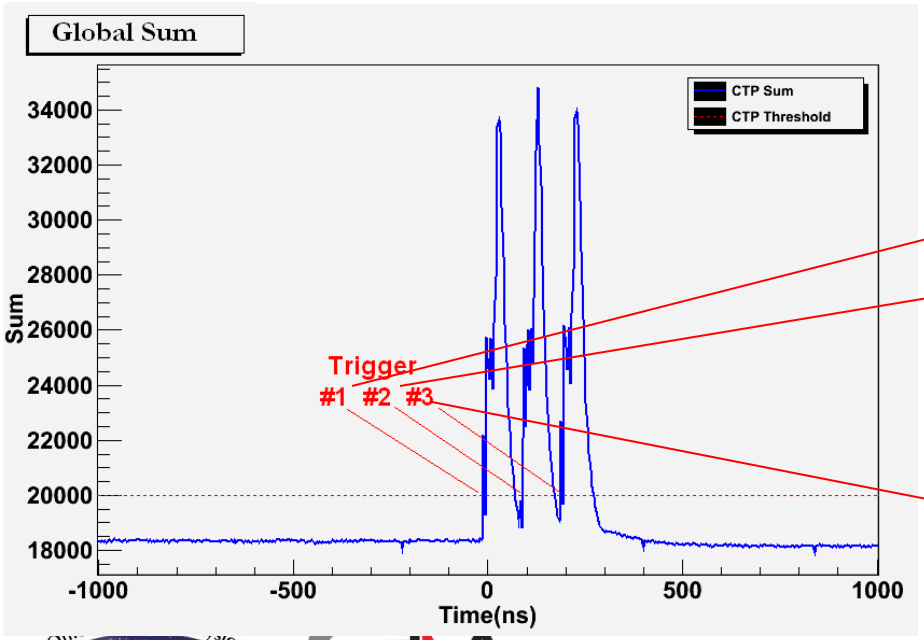


250MHz @ 12bit

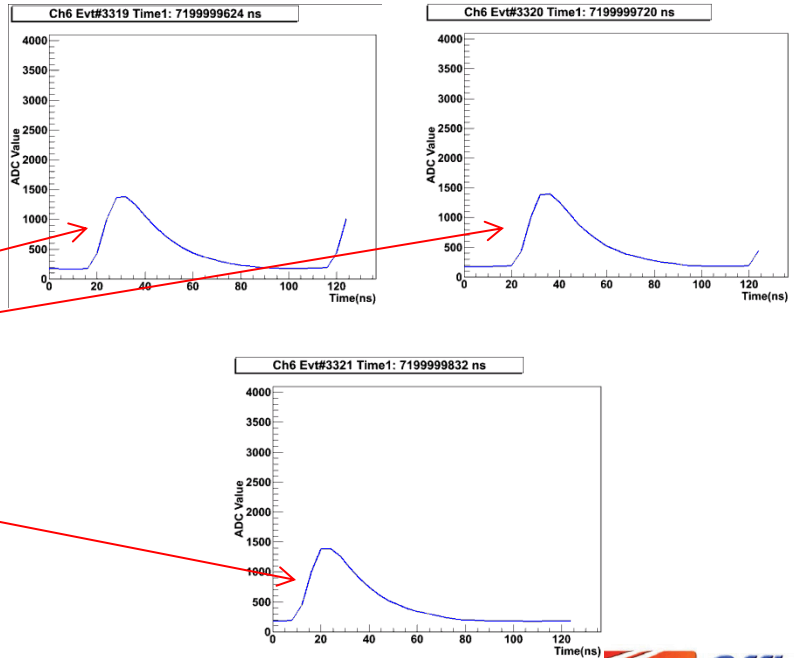
Synchronized Multi-Crate Readout

- CTP #2 is also acting as an SSP (by summing the local crate + CTP#1 sum over fiber
- A programmable threshold is set in CTP, which creates a trigger when the global sum (6 FADC boards => 96 channels) is over threshold.
- Example test with a burst of 3 pulses into 16 channels across 2 crates/6 FADC modules

A 2μs global sum window is recorded around the trigger to see how the trigger was formed:



Example Raw Event Data for 1 FADC Channel:



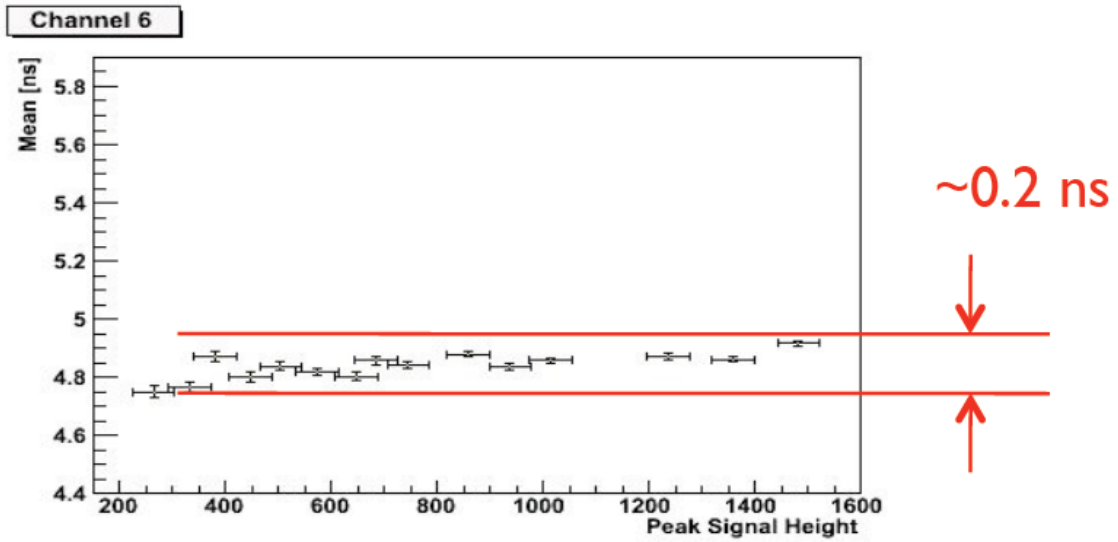
FADC Sampling – Timing Accuracy

Hall D FCAL PMT: FEU 84-3

-Timing algorithm developed & tested by Indiana University for the Hall D forward calorimeter.

- Implemented on the JLab FADC250 hardware achieving <300ps timing resolution on 50% pulse crossing time with varied signal heights.

- Resolution allow reliable information to link calorimeter with tagged electron bunch.



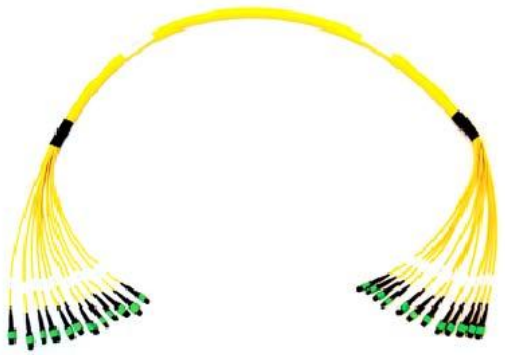
Typical timing resolution achieved ~1/10 the sample rate. The PMT shape will drive the ADC sample rate & depth requirements.

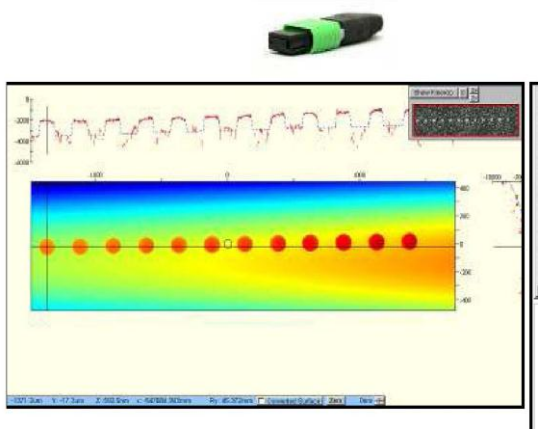
From: GlueX Doc# 1258-v1

Main Trigger Design Requirements

- 200kHz average (Hall D) Level 1 Trigger Rate, Pipelined with up to 8μs front end digitizer memory
  - High Luminosity -> $10^8\gamma$/s creates high average trigger rate
  - Initial commissioning at low beam current (~200nA). Luminosity - $10^7\gamma$/s
- L1 trigger supports pipelined subsystem hit patterns and energy summing with low threshold suppression
- Scalable trigger distribution scheme (Up to 128 crates)
  - Hall D: 25 L1 Trigger crates, 52 total readout crates
  - Hall B: 38 L1 Trigger crates, 56 total readout crates
  - Hall A & C will have < 2 L1 Trigger crates
- Low cost front-end & trigger electronics solution
- Strong FIRMWARE Features –
  - Hall B will use different programmable features than Hall D
  - Strong Partnership between Detector Groups and Firmware experts
  - Firmware "QA" control In Electronics/DAQ groups
  - Firmware can be remotely loaded to FPGAs from VME
- ALL Halls will benefit from new hardware design solutions

POP4 Avago Transceivers and MTP parallel fiber cable





-Fiber optic cable has been tested at 150m length

- **-Longest optic link is from Hall D to Hall D Tagger Is ~100m**

-Trunk lines will have 12 parallel ribbon fibers

- **-144 total fibers**
- **-Multi-mode 50/125um**
- **-MTP connectors to transceivers and patch panels**

Specifications:

Min insertion loss <0.60db
Wavelength 850nm (Avago POP4 Transceiver 3.125Gb/s)
Attenuation (db/km) - 3.5/1.5
Temperature range: -40C- 80C
Low Smoke Zero Halogen jacket – Non-Plenum tray approved

Specifications include installation and testing requirements
Each Hall will require different quantities and specific lengths
Patch panel hardware has been specified and tested