NPS Trigger/DAQ
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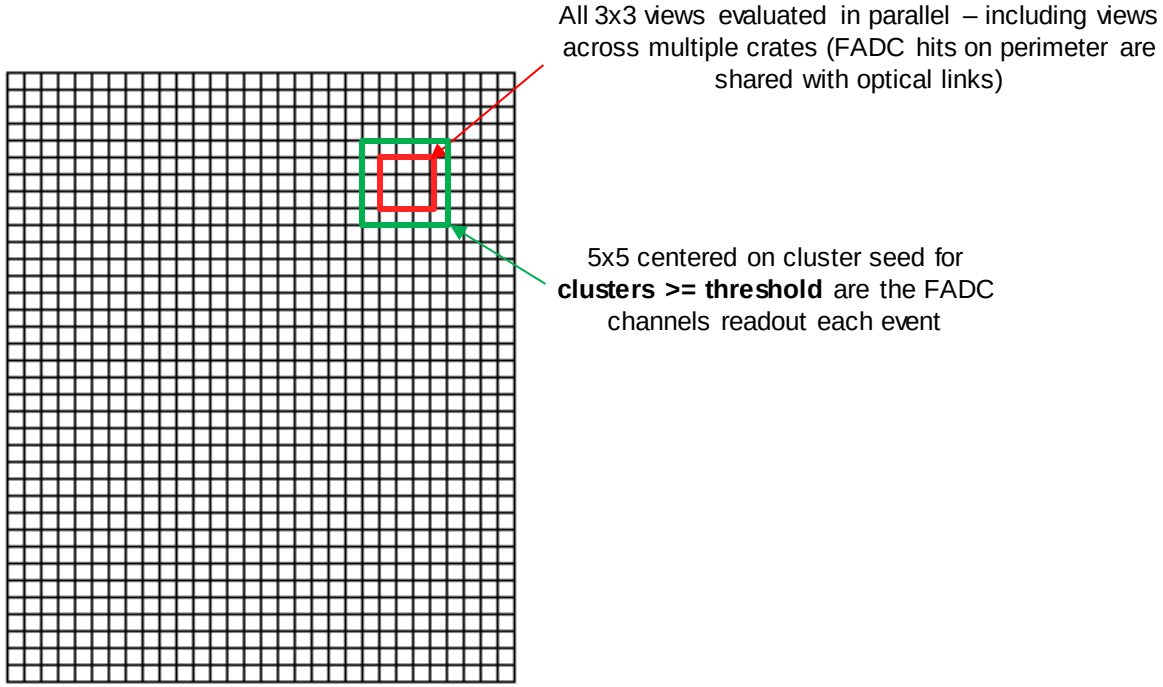
Benjamin Raydo
FEDAQ Group (Physics Division)

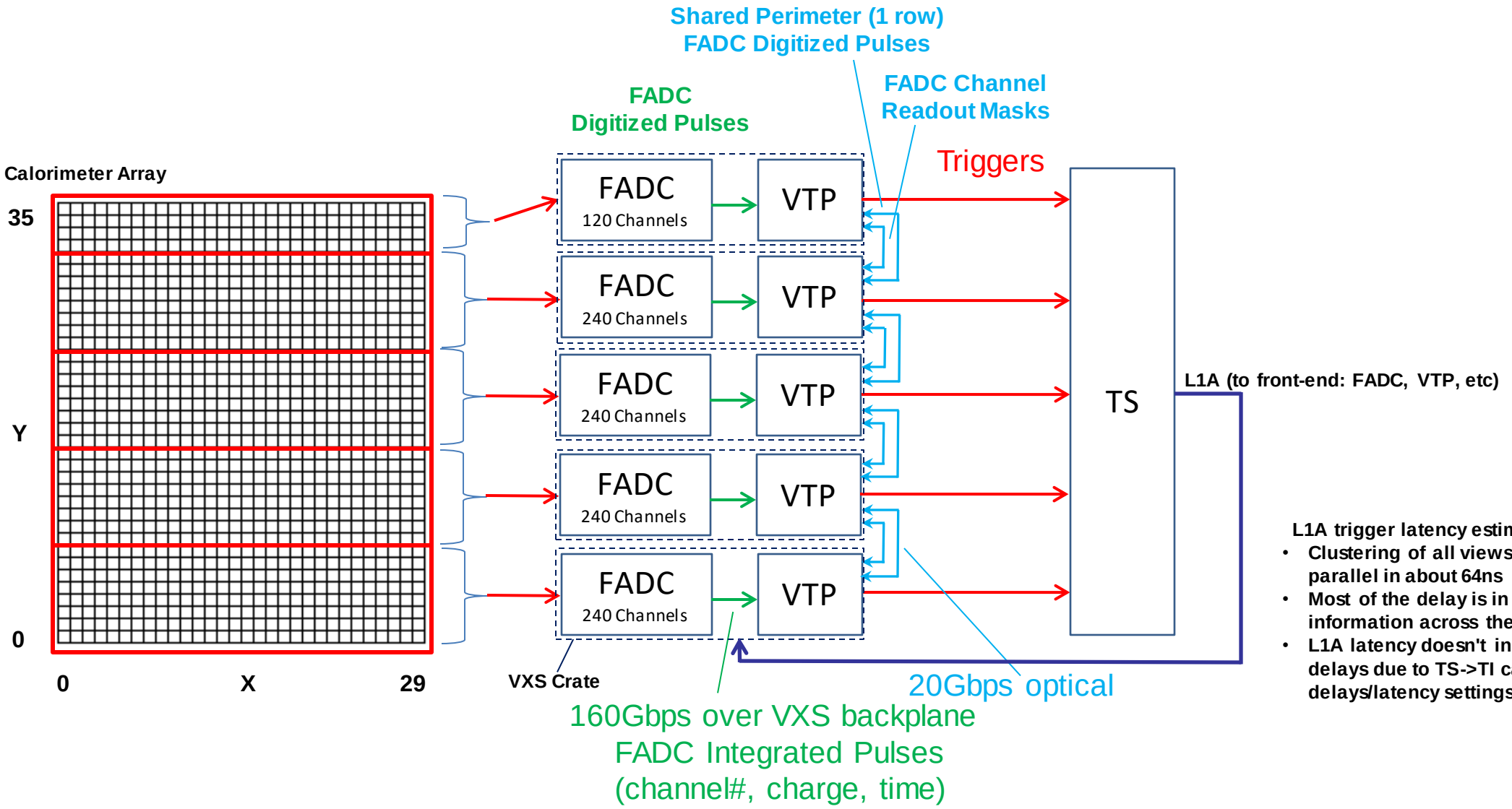
Clustered trigger & readout

Goals

- 3x3 clustering trigger across full calorimeter: trigger on **clusters>=threshold**
- 5x5 full waveform readout centered on triggered clusters



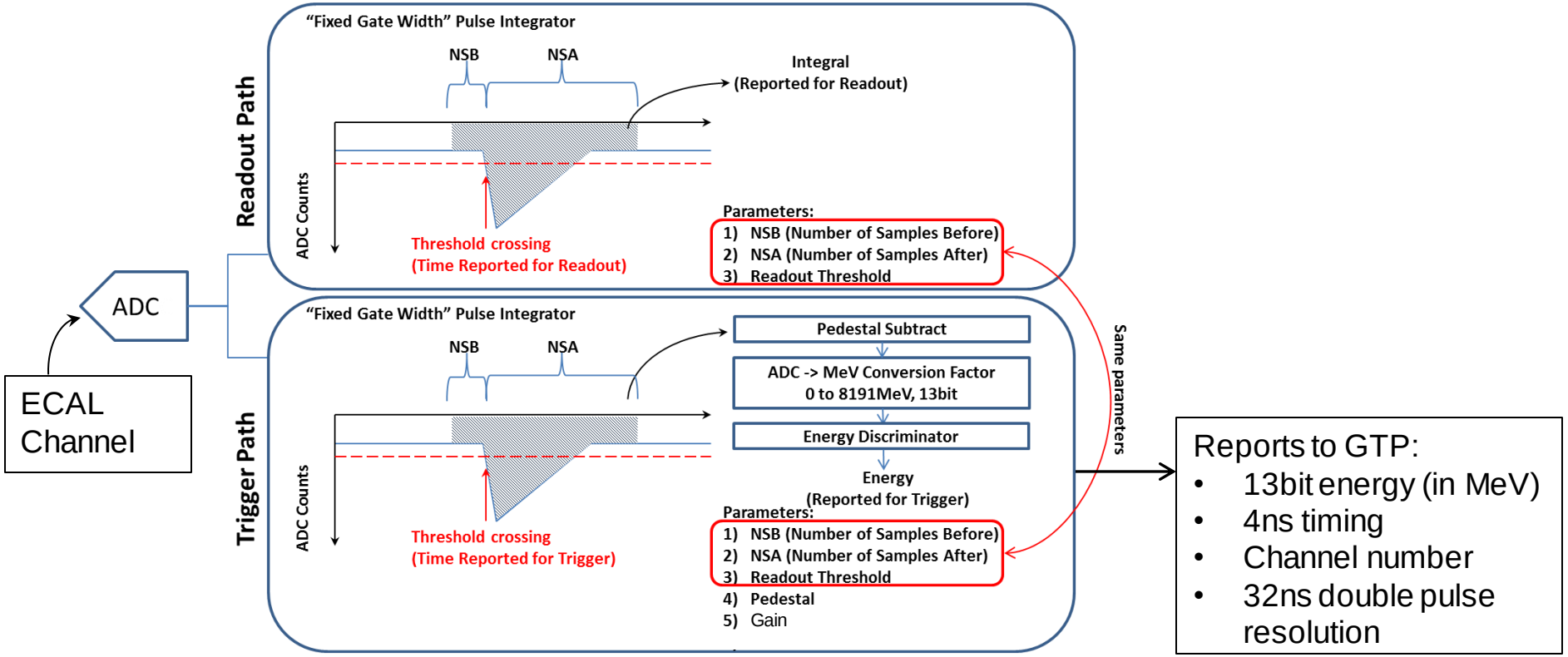
NPS Calorimeter DAQ/Trigger Setup



L1A trigger latency estimated around 1μs

- Clustering of all views happens in parallel in about 64ns
- Most of the delay is in transporting information across the serial links
- L1A latency doesn't include additional delays due to TS->TI cable delays/latency settings

FADC – Pulse Processing



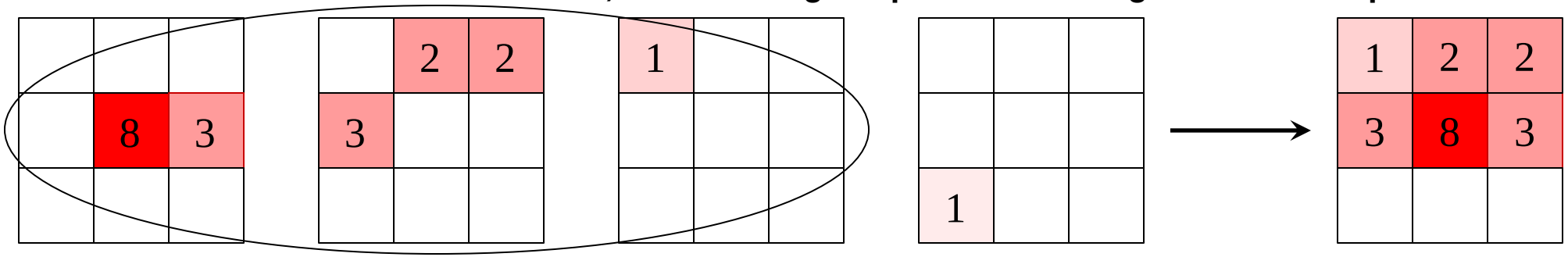
- Trigger pedestal is the same parameter that would be calculated for the readout data.
- Trigger gain parameter normally used to scale ADC -> MeV (makes VTP settings & diagnostics easy to read)
- Both pedestal and gain require calibration to determine parameters.

Cluster Finding

Cluster finding is done by (using 3x3 tower views, all views evaluated in parallel):

- **Seed hit (center) must be >= seed threshold**
- **Seed hit must also be a local maximum in both space and time**
- **Cluster is reported with:**
  - **Timestamp of seed hit (large amplitude hit => lowest jitter)**
  - **Number of hits in cluster**
  - **X,Y position of seed hit**
  - **Energy in MeV units**

e.g. for seed threshold of 2 and hit Δt=+/-8ns, the following hit pattern evolving in time will report 1 cluster:

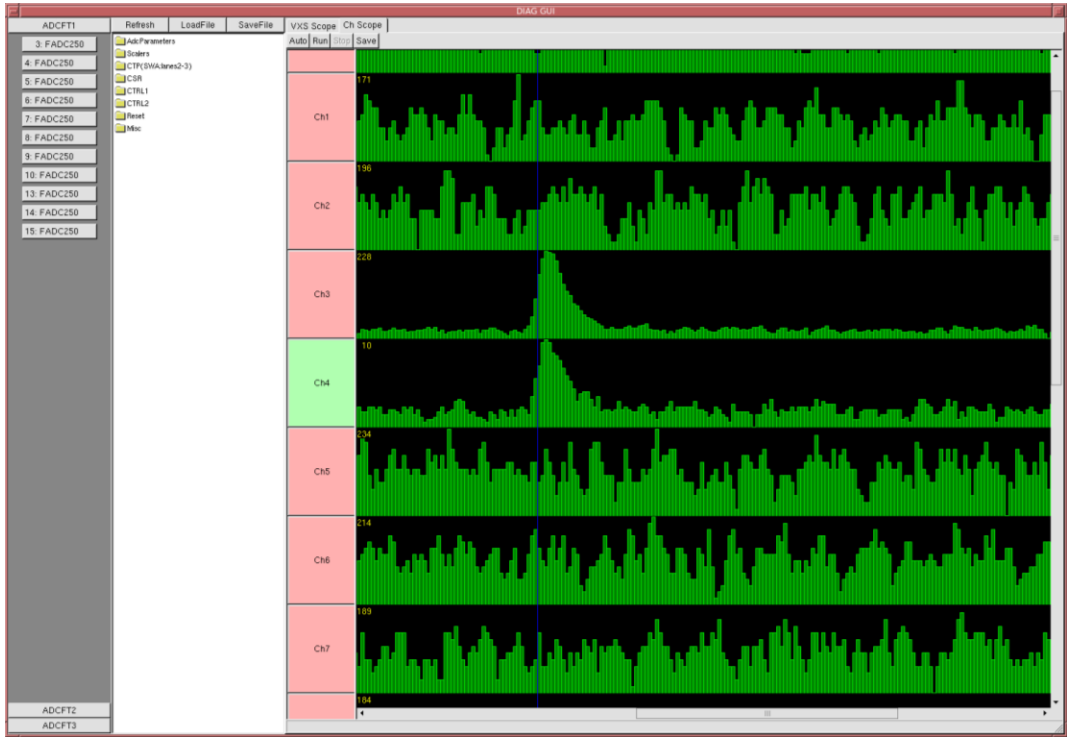


T=0ns T=4ns T=8ns T=12ns T=0ns, E=19, N=6, X, Y

DiagGUI – FADC250

DiagGUI is a general purpose tool to gain register access to DAQ modules and display various diagnostics, histograms, scalers, etc…

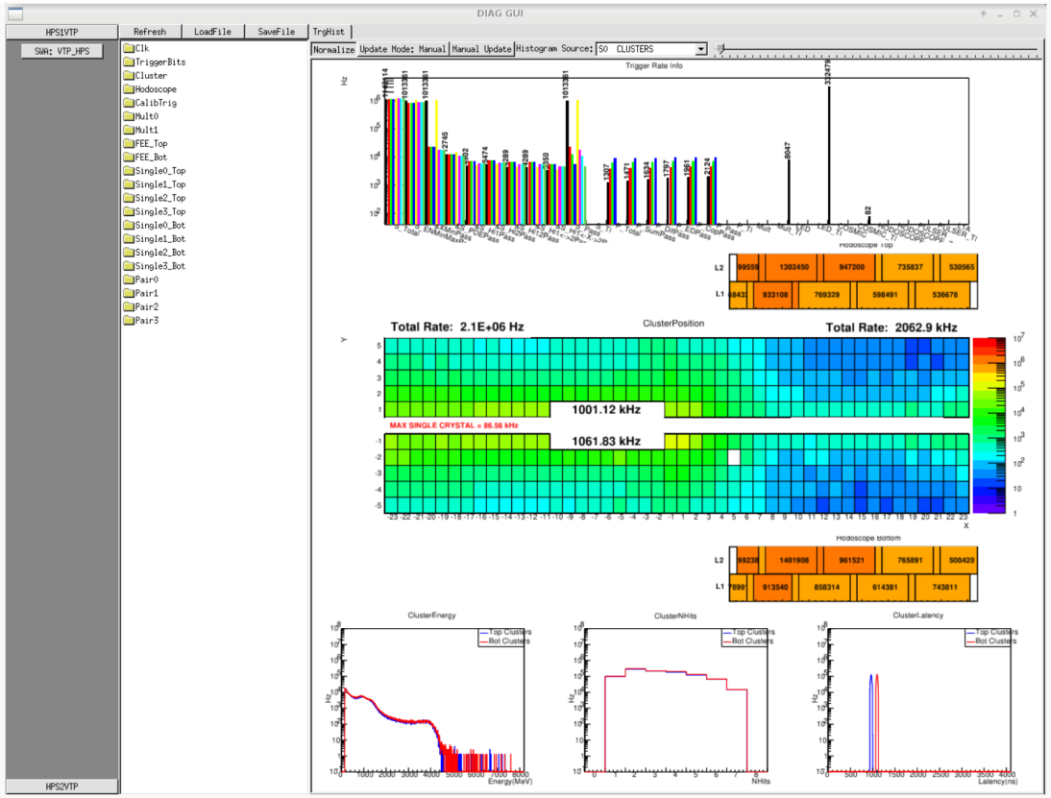
- **Runs parallel to DAQ operations...okay to view, but be careful as it allows changing module parameters on the fly! Really intended for 'expert' only.**
- **For example, you can look at any FADC250 waveforms and trigger on the channels:**



DiagGUI – VTP

On VTP, trigger features can be monitored (HPS calorimeter example shown)

- **Triggered cluster rates as function of position**
- **Cluster energy distribution, and number of hit crystals forming cluster**
- **Can select individual channels**



Trigger Configuration Files

Example/template trigger file (to be updated for NPS):

- **$CLON_PARMS/trigger/HPS/Run2019/TEST/hps_ben_test.trg**

Singles Setup:

```
# Enable trigger
VTP_HPS_SINGLE_EN    0                                1

# Minimum cluster energy: 1 to 8191, units MeV
VTP_HPS_SINGLE_EMIN  0     100                        1
VTP_HPS_SINGLE_EMAX  0    8191                        1
VTP_HPS_SINGLE_NMIN  0       1                        1

# Minimum cluster x coordinate: -31 to 31
VTP_HPS_SINGLE_XMIN  0     -31                        1

# Cluster position dependent energy threshold coefficients
# Cluster Energy >=     C0  + C1*X + C2*X*X+C3*X*X*X
VTP_HPS_SINGLE_PDE   0  1.0    1.0    1.0    1.0    1

# Hodoscope trigger
#                       require hit on l1
#                       |     require hit on l2
#                       |     |      require hit on l1 and l2 with geometry matching
#                       |     |      |      require hit on l1 and l2 with cluster X geometry matching
#                       |     |      |      |
#                       |     |      |      |
VTP_HPS_SINGLE_HODO  0  0     0      0      0      1
```

Trigger Data Banks

Enabled trigger bits and clusters are written to events

- **These allow online/offline checking of the trigger decisions**
- **...NPS format is slightly different than what is shown here ->**

```
O(31:23)=0x10+0x0C2 "HPS_CLUSTER"
   0(22:10)        "E"
   0(09:06)        "Y"
   0(05:00)        "X"
   1(13:10)        "N"
   1(09:00)        "T"

O(31:23)=0x10+0x0C3 "HPS_SINGLE_TRIG"
   0(22:20)        "INSTANCE"
   0(19:19)        "TOP_NBOT"
   0(18:18)        "H_L1L2X_GEOM_PASS"
   0(17:17)        "H_L1L2_GEOM_PASS"
   0(16:16)        "H_L2_PASS"
   0(15:15)        "H_L1_PASS"
   0(14:14)        "PDE_PASS"
   0(13:13)        "MINX_PASS"
   0(12:12)        "NMIN_PASS"
   0(11:11)        "EMAX_PASS"
   0(10:10)        "EMIN_PASS"
   0(09:00)        "T"
```

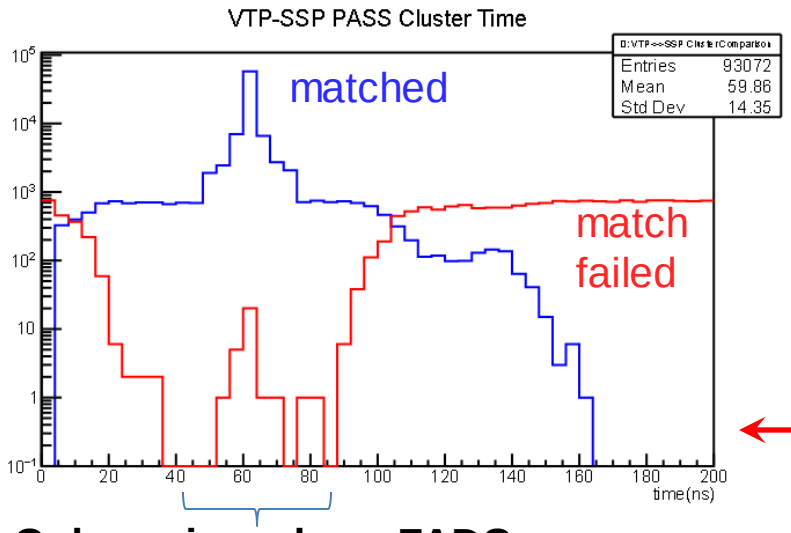
Firmware Simulation

VHDL, Verilog, C/C++ Simulator: Aldec Riviera

- Simulates source files used to compile FPGA projects
- Links to external libraries (e.g. C/C++ EVIO)
  - Can directly read and write DAQ EVIO files
  - Simulate firmware with runs and record new trigger bank structures
- Cycle accurate simulation of firmware
  - Some models are simplified for speed optimization (e.g. FADC trigger path & SerDes)
- Event simulation rate ~1Hz
  - Not very fast, but plenty can handle ~100k events in a day
- Can verify trigger logic
  - Can use cosmic and/or noise data from NPS calorimeter (before beam arrives)
  - Can use early beam data during commissioning for additional quick verification

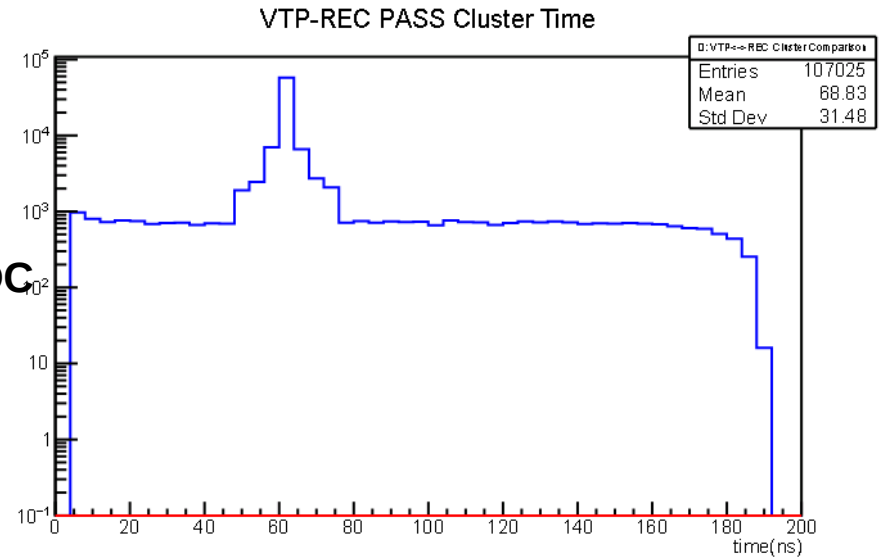
Cluster verification (from HPS)

Examples of comparing ~100k clusters (timestamp, energy, nhits, X, Y) of new firmware against HPS run 8099 trigger banks:



Only region where FADC waveforms are not clipped

- Less than 36ns and above 80ns the FADC waveforms are clipped by the readout window, so energy discrepancies develop causing VTP banks not to match SSP banks
- There are ~20 events that fail to match out of ~100k. These failures are due to pulse pileup creating dead-time on the FADC pulse detection in the trigger. Not easy or impossible to correct for, so this mismatch is not a surprise.
- Comparing VTP cluster banks to trigger emulator a 100% match is seen because both emulator and VTP see the same FADC waveforms (some which are clipped)



- Singles (old) and Pair trigger logic can be checked the same way (simulation is done, just need to run the analyzer to make the plots – will do soon)

Trigger Emulator

The trigger emulator is a basic ROOT based C++ analyzer

- Reads trigger banks and also reconstruct trigger banks from FADC waveforms
- Compares reconstructed trigger banks to recorded ones reports on discrepancies
- Measures/estimates rates of trigger bits from random trigger
  - A single random trigger run can be taken and fed through the program under various settings to tune parameters
  - These rates should match the running trigger bit rates as well – another good verification step
- Written for Hall B HPS – planning to update for NPS

Summary

- Trigger firmware is ready, but hardware testing is required (expected to happen in the next week or two)
- Simulation verification is completed (clusters trigger looks good)
- Need to implement the VTP FADC 5x5 channel mask readout firmware feature – will take a few days effort. Something expecting to do once cluster trigger is up and running