DAQ Hardware for Neutral Particle Spectrometer in Hall C

Brad Sawatzky

Needed Readout Hardware

- **NPS: 1080 PbWO$_4$ blocks**

  - → **Need to incorporate a TS module to handle additional ROCs (we have one)**

    - » **May need more 'DAQ fiber' SHMS ↔ CH**

  - → Energy / ADC:

    - » 67x   FADCs
    - » 5x   VXS crates
    - » 5x   SD + TI + Linux SBC / ROC

  - → If FPGA NPS trigger, then add

    - » 1 VXS crate, 1 TI, 1 Linux SBC
    - » 5x CTP, 1x SSP, (no GTP needed, I think…)
    - » +Firmware development
    - » +more time if fully-pipelined w/ HMS *vs* 'hybrid' trig

  - → Timing / TDC (resolution?)

    - » ~ 1 ns OK? use FADCs (no cost)
    - » ~0.1 ns required, then
      - – 10x VME CAEN 1190 TDCs (100ps/bin)
        - » can re-purpose SHMS DC modules
      - – + Splitters (needed)
      - – + Discriminators (CAMAC?)

- **Available from SHMS:**

  - → Energy / ADC:

    - » 16x   FADCs
    - » 1x   VXS crates
    - » 1x   SD + TI + SBC

  - → TDCs (if needed)

    - » 10x CAEN 1190

- **Spares inventory**

  - » **Will pull a little from here, but <u>will not</u> drain spares pool**
  - → 2–3x CAEN 1190s
  - → 5–6x F250s
  - → 3–4x SD, TI, SBC
  - → 2x   VXS crates
   - » 1 in hand, 1 on order

Needed Readout Hardware

- **NPS: 1080 PbWO$_4$ blocks**

  - → **Need to incorporate a TS module to handle additional ROCs (we have one)**
    - » **May need more 'DAQ fiber' SHMS ↔ CH**

  - → Energy / ADC:
    - » 67x   FADCs
    - » 5x   VXS crates
    - » 5x   SD + TI + Linux SBC / ROC

  - → If FPGA NPS trigger, then add
    - » 1 VXS crate, 1 TI, 1 Linux SBC
    - » 5x CTP, 1x SSP, (no GTP needed, I think…)
    - » +Firmware development
    - » +more time if fully-pipelined w/ HMS *vs* 'hybrid' trig

  - → Timing / TDC (resolution?)
    - » ~ 1 ns OK? use FADCs (no cost)
    - » ~0.1 ns required, then
      - – 10x VME CAEN 1190 TDCs (100ps/bin)
        - » can re-purpose SHMS DC modules
      - – + Splitters (needed)
      - – + Discriminators (CAMAC?)

- **Need to Aquire**

  - → Energy / ADC:
    - » +51x   FADCs (*)
    - $350k(*)$ » +3x   VXS crates
    - » +3x   SD + TI + SBC

  - → if FPGA NPS trigger
    - » +1 VXS cr., +1 TI, +1 SBC
    - $45k   » +4x CTP/VTP

  - → Timing / TDC (high resolution)
    - » ~0.1 ns
    - ??   – + Splitters
    - ??   – + Discriminators

- VXS Crates and support modules are in the Hall C purchase plan/schedule

- (*) F250s are assumed to be provided by Physics Division/ Fast Electronics group
  - → PR for ~40+4 units (PD+HC) approved Jan 2019

Rackspace in SHMS hut

- 4+1 VXS crates + 2 High Voltage crates
  - → It's pretty snug, but it'll fit...
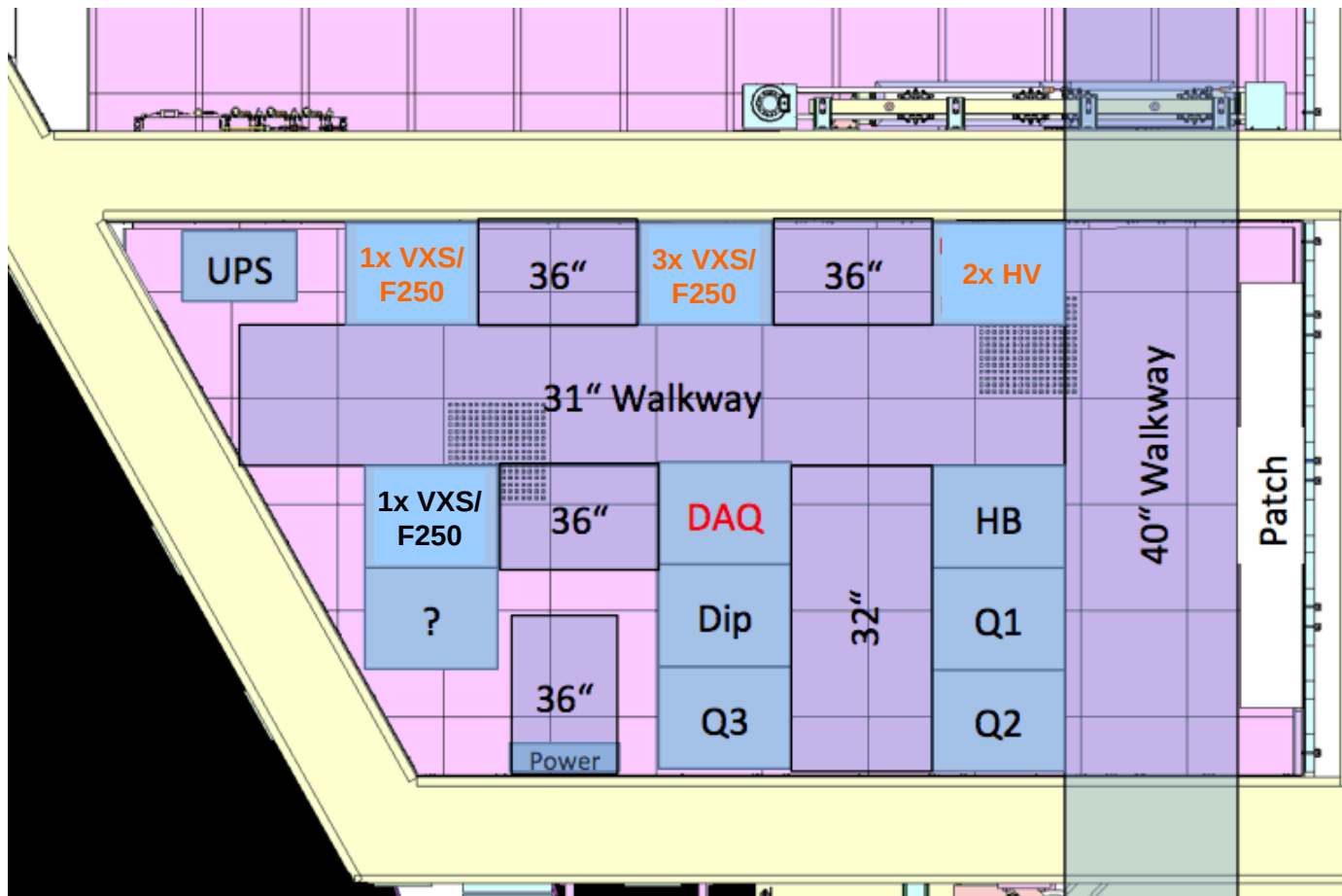
HV / Slow Controls / Cabling

- High Voltage – TBP
  - → High Voltage (-1.6kV @ < 1 mA base draw)
    - » 2x CAEN SY4527 Chassis
    - » 2x CAEN A4532 Booster (600→1200W)
    - » 26x CAEN 7030N Cards (48ch, 1mA max/ch)
  - → $175k (recent quote)

- LED Control / Logging?
  - → EPICS?
  - → Cabling?

- High Voltage Cables (2 sets) – TBP
  - → Multi-conductor cabling 48 ch/cable
    - » NPS roof patch →
    - » Patch panel rack on SHMS carriage near pivot →
    - » SHMS detector hut (HV crates)

- Signal Cables (2 sets) – TBP
  - → RG58 or RG-174?
    - » NPS roof patch (LEMO) →
    - » Patch panel rack on SHMS carriage near pivot (BNC) →
    - » SHMS detector hut (LEMO)

- Patch cables (3 sets) – TBP
  - » Only significant burden if CAEN TDCs are needed
  - → RG-174 (LEMO/LEMO)
    - » Splitter → Discrim → TDC
    - » Splitter → FADC

Jefferson Lab

Data Rates / Compute Resources

- **Data rates / Compute resources (from OLD documents, I think...)**
  - → **Singles Rates:**
    - » NPS documents suggest 1—12 kHz HMS singles rate (few kHz 'typical')
    - » ~200 kHz / NPS crystal (@ 1uA on 10 cm LH2)
  - → **Data rate:**
    - » ~4% random occupancy in 200 ns window (NPS doc suggests 200—300ns range)
    - » ~2.5 kB/trigger * L1A rate → 2.5 MB/sec @ 1 kHz   (no problem)

- **General considerations:**
  - → 20 MB/sec (sustained) is fairly "straight forward"
    - » ensure the online analysis software keep up with monitoring/debugging requirements
    - » all physics analysis (even semi-prompt "online" summaries) should be done by the Farm
      - – ie. "Qweak-mode", closer to Hall B's workflow than conventional Hall A/C workflow
      - – recommend a "data challenge" to make sure software is ready
  - → 200+ MB/sec (sustained!) requires investment (ie. 100% occupancy, 300ns window @ 1 kHz)
    - » big local disk buffers, dedicated disk arrays, fat pipes to SciComp, lots of redundancy
    - » the entire chain from VME crate(s) to tape must be capable of this sustained rate
   - » IT/SciComp needs to be in the loop so they are ready

Data Rates / Compute Resources

- **Data rates / Compute resources (from OLD documents, I think...)**
  - → **Singles Rates:**
    - » NPS documents suggest 1—12 kHz HMS singles rate (few kHz 'typical')
    - » ~200 kHz / NPS crystal (@ 1uA on 10 cm LH2)
  - → **Data rate:**
    - » ~4% random occupancy in 200 ns window (NPS doc suggests 200—300ns range)
    - » ~2.5 kB/trigger * L1A rate → 2.5 MB/sec @ 1 kHz   (no problem)
- **General considerations:**
  - → 20 MB/sec (sustained) is fairly "straight forward"
    - » ensure the online analysis software keep up with monitoring/debugging requirements
    - » all physics analysis (even semi-prompt "online" summaries) should be done by the Farm
      - – ie. "Qweak-mode", closer to Hall B's workflow than conventional Hall A/C workflow
      - – recommend a "data challenge" to make sure software is ready
  - → 200+ MB/sec (sustained!) is non-trivial   (ie. 100% occupancy, 300ns window @ 1 kHz)
    - » big local disk buffers, dedicated disk arrays, fat pipes to SciComp, lots of redundancy
    - » the entire chain from VME crate(s) to tape must be capable of this sustained rate
- **Firmware / FPGA trigger development is NOT an outside project**
  - → "Contract" with the JLab FE group and have them handle this subproject
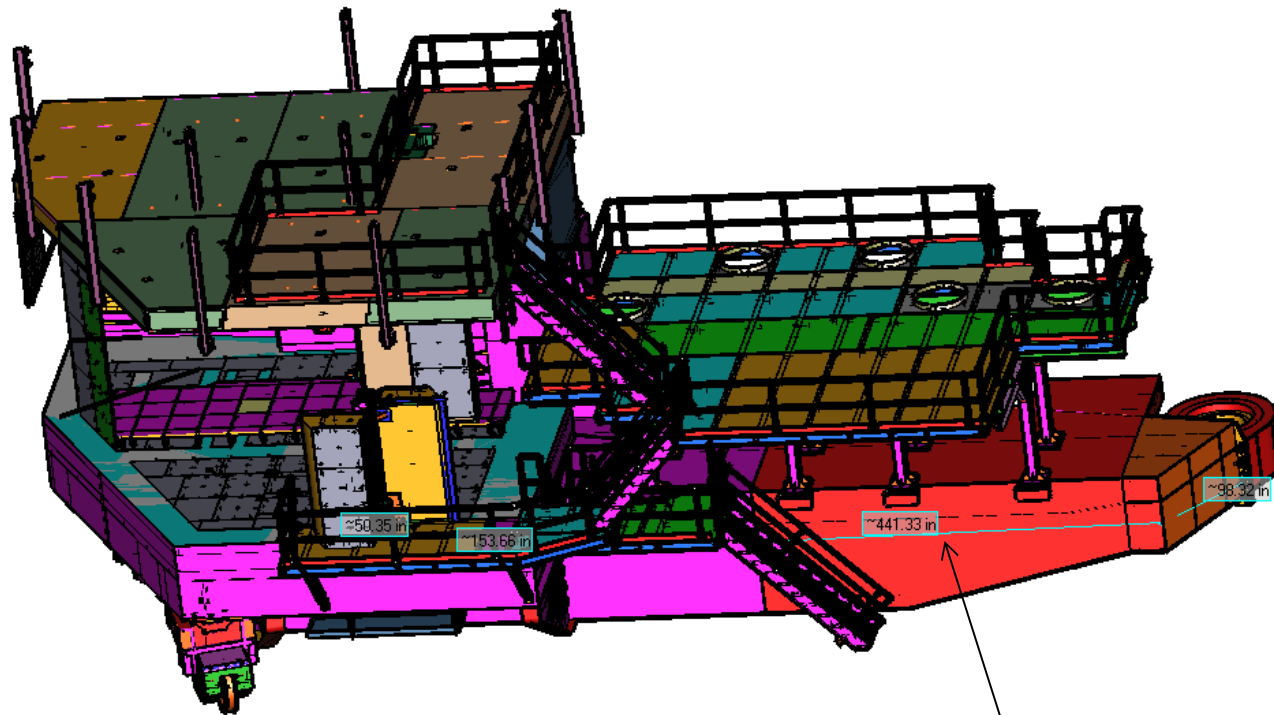 - → Many, many devils are in the details + hard to debug → Stay away

Backup Slides

~98.32 in

~153.66 in

~50.35 in

~441.33 in
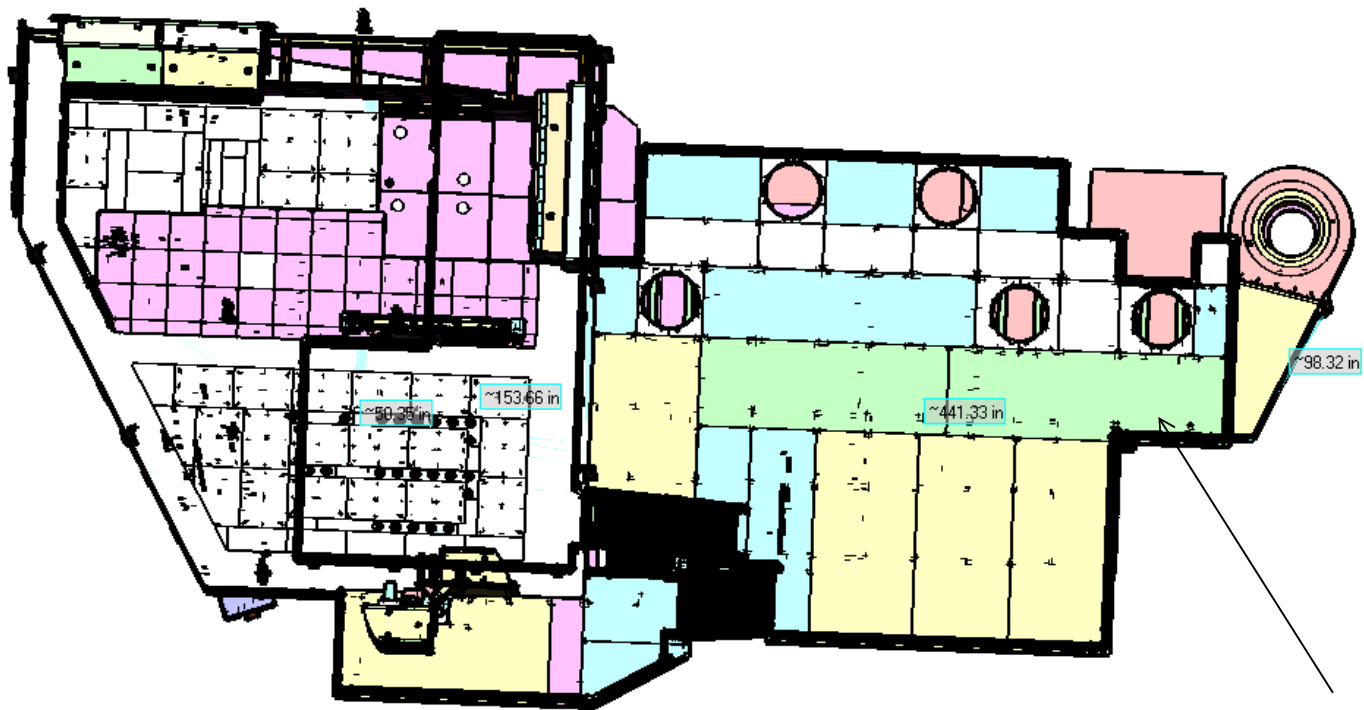
Patch panel here?
(next to small crane)

~50.35 in ~153.66 in ~441.33 in ~98.32 in

Cable run here?

SHMS "pivot-patch" cable run


Experiments: NPS, LAD(?), CGEN(?)

1200 HV cables (NPS-driven others are less)
 - RG59 : 0.242" OD; 0.023 lbs/ft
 - 72 in2 + overhead
 - Cable tray: nominal 24" wide 4--6" tall tray
 - fills 1--2 penetrations

1200 RG213 cables
 - Diam: 0.405" OD,
 - Weight: 0.115 lbs/ft
 - Sig Sp: 66%
 - Termination of old cables?
 - reterminate at least one end -- cost?

 - Cable tray:
   - 200 in2 + overhead
   - nominal 30" wide 10" tall tray
   - nominal 24" wide 12" tall tray

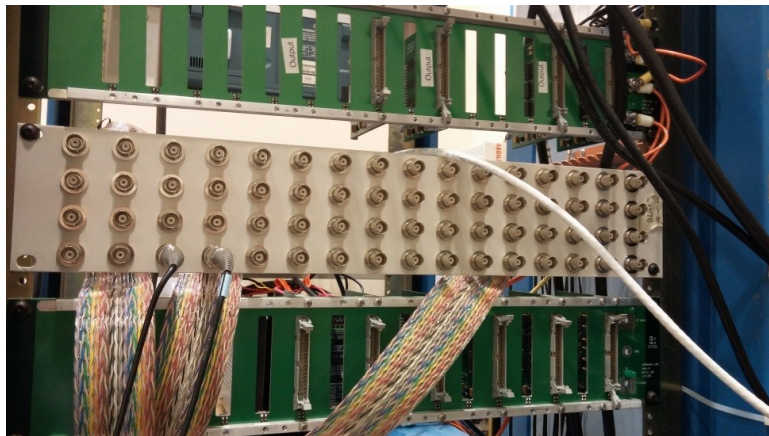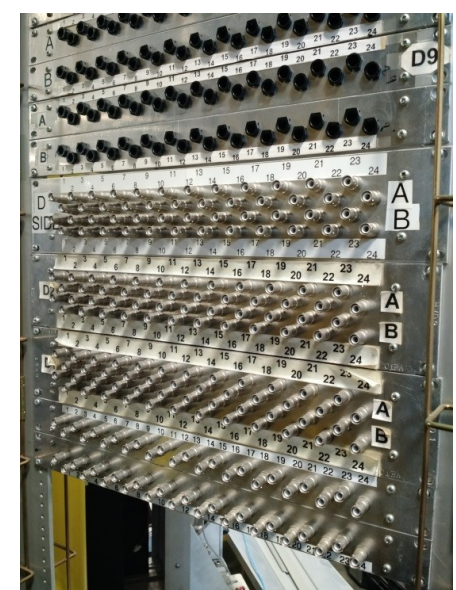 - fills 3--4 penetrations   1200 RG58 cables only 1-2 penetrations
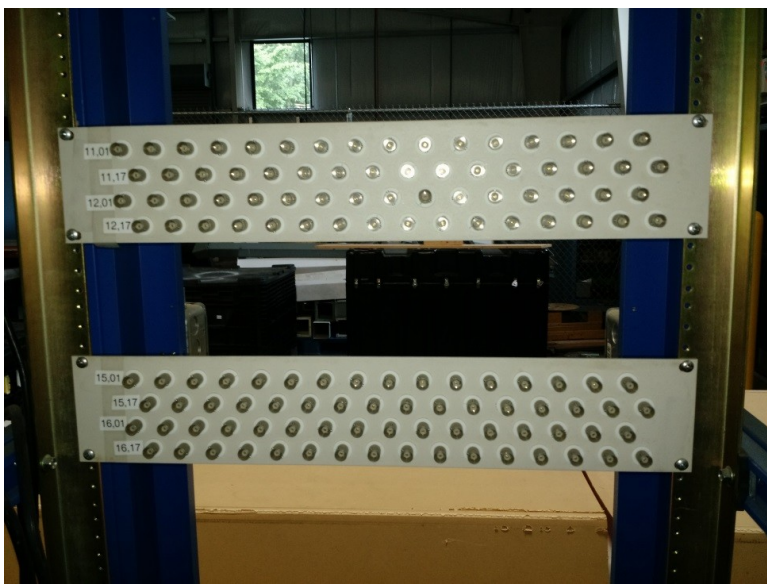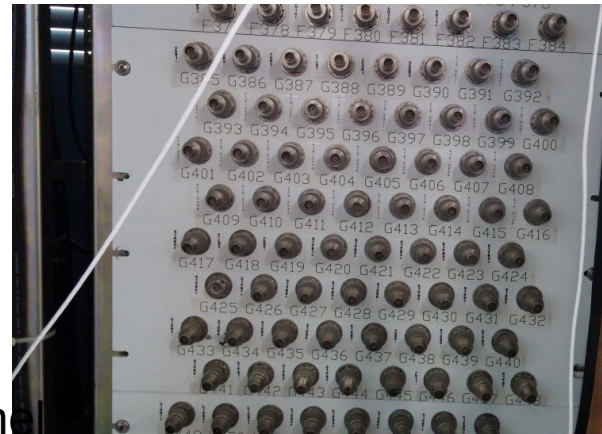
High density BNC patch

High density HV breakout panel (BETA weldment in ESB)

Like this 64 cables on 3.5 inch high panel
Can fit over 1200 cables in one rack

like HMS: Here can fit at best 5 times 64 cables in rack