EEEMCAL General Meeting – 9 August 2024

- ❑ Prototype beam test planning
- ❑ Initial discussions about space/assembly planning
- ❑ TDR – first draft by and of Sept
- ❑ Other

EEEMCAL Readout Chain Prototype Tests 2024

- Goals of the beam test: engineering articles test
  - Test if ASIC gives comparable result with fADC - investigations of stability, linearity, and power deposition
  - Determine what is the minimum energy that can be detected with both sets of electronics
  - Mechanical aspects: carbon frame impact on resolution

- Three PWO prototypes
  - MIT – comparison PMT and SiPM (3015)
    - 2 channels will be instrumented with SiPM
  - IJCLab-Orsay – comparison of readout chains and test mechanical items
    - All 25 channels will be instrumented with SiPM
  - Crytur-USA – compare a different readout

- Personnel – confirm names with Douglas
  - AANL: Artur
  - Crytur-USA: 2 people (Sylvia,)
  - CUA: 1-2 people
  - IJCLab-Orsay: 2 people
  - Lehigh: Tristan
  - MIT: Douglas, Ethan, Ivica (Zagreb, 1 week)
  - OU: Justin?

Preparations for EEEMCAL Readout Chain Prototype Tests 2024

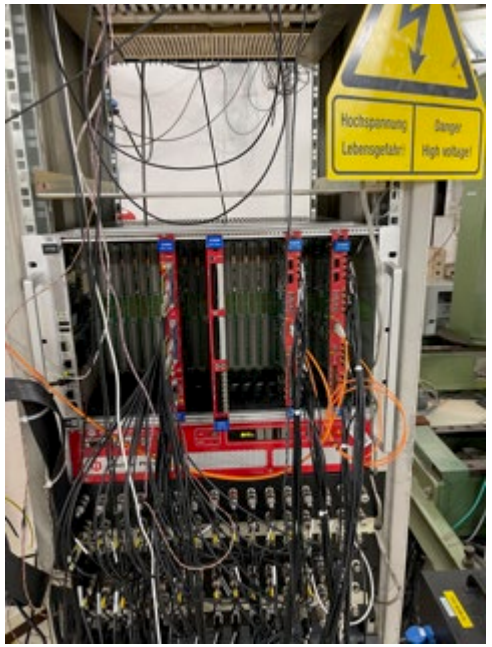
- ✓ ❑ Radiator (Summer 2024): CUA, JMU, UKY, …
  - ✓ ○ Start setting up test benches at JMU and UKY – JMU nearly done, UKY-CUA visit on 29 July
  - ✓ ○ Ship crystals to, e.g., IJCLab-Orsay – 30 crystals shipped from CUA and arrived early August
- ❑ SiPM and readout chain (Summer 2024): ACU, OU, …
  - ✓ ○ Decision on pixel pitch – 15um, 3mm x 3mm
  - ✓ ○ Purchase SiPMs: to instrument with 4 SiPM/crystal need: 100 SiPMs for a 5x5 array (IJCLab-Orsay prototype)
  - ○ Complete PCB board development: two 16 (3 x3) SiPM designs; parallel and independent (has SiPM and mezzanine board)
  - ○ Test PCB board
  - ○ Materials survey (e.g., for discrete: fADC, VME crate, LV supply, amplifier+cables, LV and bias cables, oscilloscope, , etc.)
  - ○ Ship materials to DESY (→ MIT ships end of September)
- ❑ Mechanical Construction: IJCLab-Orsay, MIT
  - ○ Wrapping crystals with reflector
  - ○ Construct prototype
  - ○ Materials survey (HV/signal long cables, alignment materials, oscilloscope, , etc.)
  - ○ Ship materials to DESY (→ MIT ships end of September)
- ❑ Simulations: UKY, AANL, …
  - ○ Geometry and material
  - ○ Digitization
- ❑ Cosmic Test: IJCLab-Orsay, …
  - ○ Demonstrate working prototype on test bench: Light yield with SiPM readout (PCB + boards)
- ❑ Data acquisition and analysis
  - ○ Any special requirements?

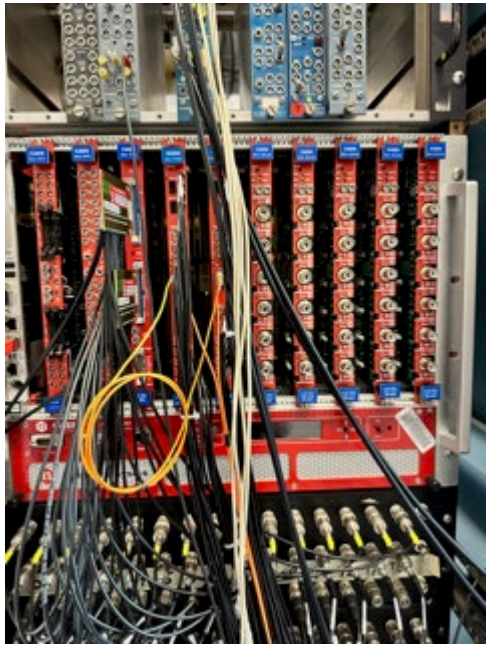
MIT 5x5 Prototype Materials List

- (From Douglas) MIT would bring/ship these to DESY for the beam test:
  - the 5x5 PbWO4 calorimeter plus 5 spare crystals and spare PMTs and ESR foil.
  - LeCroy 1458 HV Mainframe and a number of -HV and +HV pods. The PMTs typically take ~-1000 V at room temperature.
  - VME crate with controller, 32 channel CAEN QDC (V792), and two 16 channel CAEN Digitizers (V1725S, 14 bit 250 MHz)
  - splitter panels if you want to run QDC and Digitizer in parallel
  - 100’ of signal cables (need the length to delay signal until trigger electronics is ready to give trigger)
  - HV cables
  - fibre optic cables
  - chiller ? (I don’t think you will want to cool the calorimeter too much but maybe a stable temperature is useful at 15 - 25 C can use just water as the recirculating fluid). Transformer for German power.
  - a trigger scintillator with PMT
  - one or two computers with monitor, key board, etc.
  - toolbox and various odds and ends
- Pictures of the setup:
  https://wiki.jlab.org/cuawiki/images/a/a7/20240405_DESY_TB.pdf

MIT 5x5 Prototype Readout

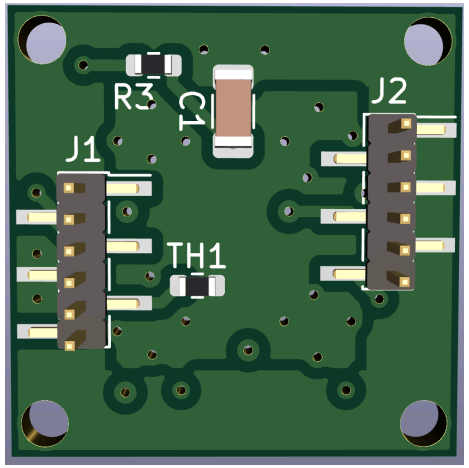
- The MIT readout consists of:
  - One (1) CAEN V792 - QDC, 12 bit, 32 channels via adapter board from ribbon connector on module to individual Lemo cables (see images)
  - Two (2) CAEN V1725S - Digitizers, 14 bit, 250 MS/s each with 16 channels input via MCX connectors to Lemo cables, optical fibre readout (see first image)
- Also in the first image are two (2) 50 ohm splitter boards, 16 channels input, 32 channels output BNC with Lemo adapters. I'll ship four (4) such splitter boards.
  - This image is from our old configuration where we also had a NIM crate with the trigger logic and a huge LeCroy mainframe HV unit.
- The new configuration is shown in the second image.
  - One (1) CAEN VME crate with:
    - one (1) CAEN V4718 crate controller/bridge (not pictured, this just arrived this week),
    - CAEN V812 CFD module 16 channel,
    - CAEN V976 quad logic AND/OR/MAX module,
    - V792 (described above),
    - two (2) V1725S (described above), and
    - five (5) CAEN V6533N 6 channel HV modules, SHV connectors.

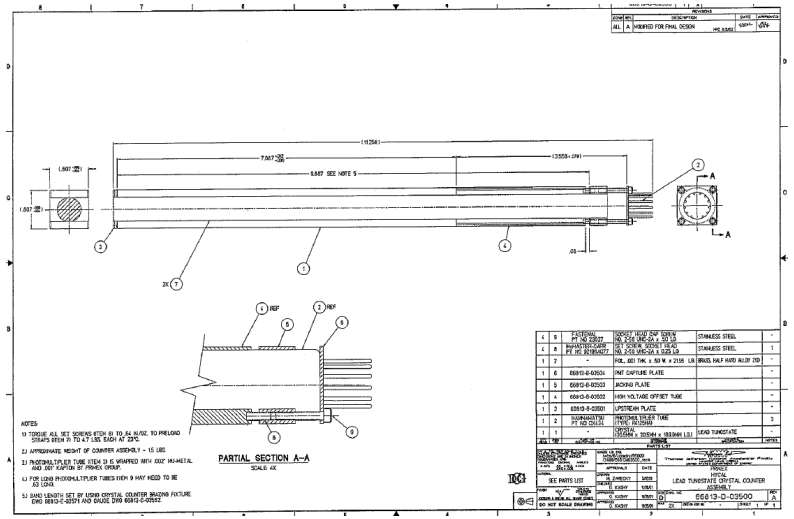




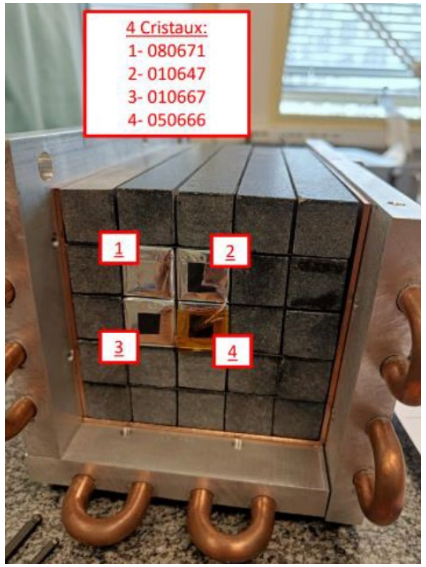
Two channel SiPM for MIT 5x5 Prototype

- ❑ Plan is to have a pre-amplifier circuit that will match the gain of the SiPMs to the gain of the PMTs before feeding the signals into the rest of the MIT prototype readout.
- ❑ (Larry) Reworking the pre-amplifier board to match with the mounting piece from Josh and assemble 2 SiPM and 2 pre-amp boards to be sent to JLAB by the first week of September.
  - will include the short cable that ends in an SMA connector and 2 power cables.
  - How long does the power cable need to be? will check to see if I have two SMA to BNC cables that are about 2 feet long that I can also send with the boards.
  - Expected wires from each board: 1 BNC signal cable, 3 twisted pairs (6 wires total) for HV, ground, +5, -5, and thermistor connections. 1 cable to interface with the LED
  - power and thermistor cable should be shielded. May have enough of a cable like this to make a couple 5-10 foot cables. Is this the best option or do we need to make a longer cable or different type of cable for these connections?
- ❑ (from Larry) Needed at DESY – could be provided by IJCLab-Orsay supplies:
  - 2 channels of bias voltage at about 42V
  - +5V supply (~30 mA needed total for both boards)
  - -5V supply (~30 mA needed total for both boards)
- ❑ (Josh) Working on assembling materials for mounting
- ❑ Ship to MIT before end of September or directly to DESY

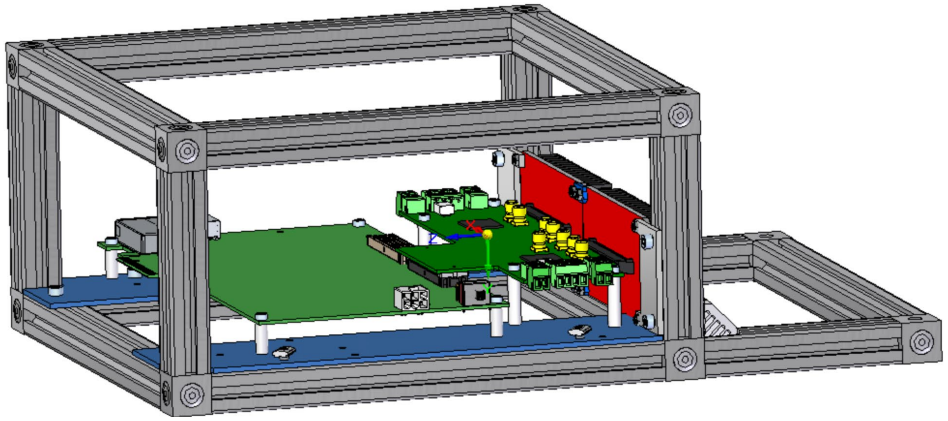


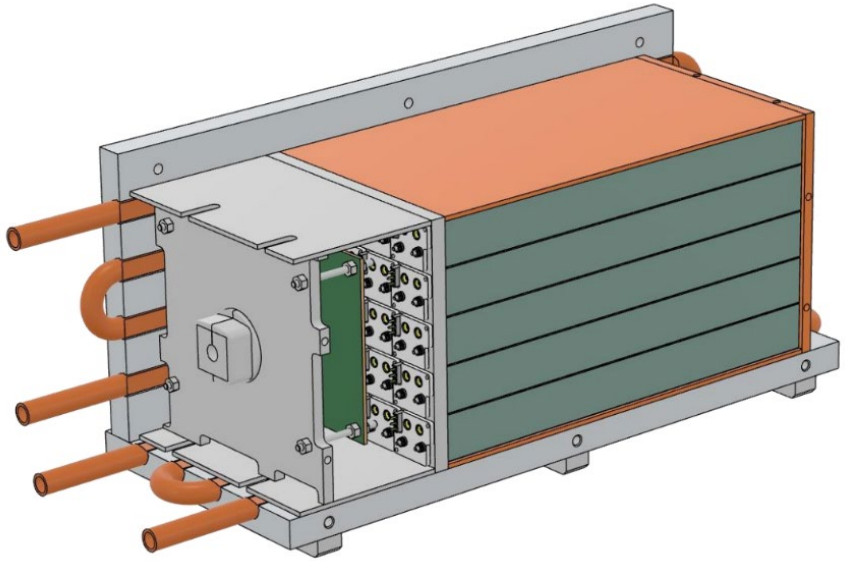


IJCLab 5x5 Prototype Materials List



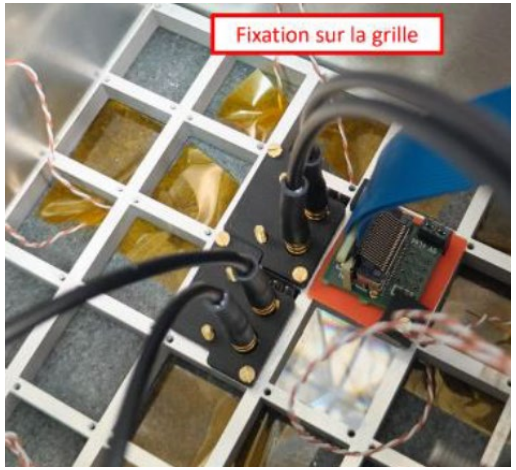
- ❑ IJCLab would bring/ship these to DESY for the beam test:
  - the 5x5 prototype (currently not yet instrumented with crystals and SiPMs)
  - 30 PWO crystals (received from CUA)
  - HGCROC readout frame (protoboard, KCU, adaptor board)
  - Power supply (Keithley module that will be used to power the HGCROC boards and provide bias to the SIPMs) - could also be used to instrument two SiPM channels on the MIT prototype
  - Oscilloscope
  - 16-channel wavecatcher (flashADCs) unit
  - Chiller (and hoses)
  - Linux laptop
- ❑ Note on the LED: no plans to operate it for this upcoming beam test.

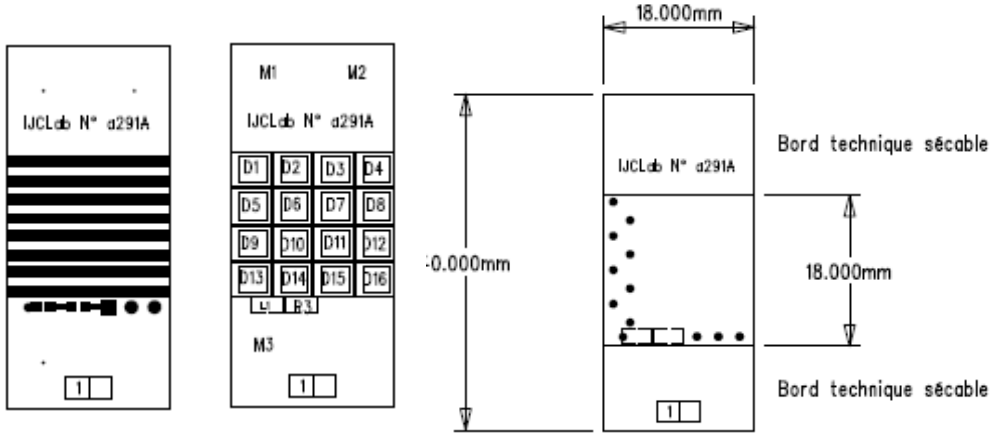




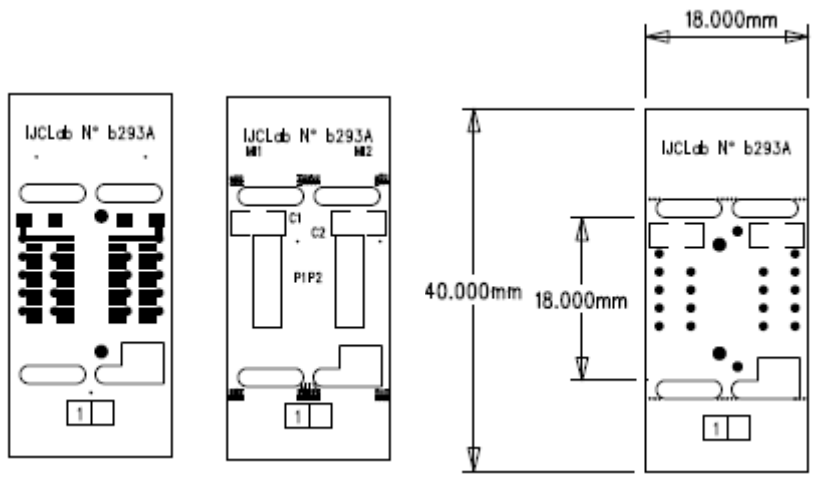
“Discrete” (fADC) Readout on IJCLab 5x5 Prototype

- IJCLab-Orsay 2 designs for the PCBs: one where we read all 16 (3x3 m2) SiPM in parallel and one where we read all 16 SiPM independently
- A new version of the board will be ready soon
  - Main difference to previous version: separation of the SiPM cathodes
  - Another change: A thermistor is being added to the board
- To implement the “discrete” (fADC) readout need to design a mezzanine board – Larry/Gerard are working on that





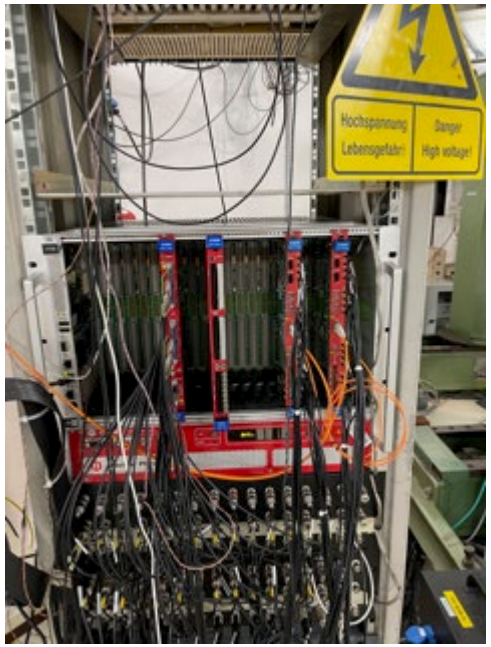
Parallel design

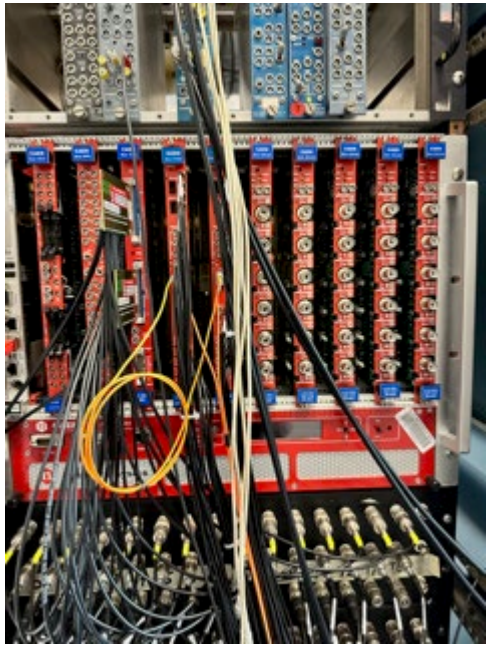


Independent design (SiPM + mezzanine board)

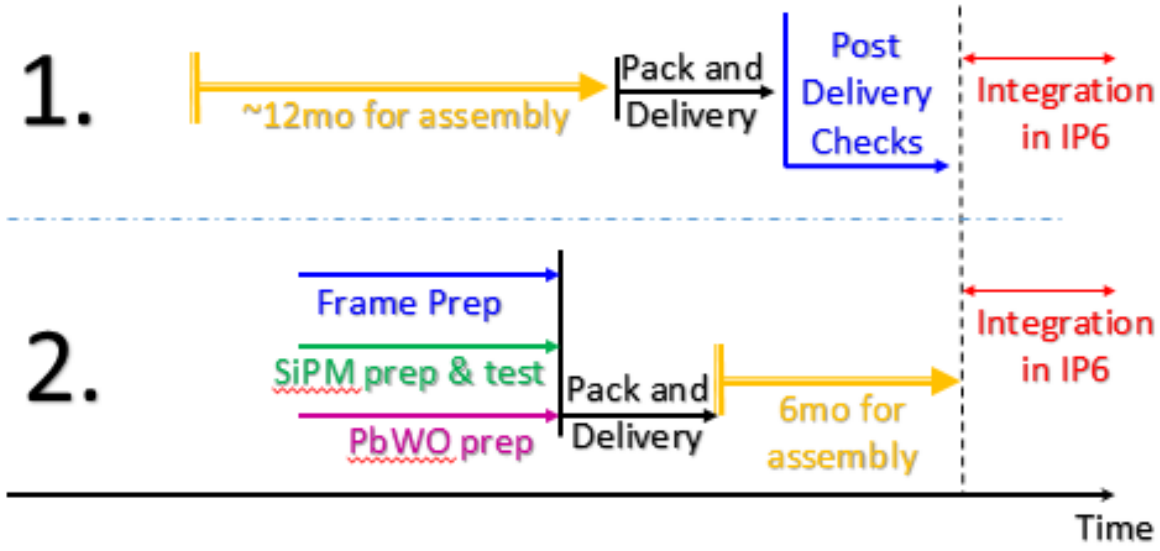
“Discrete”/fADC using the MIT 5x5 Prototype Readout

- (From Gerard) The MIT CAEN V1725S's will serve excellently for waveform readout of SiPM's. (Assuming the waveform readout firmware is the plan, is that right?) What is planned for the communications to these boards? Is it "PC → USB3 → A4818 → CONET → VME64/VME64X Digitizer" or a different option?
- (From Douglas) In the past we used a CAEN A2818 or maybe it was A3818 PCIe card in a Linux box to control the Digitizer via long optical fibre from the control room to the electronics rack. Now that we have a new V4718 in the VME crate I would like to use short fibres locally on the electronics rack and just use ethernet to the counting room. But I’ll ship the PC with the old PCIe card as well.





Initial discussions about space/assembly planning



option (1) is for on-site assembly to occur at JLab and option (2) is for wrapping and prep at Jlab but final assembly at BNL.

Option (1): this option is preferable in general, for the following reasons: better access to experts, ease of assembly and access to JLab, etc. It may also be advantageous to have the assembly at JLab since it would allow for a longer assembly time, possibly staged, or carried out in multiple waves rather than continuously. Overall, this option gives more flexibility and time to work out issues during the assembly and pre-installation phases.

Option (2) It is feasible but means that the assembly process would have a hard stop date when integration needs to begin. Depending on how the group that designs/constructs the mechanical frame wants to handle that process this option could complicate their strategy. This option could have an advantage if there are any long lead items that would make a later assembly stage a better option. Starting later means there would be more time to accumulate either the PbWO4 or the SiPM assemblies.

Space planning details

3) Having the wrapping material available at the correct sizes the next step would be the pre-shaping of the ESR material. For this a specialized jig is required - at JLab we have 16 jigs available from the NPS project - and an industrial oven. **For the pre-shaping with the oven another workspace of ~300ft^2 would be required and it would need to be a dust-free environment. In the current updated safety environment**, this work would likely have to be performed by skilled workers. For storage of the wrapping material and final shaped articles three standard storage cabinets would be sufficient. It would also be necessary to have ESD (static free) bags at hand.

4) The **wrapping of the crystals with the pre-shaped wrapping material we estimate to require another 300 ft^2 clean space (different from the oven space above) with an additional storage space of 350 ft^2 holding four rolling rack type shelving units** as used for the NPS assembly final stage. Based on our NPS experience, the wrapping would take about six months with one senior postdoc, one postdoc, one senior grad, and three additional skilled workers (scientists/faculty/university researcher).

Space planning details