Technical Specification

Specification of L0 Silicon Microstrip Sensor for HPS experiment

Abstract

HPS Collaboration specifies technical aspects of the silicon microstrip sensors to be fabricated in the year of 2017. This supply serves to provide sensors for an additional tracking layer to be installed in the upgraded detector. The sensors are single-sided with ac-coupled readout and *p*-strips biased through polysilicon resistors. The substrate is high resistivity n-type silicon. The sensor thickness is 150 μm to reduce multiple scattering in the experiment. One of the sensor edges is within 200 μm from the bias ring to enable close proximity to the accelerator beam. There are two rows of strips to reduce the individual strip occupancy and amplifier's input capacitance.

1. Introduction

1.1. General

Heavy Photon Search (HPS) experiment is one of major experiments using Continuous Electron Beam accelerator at Jefferson Lab. It is searching for Heavy Photon, a particle that weakly couples to dark matter, by identifying the decay products of the electron beam incident on a thin target. It is using both invariant mass search and detached vertex technique to identify heavy photon candidates that may have a significant lifetime. The current experiment contains 6-layer Silicon Vertex Tracker to measure the particle momenta and vertices in the forward geometry. The first layer is situated 10 cm from the target. During the data taking it is lowered to position the sensor active area within 1.5 mm from the beam.

The experiment's upgrade will feature an additional tracking layer, called "Layer 0", that is to be positioned 5 cm from the target. The main goal of the upgrade is to increase the acceptance and improve the vertexing resolution. One side of the sensor has to have slim edge to avoid having the (inactive) sensor material in the beam line.

1.2. HPS p-on-n Microstrip Sensors

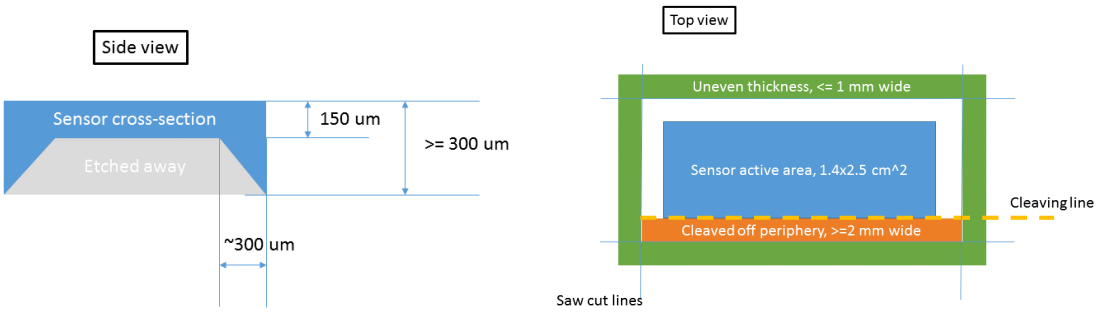
There are several technical drivers for the sensor design:

1) The sensors need to have n-type bulk silicon to be compatible with the standard HPS readout electronics.
2) The sensors' active area and one of the edges near the beam has to be only 150 μm thick to limit the multiple scattering effect.
3) Due to the close proximity of the sensors to the beamline, the beam edge of the sensor has to be "slim". The distance between the bias ring and the physical edge is within 200 μm, as measured in the midpoint of the sensor edge.
4) The method for fabricating the slim edge is "Scribe-Cleave-Passivate", which is based on exploiting the lattice orientation of the bulk silicon during the cleaving process to obtain the sidewall surface with low defect density. Therefore, the silicon wafers should have (100) orientation, and the sensor layout should be aligned with the wafer flat.

It is anticipated that the bulk thickness of 150 μm will be achieved by etching away a larger initial thickness of the original wafer in the region surrounding the active area of the sensor. Since some regions of the wafer need to remain thick to maintain the structural integrity of the wafer, there will need to be 3 regions for each sensor:

1) The active area of the sensors within the bias ring, of about 1.4x2.5 cm^2. It has 150 μm thickness.
2) The thin areas around the active area with guard ring and passive material. This area will be cleaved on one side. Therefore, it should also have 150 μm thickness. To enable cleaving along the "long" edge of the sensor, the width of this area should be around 2 mm.
3) The region around the area (2) with transition between the initial wafer thickness and the thinned region.

The full physical footprint required on the wafer for each sensor is therefore about 2.0 x 3.1 cm^2.



The readout is ac-coupled and the strips are biased via polysilicon resistors.

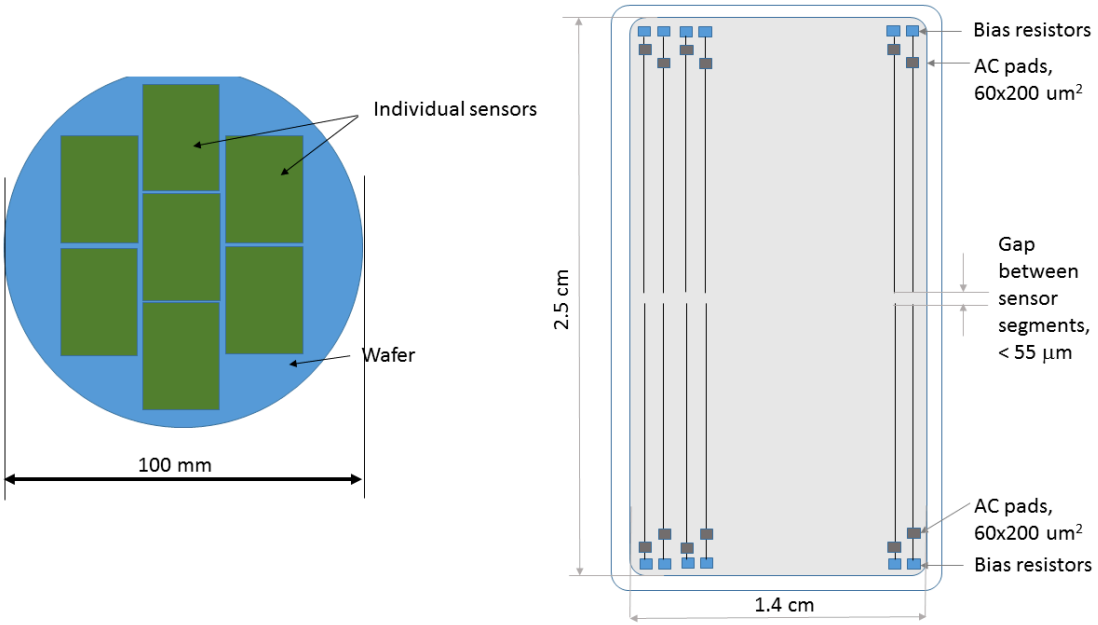
2. Scope of the Technical Specification

The Contractor's obligations include:
- Procurement of the polished silicon substrate material;
- Design and manufacture of the sensor masks (based on the specifications provided by HPS);
- Processing the silicon sensors;
- Quality control, inspection, acceptance testing and documentation;
- Packing;
- Delivery to SLAC

3. Technical Description

All dimensions quoted are those to be found in the processed devices, not the dimensions on the mask designs.

A possible sketch of wafer layout of the 4-in. wafer is shown below. It is desirable to put the maximum number of sensors on a wafer, as long as the requirements for the areas around the active region are satisfied and the "safe" wafer margin is not compromised. The gap between the strip segments should not exceed the strip pitch of 55 μm.



3.1. Specifications In General

3.1.1. Mask Requirements

The Contractor shall be responsible for the final mask designs and shall produce engineering drawings or mask designs to be submitted to the HPS collaboration for approval before the start of production.

- *Number of strip segments*: 2 segments in a large area sensor.
- *Number of implanted strips per segment*: 255
- *Number read out strips per segment*: 255
- *Read-out implant strip width*: TBD in collaboration with the Contractor
- *Read-out strips*: Aluminum, capacitively coupled (see below) over the *n*-implant strips; width TBD in collaboration with the Contractor
- *Polysilicon bias resistors*: Either overlapping the implanted strips or running beside the implanted strips
- *Edge distance*: <= 200 μm for cleaved edge, as measured at the midpoint of the sensor4. 2 mm for un-cleaved edge.
- *Termination structure of the edge*: Manufacturer choice.

- *High Voltage Contact***:** Large metalized contactable layer on the back, with n^+ implant .
- *Readout bond pads***:** 200×60 μm pads for wire-bonding and probing (if feasible), 2 rows in a strip segment.
- *p-bias contacts***:** Available on the bias ring, along the readout bond pads.
- *DC-probe pad contacts***:** Provided to every read-out strip implant at contact point to bias resistor and at the end of strip segments.
- *Passivation***:** Sensors to be passivated on the strip side and un-passivated on the backplane. See the appended drawings for the openings on the passivation.
- *Identification***:** Position of every 10th strip to be clearly indicated. Identification pads are to be used for sensor labeling. Alignment marks are required for module optical metrology.

3.1.2. Special mask requirements

- *Locations* of bias contacts, bond pads, probe points, alignment features, identification marks, etc. are TBD.

3.1.3. Sensor Mechanical/Optical Properties

- *Thickness:* 150μm, with a tolerance of ±10 μm. Signal-generation thickness (=active thickness) ≥ 90% of the physical thickness.
- *Uniformity of thickness within one sensor (Total Thickness Variation, TTV)***:** 10 μm (i.e., central value ± 5 μm)
- *Flatness***:** The sensors should be flat (when unstressed) to within 200 μm
- *Active Area Length:* 2.5 cm.
- *Active Area Width***:** 1.4 cm.
- *Quality of cut edges***:** The dicing should be "full thickness cut". Edge chipping to be avoided and all cut edges to be clean and smooth. No chips or cracks should extend inwards by more than 50 μm
- *Damage and defects:* Device free from scratches, and systematic effects such as consecutive bad strips and/or bad strips in a same location in multiple of sensors, and other defects that could compromise the sensor performance during the lifetime of the experiment. The criteria are to be established in collaboration with the Contractor.

- *Bond Pads*: Metal quality, adhesion and bond pad strength to be such as to allow successful uniform bonding to all readout strips of the sensor using wedge wirebonding, and without causing a degradation in strip quality.

- *Alignment fiducial marks*: All fiducial marks situated between the cut edges and the bias line to be fully visible.

- *Mask alignment tolerances*: ≤3μm misalignment with respect to any other mask. Specific values are the responsibility of the Contractor.

3.1.4. Sensor Electrical Properties

As the wafer bulk type is n- and the strip implant is p-type, the direction of the bias voltage is such that the strip implant is 0 V and the backplane is the positive high voltage. The voltages in this document are in the absolute values otherwise explicitly noted.

- *Processing reproducibility*: ***To be monitored by Contractor*** on test structures.

- *Wafer bulk type*: n-type, FZ

- *W*afer crystal orientation: <100>

- Wafer resistivity: > 1.5 kΩcm.

- *Full Depletion voltage*: V_{fd} < 50.

- *Maximum operating voltage*: 500 V (desirable)

- *Total initial leakage, including guard, with guard ring floating, normalized to 20°C*: < 1 μA at 500 V, ***to be verified by Contractor.***

- *Leakage current stability*: the leakage current to vary by no more than 15% in dry air during 24 hours at 500 V after correcting temperature fluctuations, verified on the sample basis.

- *Resistance of p-implant strip*: <200 kΩ/cm

- *Resistance of aluminum read-out strips*: <100 Ω/cm.

- R_{BIAS} *(Polysilicon) of bias resistor*: 1.0±0.5 MΩ.

- *Interstrip resistance* (R_{int}): $>10\times R_{BIAS}$ at 300V at room temperature (temperature at measurement should be documented in the datasheet.)

- *Interstrip capacitance (C_{int})***:** <1 pF/cm at 100V, measured at 100 kHz. Capacitance between a strip and its nearest neighbors on both sides.

- *AC coupling capacitance ($C_{coupling}$)***:** ≥20 pF/cm, measured at 1 kHz.

- *Percentage of bad strips (i.e. those non-conforming to the Technical Specification)***:** < 1% per strip/segment and < 1% per sensor.

Definition of bad strips (i.e. those non-conforming to the Technical Specification):

In addition to failing the specifications for bias resistance and coupling capacitance, any of the following 5 types of fault will cause a strip to be counted as bad:

1. *Coupling dielectric***:** Shorts through dielectric with 5V applied between the metal and the substrate.
   Measured by Contractor, see article 5.1.

2. *Defective metal strips***:** Metal breaks or shorts to neighbours.
   Measured by Contractor, see article 5.1.

3.2. Wafer Test Structures

HPS assumes that CNM may place test structures on the wafer that help monitor the fabrication process and its quality. Additional structures may be of interest to HPS, however they are not specified at this point.

4. Device Singulation

All sensors that have breakdown voltage above 100 V are to be singulated with saw cutting to leave chips containing active areas with the 2 mm passive margines around them. A subset of the singulated sensors will be cleaved by the contractor to realize a slim edge on one of the long sides. This fraction is TBD in collaboration with the Contractor.

5. Quality Control, Inspection, Acceptance Tests and Data Sheets

5.1. Quality Control, Inspections, Acceptance Tests to be performed by the Contractor

5.1.1. General

The Contractor is required to perform sufficient checks to ensure consistency of processing and to maintain all electrical parameters within the HPS specifications defined in article 3.

5.1.2. Acceptance Test Measurements

The **Contractor** is required to perform the following test measurements on every sensor and strips. The contractor is to supply the measurement results to HPS Collaboration with the delivered sensors:

1. Sensor I-V up to 1000 V bias, stopping at the onset of microdischarge, measuring the current in 20 V steps as the voltage is raised from 0V to 1000 V, with a delay time of 1 to 10 sec. between steps. The condition, i.e., voltage step and delay time, should be annotated in the data sheet.
2. Sensor C-V up to 200 V bias if the breakdown voltage is above 200 V.

2. (*) Strip dielectric shorts for all strips, labeled as strip#", with 5V across the strip dielectric.

3. (*) Strip metal breaks for all strips.

4. (*) Strip metal shorts to neighbours for all strips.

(*) These tests are to be carried out if the breakdown voltage is above 200 V and the full depletion voltage is below 50 V.

5.1.3. Special Labeling

1. The sensors and test structures have the identification label-masks.
2. If the wafer number is not indicated with a scratch pad, it should be clearly labeled with sensor shipment in gelpacks or other packaging methods.

5.1.4. Data Supplied by the Contractor

The following data are required from the Contractor for each sensor:

1. The sensor and wafer labels.

2. Temperature, voltage step and delay time of IV measurement.

3. IV data.

4. Sensor thickness.

5. Depletion voltage.

6. Typical polysilicon bias resistance value(s) for the sensor, or range for the processed batch.

7. List of strip numbers of oxide pinholes.

8. List of strip numbers with strip metal shorts to neighbours.

9. List of strip numbers with strip metal discontinuities.

10. Whether sensor edge cleaving was done, and (for cleaved sensors) distance from the cleaved edge to the bias ring.

6. Documentation

To be supplied for approval prior to the fabrication of sensors:

Detector engineering drawings or mask designs;
Schedule for delivery.

To be supplied with each delivery:
Test data defined in article 4.

Table 1. A summary of HPS-L0 specification

	HPS-L0
Wafer size	4-in. (100 mm)
Wafer type	n-type FZ
Wafer orientation	<100>
Wafer thickness (after thinning)	150 +/- 10 μm
Wafer thickness tolerance	±5%
Wafer active thickness	≥90% of physical thickness
Wafer resistivity	> 1.5 kΩcm
Full depletion voltage	<50 V
Maximum operation voltage	500 V
Inner dimension	14×25 mm^2
Sensor bow after process and dicing:	< 200 μm
Strip segments	2
Number of strips in a segment	255
Strip segment length (approximate)	12.4 mm
Strip implant	P
Strip pitch	55 μm
Gap between strip segments	<= 55 μm
Strip readout coupling	AC
Strip readout metal	Pure Aluminum
Readout strip width	< 10 μm
Strip AC coupling capacitance	>20 pF/cm
Resistance of readout Al strips	<100 Ω/cm
Resistance of N-implant strips	<200 kΩ/cm
Strip bias resistor	Polysilicon
Strip bias resistance (R_b)	1.0+/-0.5 MΩ
Interstrip resistance (R_{int})	>10×R_b at 300 V at RT (temperature should be documented)
Number of strip defects	< 1% per strip/segment, < 1% per sensor
Strip defects	(due to dielectric breakdown, metal and implant strip defects (opens and shorts), micro-discharging strip or bias resistor failures)
Leakage current	<1 μA/cm^2 at 200 V at RT (temperature should be documented)
Leakage current stability in dry (RH<5%) and elevated humidity (RH≥60%)	(<15% for 24 hrs after temperature correction) TBD

Persons in Charge for Technical Aspects

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