To the problem of the lifetime of electronic in the Tagger Hall during the KLF experiment.

Chip Radiation Hardness Assurance. Military/Space grade.

- MIL-PRF-38535K standard. Tests are performed with Co-60 at 50-300 rad/s (100 s => 5-30 krad). Same dose at low intensity may be more harmful.

Grade	krad(Si)	
M	3	Commercial/Industrial (5-10 krad)
D	10	Commercial/Industrial
P	30	
L	50	
R	100	
F	300	
G	500	
H	1000	

Other specifications:

DDD-Displacement Damage Defect. (neutrons)
SEL - Single Event Latch-up.
SEB -Single Event Burnout.
SERG -Single Event Gate Rupture.
TID - total ionising dose effect. (rad or Gy)
SET - single event transient.
SEU single event Upset.

- Military chips withstand up to 1 Mrad and even higher TID.
- Commercial/industrial chips are not graded. However their min TID = 5 krad and min DDD = E+11 n/cm^2

Radiation Hardness Assurance. Military/Space grade.

- Example of Rad. Hardness specifications. Military grade Chip RH3080. (https://www.analog.com/en/products/rh3080mk.html#product-overview)

  TID =200 krad at 50 rad/c;
  TID =100 krad at 10 mrad/c ;
  SED SEU SEL = 120 MeV/cm^2/mg;
  DDD =**1.E+12 n/cm^2**.
- More Examples of Rad. Hardness specifications.

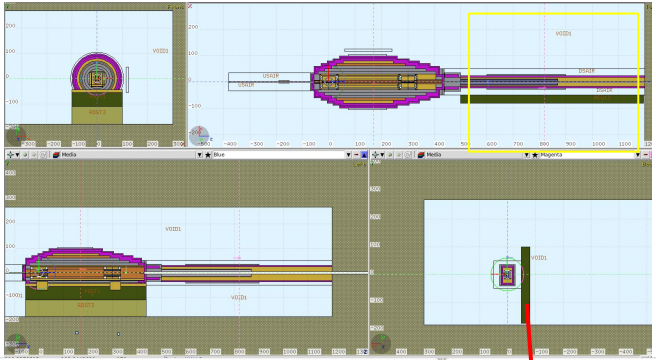
Data Device Corporation TID >=100 krad (memory and processors),
CMOS chips up to **1.E+15 n/cm^2** and **50 krad.**
TTL 5400 , the low-power Schottky (LS) TID=1000 krad.
Emitter-coupled logic (ECL) TID= 1.E+4 krad.

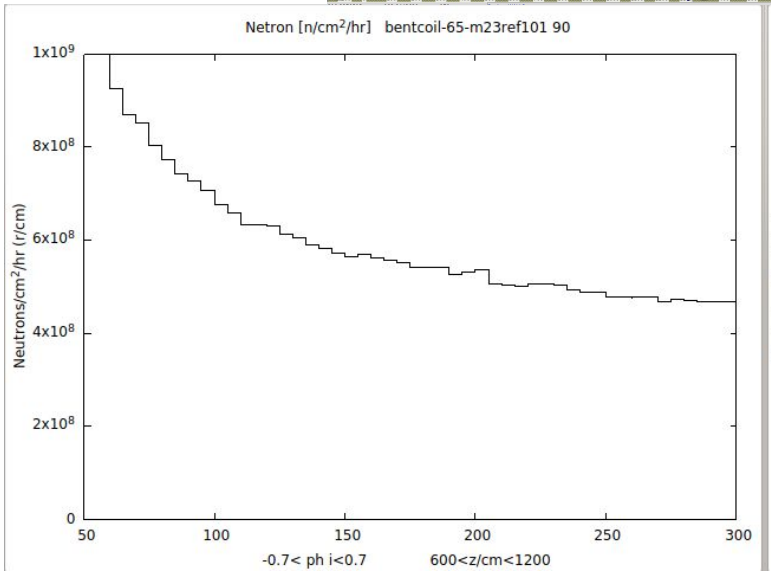
- For now E-mails we sent to

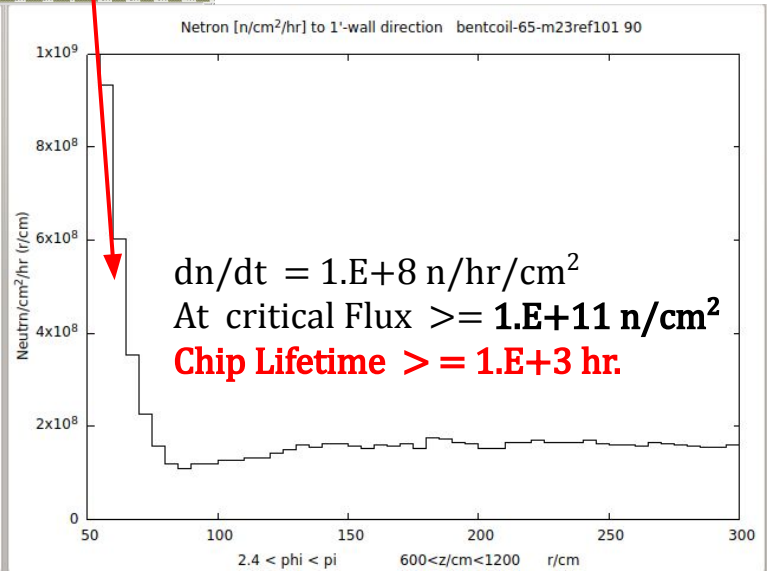
1) ARI Corp (www.aricorp.com), Jozef Lebiedzik. Preamplifier PMT-5R for active collimator. Responded:"...All parts in the PMT-5R are standard commercial grade rating… most sensitive is **CMOS LMC662** …".
2) Rockwell Automation. (https://www.rockwellautomation.com). Allen Bradley 1769-L35E controller. Not yet responded.
3) Pfeiffer Vacuum Technology AG · Headquarters/Germany, info@pfeiffer-vacuum.de.www.pfeiffer-vacuum.net

- Most likely all chips in Tagger Hall are of commercial grade. Therefore, for Lifetime estimates let's use:
  TID = 5 krad
  DDD = E+11 n/cm^2

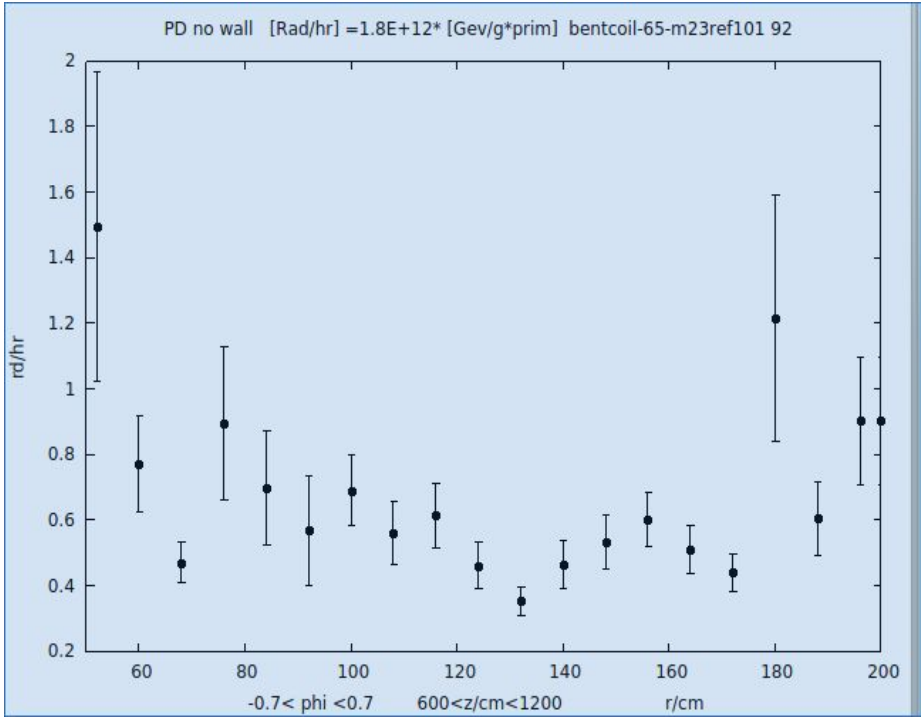
DDD (neutrons) and chip Lifetime. Effect of 1'-B+Concrete wall: 5 times lower neutron

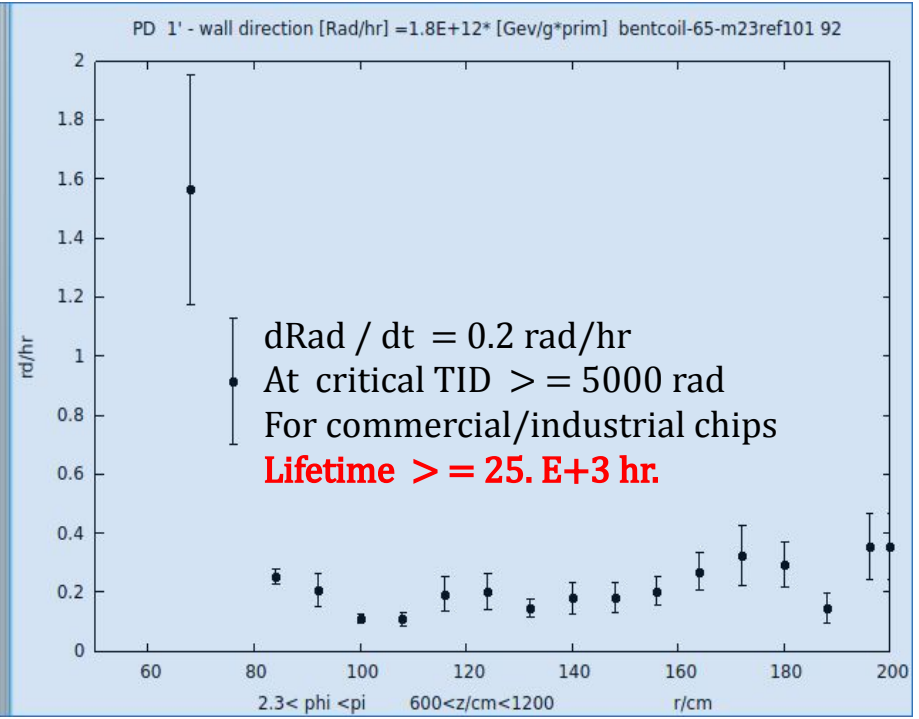




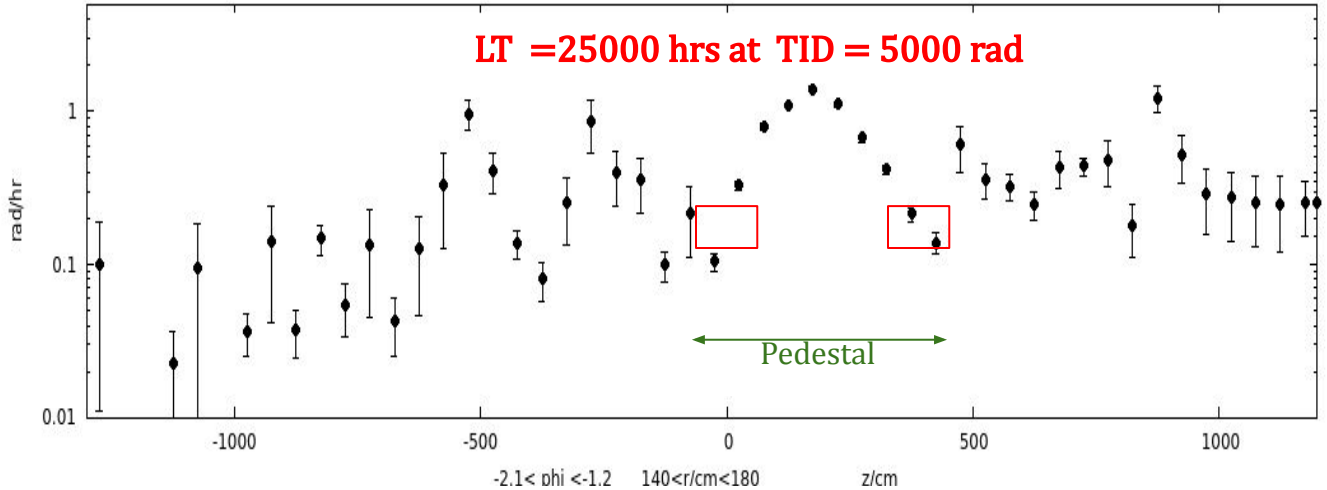


TID (rad) and chip Lifetime. Effect of 1'-B+concrete wall: 5 times lower Prompt Dose.

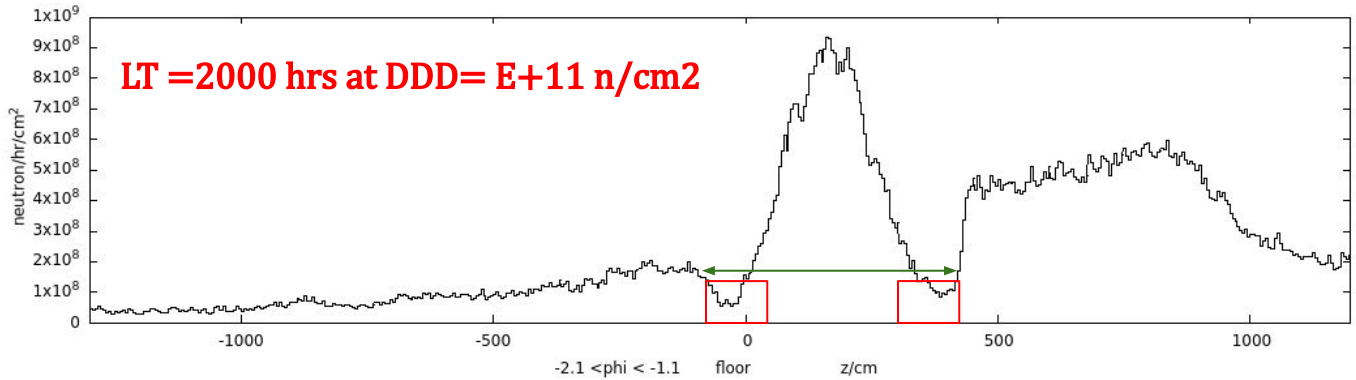




Prompt Dose Profile (rad/hr) at floor level



Neutron Flux Profile (n/cm^2/hr) at floor level

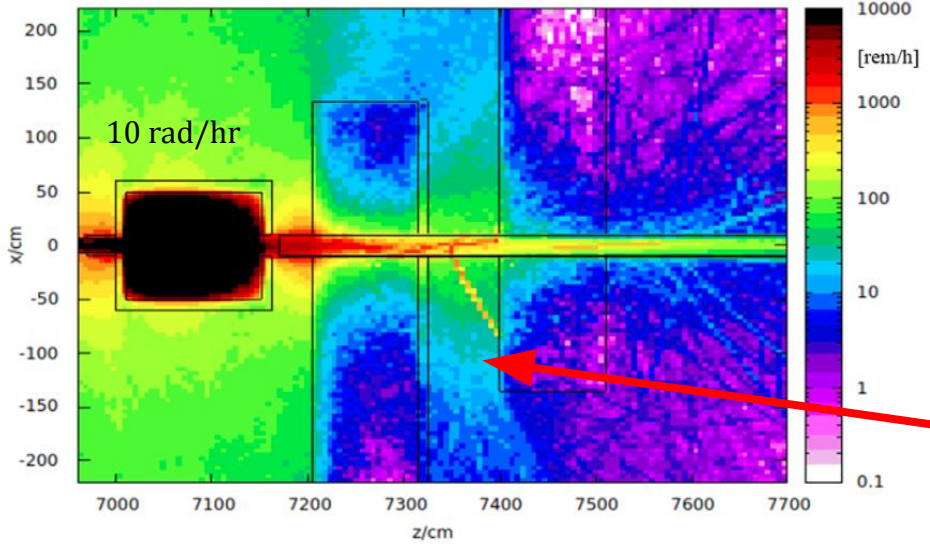


At the floor level of the Tagger Hall

The most pessimistic estimate of the Lifetime of commercial/industrial chips

- Under DDD=1.E+11 n/cm^2 LT2 >= 1000 hrs. (upstream CPS and
  - downstream behind a 1' thick wall).
- Under TID = 5 krad LT>=5000 hrs. (upstream and downstream CPS without wall)

Note that CMOS withstands 1000-10000 times higher DDD and 10 times higher TID!!!
We need specification of chips in use.



Location of PMT-5R (CMOS) for

Active Collimator

Preliminary.

Need to calculate PD field.

Since rad/hr=~1/20 rem/hr

~1 rad/hr => LT =50000 hrs