

LERF RF User Guide

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I. Standard Controls and Information

1. CPUs and IOCs

<i>JLab Cryomodule Number</i>	<i>LCLS-II Cryomodule Name</i>	<i>CPU Node Name*</i>	<i>EPICS IOC Name*</i>
1	ACCL:L1B:0200	lcls-llrfcpu01	sioc-l1b-rf01
2	ACCL:L1B:0300	lcls-llrfcpu02	sioc-l1b-rf02

*CPU Node Name is referred to as <cpuname> in the commands shown below.

EPICS IOC Name is referred to as <iocname> in the commands shown below.

2. Chassis IPs

These are the IP addresses used in the LLRF internal network. They are the same for each cryomodule.

<i>Rack</i>	<i>Chassis</i>	<i>IP</i>
Cavities 1-4 (aka Rack A)	RES	192.168.0.100
Cavities 1-4 (aka Rack A)	RFS1 (cavities 1,2)	192.168.0.101
Cavities 1-4 (aka Rack A)	RFS2 (cavities 3,4)	192.168.0.102
Cavities 1-4 (aka Rack A)	PRC	192.168.0.103
Cavities 5-8 (aka Rack B)	RES	192.168.0.200
Cavities 5-8 (aka Rack B)	RFS1 (cavities 5,6)	192.168.0.201
Cavities 5-8 (aka Rack B)	RFS2 (cavities 7,8)	192.168.0.202
Cavities 5-8 (aka Rack B)	PRC	192.168.0.203

PRC=Precision Receiver Chassis

Reads cavity probe signals

RFS=RF Station

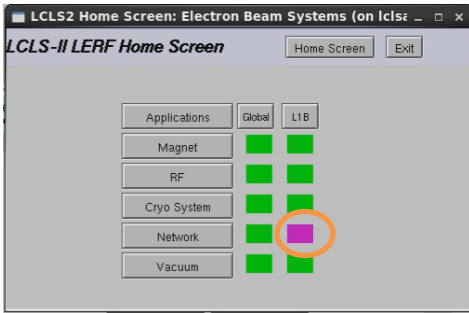
Provides RF drive; reads forward , reverse, detune signals

RES=Resonance/Interlock Chassis

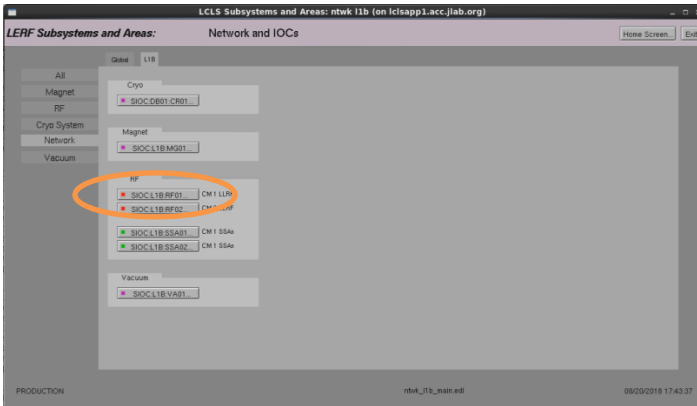
Controls tuners; performs interlock logic

3. Start/Restart the EPICS IOC

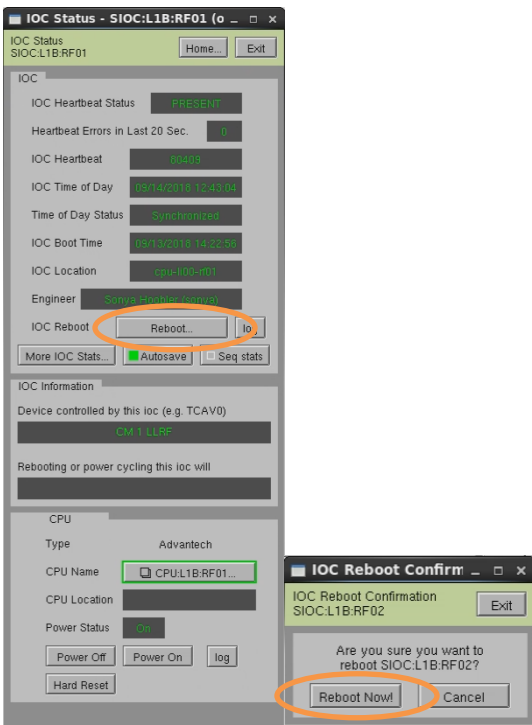
1. Log into LERF workstation or server
(lcls01/2/3/lclsapp1 with individual user id)
2. Type lerfhome&



3. Click on box intersecting Network and L1B



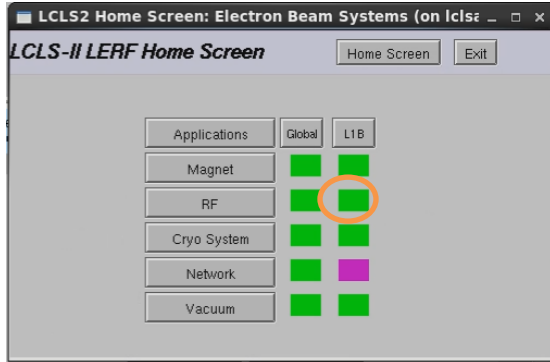
4. Click on IOC of interest



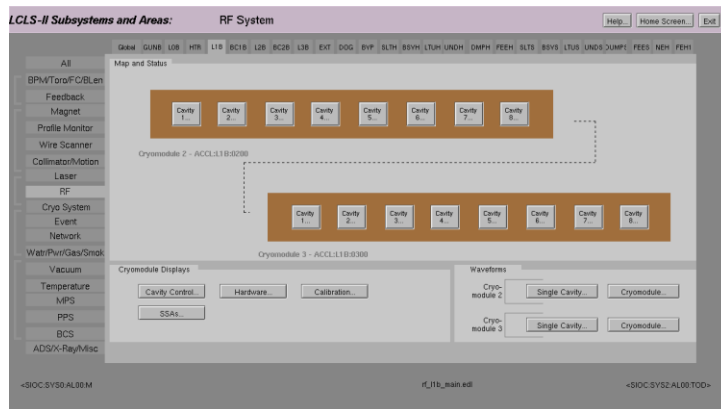
5. Click on *Reboot...* Then click on *Reboot Now!*

4. View RF EDM displays

- Log into LERF workstation or server
(lcls01/2/3/lclsapp1 with individual user id)
- Type `lerfhome&`



- Click on box intersecting RF and L1B



L1B Overview Display

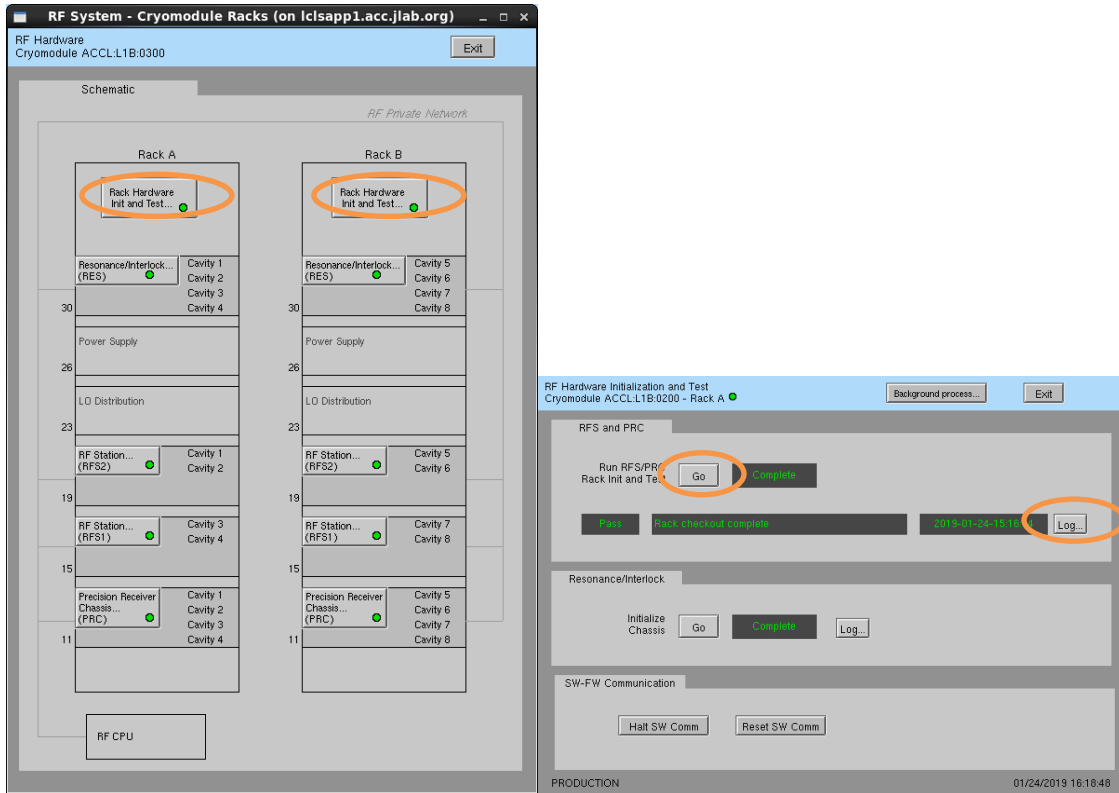


Single Cavity Display

5. Initialize/Checkout LLRF Hardware

Needed after power outage, hardware swap, etc.

- Click on *Hardware...* (from either L1B Overview or Single Cavity display—see above).

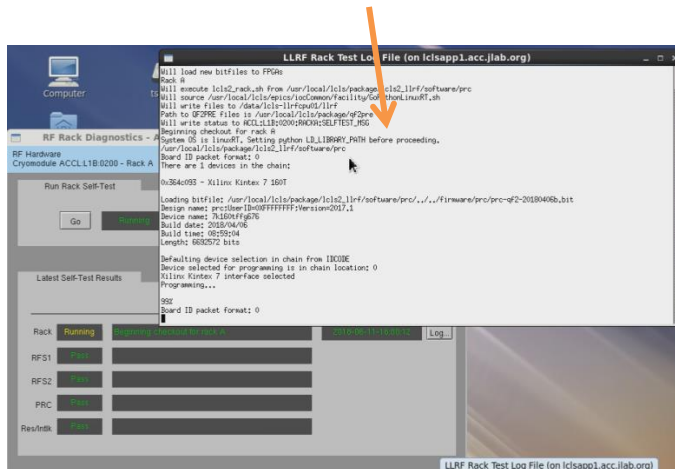


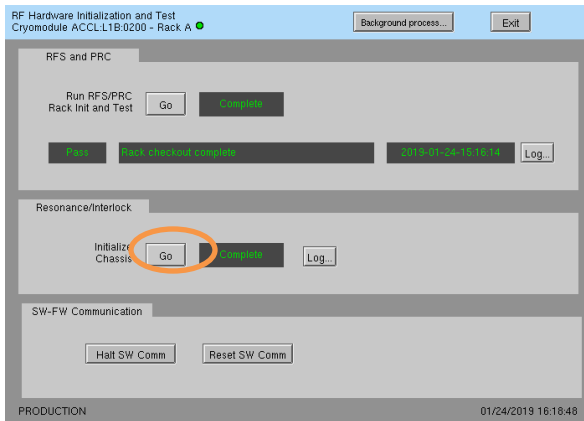
- For appropriate rack (A or B), open display labelled *Rack Hardware Init and Test...*

- Execute RFS/PRC initialization and checkout. Click on *Go*
(The script will disable and then re-enable communication with EPICS.)

To view the rack test script output, click on *Log...*

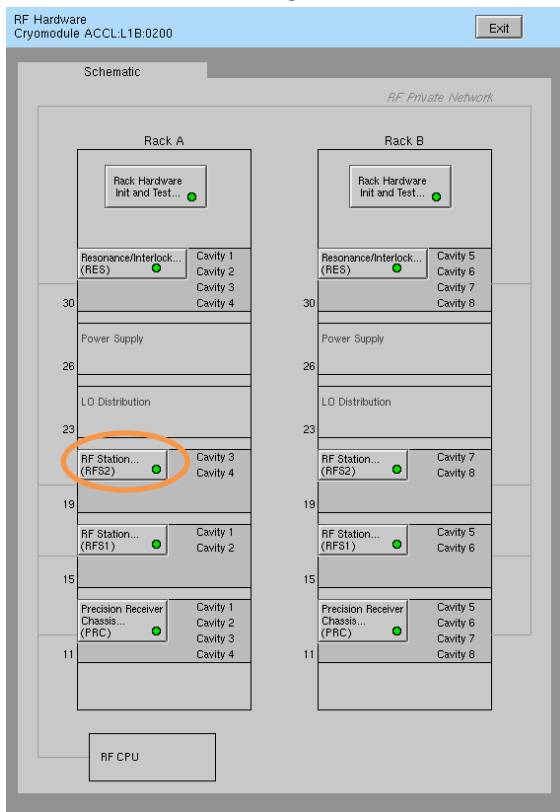
It will open an xterm window and display the script output as it progresses.





- d. Initialize RES chassis. Click on *Go*
 (The script will disable and then re-enable communication with EPICS.)

There are currently no automated checks for RFS<->RES communication. You'll need to look at the diagnostic display. From the Hardware display, for the appropriate rack, click on an individual chassis, then click on *Comm Diag...*



RF Chassis
ACCL11B:0200:RFS1A

Comm Diag... Exit

Chassis Software Controller

State: **Running** [Reset]

Status: **NO_ALARM**

Last Error:

Count TX: **3148288**

Count RX: **3148182**

Count Timeout: **0**

Count Error: **0**

Clock Status: **Valid**

IP Address: **192.168.0.101**

[Halt]

Chassis Monitoring

LO: **15.45 GHz** [More AMC7823...]

Temp: **77.8 DegF**

QF2 Board 6V: **6.22 V** [More FPGA Board...]

Kintex Temp: **43.12 DegC**

QF2 Board Temp: **30.98 DegC**

Other

FW Code Hash: **af8cc340276e2b009128f735a6234403b1589e543**

CRC Errors: **58885** Status: **OK**

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LLRF Chassis Communication Diagnostics
Rack A Cryomodule ACCL11B:0200

Exit

Resonance/Interlock

Rx 0: Error Lock, Link Error, Timeout, Wrong Protocol, CRC Fault, Wrong Frame, Protocol Version, Gateway Type, Location. Detune Valid, Detune Valid. Rev ID: **489313F3**, Counts: **100DA38C**

Rx 1: Error Lock, Link Error, Timeout, Wrong Protocol, CRC Fault, Wrong Frame, Protocol Version, Gateway Type, Location. Detune Valid, Detune Valid. Rev ID: **489313F3**, Counts: **6A9E5DF0**

RFS1

Rx: Error Lock, Link Error, Timeout, Wrong Protocol, CRC Fault, Wrong Frame, Protocol Version, Gateway Type, Location. Permit, Permit. Rev ID: **F71E3D2E**, Counts: **8E97A6**

RFS2

Rx: Error Lock, Link Error, Timeout, Wrong Protocol, CRC Fault, Wrong Frame, Protocol Version, Gateway Type, Location. Permit, Permit. Rev ID: **F71E3D2E**, Counts: **F17869F**

Tx

Cav 0 Aux, Cav 1 Aux, Cav 2 Aux, Cav 3 Aux. Location: **0**, **0**

Cav 0 Aux, Cav 1 Aux. Location: **0**, **0**

Cav 0 Aux, Cav 1 Aux. Location: **0**, **0**

PRODUCTION 05/22/2019 10:28:28

The top row shows the RES status; the bottom the RFS status. In the *Rx* sections, the *Link Error* bit is set (blue) if there is a problem. (This snapshot shows no communication errors.) There is other useful data on this display too: the detune frequency measured by the RFS and a bit indicating if that value is valid and should be used; the permit bit sent from the Resonance/Interlock chassis to the RFS.

6. Cavity Characterization and Setup

There are a set of scripts used during initial cavity setup.

These are accessible from the *Characterization...* display. They are listed in the order in which they should be run.



With the exception of SEL phase offset, the calculated characterization parameters must be accepted by the user before they are 'in use', i.e. pushed to the primary EPICS PVs and used by software.

SSA Calibration

This measures the SSA output/input slope. The Results Summary will indicate if the scan was successful. The user may need to iteratively adjust the *SSA Drive Max* and re-run the scan. (This *SSA Drive Max* is also used as the upper limit when setting RF amplitude via the usual cavity controls.)

User Inputs:

SSA stimulus amplitude

Script Actions:

Drive SSA for about 200 microseconds.

At end of scan, leave RF off.

Script Results:

(action required to use)

SSA slope - ratio of output to input in normalized units

This value written to *Newly Calculated*; user must press *Push* to accept new value

Detune Frequency Scan

Measure detune frequency offset from 1300 MHz. The scan range is +/- 10 kHz so it is recommended to use this when the cavity frequency offset is within that range. (At LERF, that initial tuning is done using a network analyzer and the frequency offset brought to about 1 kHz.)

User Inputs:

Scan Freq Offset: offset from 1300 MHz to use as scan center

Drive Level: LLRF drive level

Script Actions:

Scan +/- 10 kHz about desired offset.

At end of scan, leave RF off.

Script Results:

(informational)

Measured detune frequency offset from 1300 MHz

Measured cavity amplitude at that detune frequency

Pulsed SEL Calibration

Measures optimal SEL phase offset, cavity probe signal scale factor, and loaded Q. Leaves the cavity on in pulsed SEL mode

User Inputs:

LLRF drive level

Script Actions:

Run pulsed SEL RF at requested drive level.

At end of scan, leave RF in pulsed SEL.

Script Results:

(action required to use)

Cavity amplitude scale factor (rev wf method)

Loaded Q

These values written to *Newly Calculated*; user must press *Push* to accept new value(s)

(immediately in use)

SEL phase offset

Cavity Ramp-Up

Brings cavity on in CW SELAP mode by starting in pulsed SEL, increasing pulse length and amplitude, and locking amplitude and phase. Like Pulsed SEL Calibration, it also measures optimal SEL phase offset, cavity probe signal scale factor, and loaded Q. Leaves the cavity on in CW SELAP.

User Inputs:

Cavity amplitude goal

Script Actions:

Run pulsed SEL RF

Incrementally lengthen pulse, until in SEL CW
Switch to CW SELAP, locking phase and amplitude loops
At end of scan, leave RF in CW SELAP at amplitude goal

Script Results:

(action required to use)

Cavity amplitude scale factor (RevCal method)

Loaded Q

These values written to *Newly Calculated*; user must press *Push* to accept new value(s)

7. Basic LLRF Controls

When turning on a cavity, first select the desired *RF Mode* from these options:

SELAP CW Self-Excited Loop with amplitude and phase locked. Functionally identical to GDR when the cavity detuning is small enough to allow lock. Unlike traditional GDR mode, it temporarily falls back to SELA when detuning increases.

SELA CW Self-Excited Loop with amplitude locked. Tracks cavity natural resonant frequency.

SEL CW Self-Excited Loop. Tracks cavity natural resonance frequency.

SEL Raw CW Self-Excited Loop with raw amplitude control. Set amplitude using % of full drive scale instead of relying on the calibrated values used in ADES.

Pulse Pulsed Self-Excited Loop. Set amplitude using % of full drive scale. Then use pulsed Go/Stop buttons.

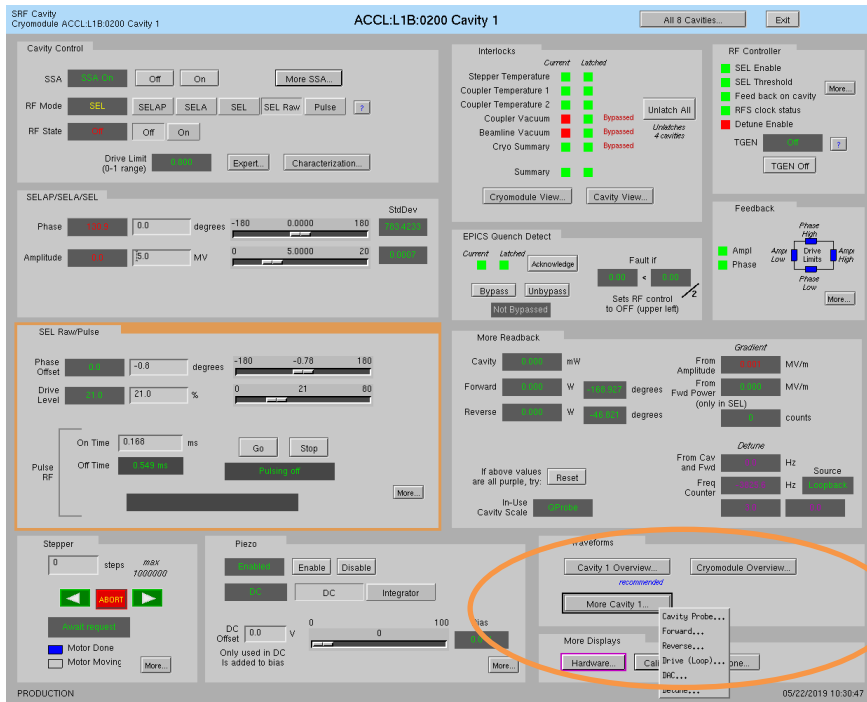
Then set *RF State* to *On*.

The amplitude and phase controls are different between (a) modes SELAP, SELA, SEL and (b) SEL Raw, Pulse. On the cavity screen, the appropriate phase/amplitude control block will be highlighted in orange



See sections 9 and 10 for more details on SEL Raw and Pulse controls.

8. View RF Waveform Plots

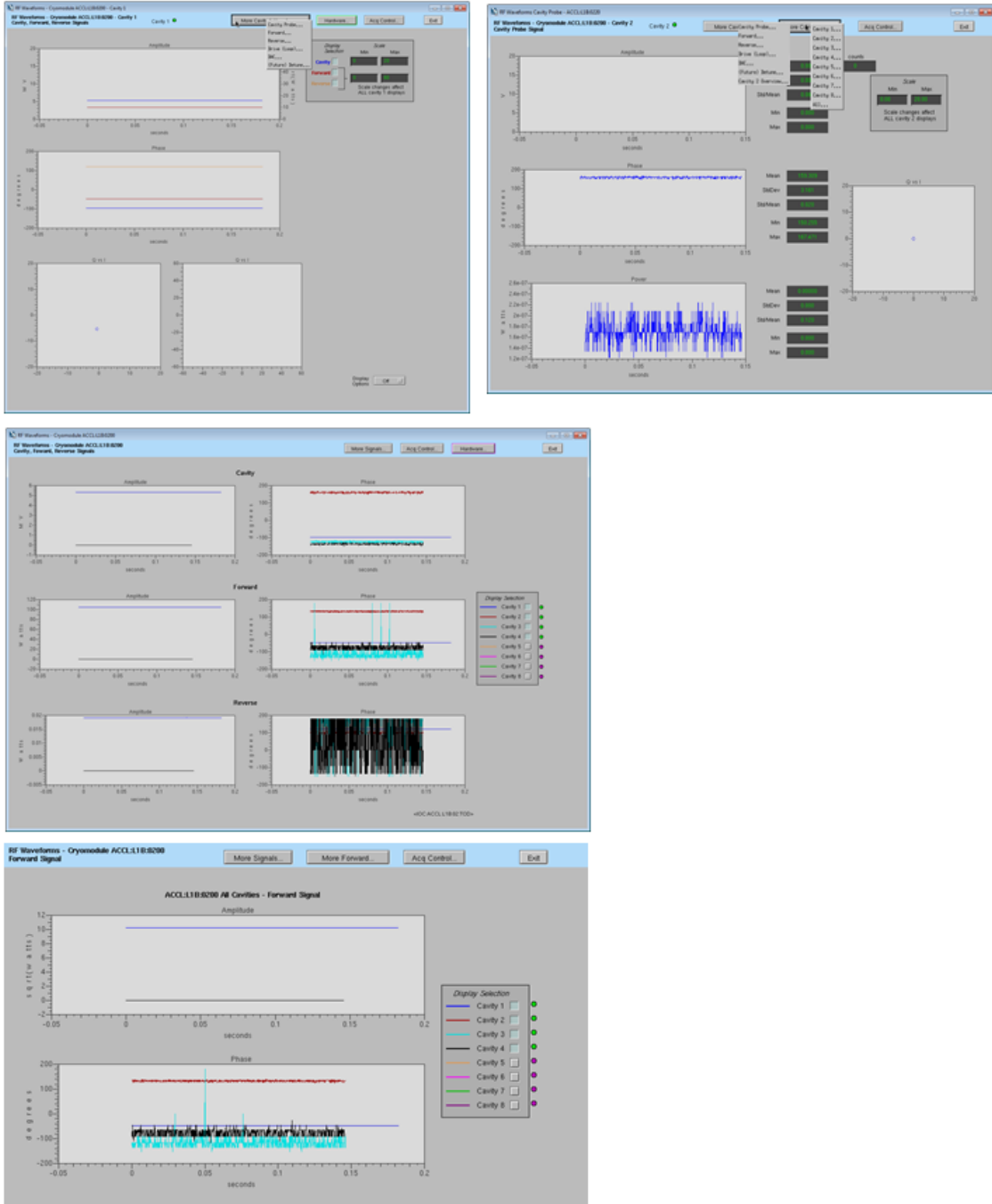


Cavity Overview -- Cavity, Forward, Reverse signals for single cavity

Cryomodule Overview -- Cavity, Forward, Reverse signals for all 8 cavities

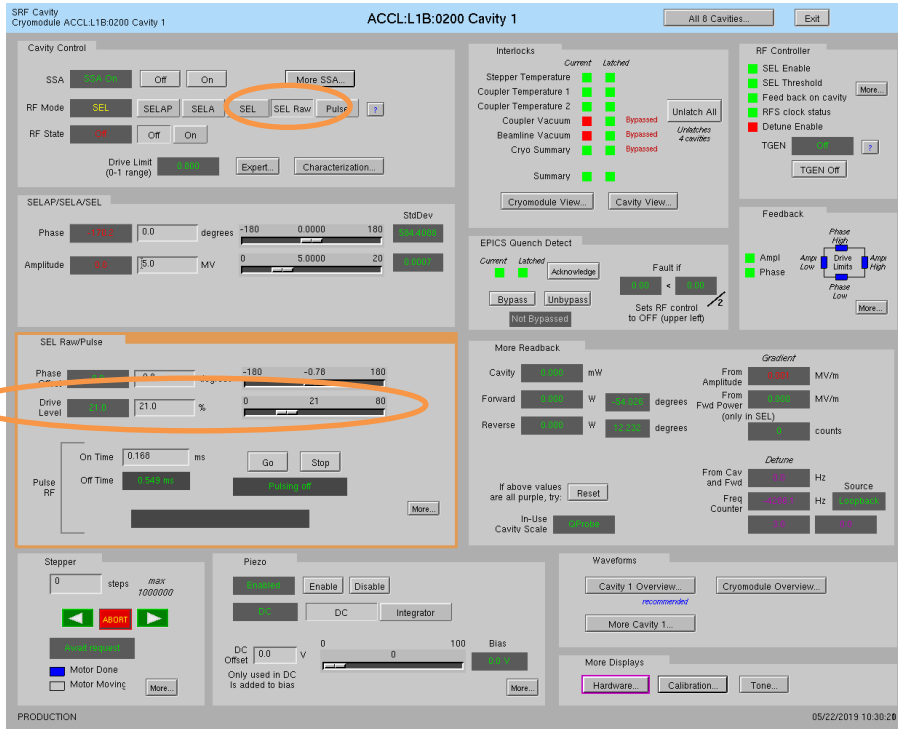
More Cavity -- Drop-down menu for single-cavity single-signal display

From those displays, you can navigate to other cavities, other signals, or display a single signal for all 8 cavities. Example display shots:



9. Raw SEL Amplitude Control

If the SSA parameters and cavity signals are not yet fully calibrated, it may be desirable to run in SEL mode using raw drive control.



- Set *RF Mode* to *SEL Raw*
- Set *RF State* to *On*
- Set *Drive Level*. *Drive Level* is set in percentage of full drive scale. Its upper limit is slaved to the SSA max drive level, which can be set from the Expert phase/amplitude display. Modifying that limit is an expert function.



10. Run SEL Pulsed RF

The screenshot shows the SRF Cavity control interface for ACCL1B:0200 Cavity 1. The interface is divided into several sections:

- Cavity Control:** Includes SSA (Off), RF Mode (SEL), RF State (On), Drive Limit (0-1 range), and buttons for Expert... and Characterization...
- Interlocks:** Shows various interlock statuses (Current/Latched) for Stepper Temperature, Coupler Temperature 1/2, Coupler Vacuum, Beamline Vacuum, and Cryo Summary.
- RF Controller:** Includes SEL Enable, SEL Threshold, Feed back on cavity, RFS clock status, Detune Enable, and TGEN (Not off).
- SELAP/SEL/SEL:** Shows Phase Offset (0.0 degrees) and Amplitude (5.0 MV).
- EPICS Quench Detect:** Includes Current/Latched, Acknowledge, Fault if, Bypass, and Unbypass buttons.
- Feedback:** Shows Ampl and Phase feedback with Drive Limits and Phase Low/High indicators.
- SEL Raw/Pulse (highlighted):** Shows Phase Offset (-0.8 degrees), Drive Level (21.0%), On Time (0.163 ms), and Off Time (0.0 ms). The Go button is highlighted in yellow.
- More Readback:** Shows Cavity, Forward, and Reverse power (mW) and various readback parameters like Gradient, Detune, and Freq Counter.
- Stepper:** Shows steps (0) and Motor Done/Moving status.
- Piezo:** Shows DC (0.0 V) and Bias (0) settings.
- Waveforms:** Includes Cavity 1 Overview, Cryomodule Overview, and More Cavity 1 buttons.
- More Displays:** Includes Hardware, Calibration, and Tone buttons.

- Set *RF Mode* to *Pulse*.
- Set *RF State* to *On*.
- In the *SEL Raw/Pulse* block, set *Drive Level* and *On Time*. Click on *Go*.
- When done, click on *Stop*.
- To update *Drive Level* or *On Time*, enter new values and then click on *Go* again. The *Go* button will be highlighted in yellow to remind you of this.

Note that the total pulse on/off cycle length is determined by the waveform configuration settings. Click on *More...* for the SEL controls display, which has more detail on this:

The screenshot shows the SRF SEL Controls interface for ACCL1B:0200 Cavity 1. The interface is divided into several sections:

- SEL Phase Offset:** Shows Phase Offset (-0.8 degrees).
- SEL Drive & Pulsed:** Shows RF Mode (SEL), RF State (On), Drive Level (21.0%), and buttons for Go, Stop, and Pulsing on.
- Pulse RF:** Shows Amplitude (5.0 MV), RF On Time (0.163 ms), and RF Off Time (0.0 ms). The Go button is highlighted in yellow.
- More...:** A button labeled 'More...' is highlighted in yellow at the bottom right of the Pulse RF section.

11. Control Stepper Motor Tuner



From the *Stepper* block you can enter number of steps and then click the green arrow to go in one direction or the other. (Relationship between direction and frequency is not yet known.) Click on *More...* for the detailed single tuner display.

12. Control Piezo Tuner

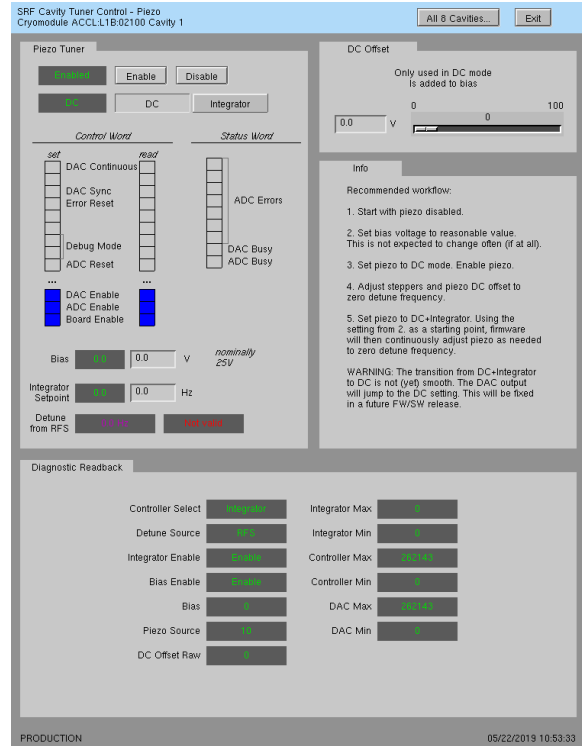


From the *Piezo* block you can control piezo enable/disable, mode, and DC offset. Click on *More...* for the detailed piezo tuner display.

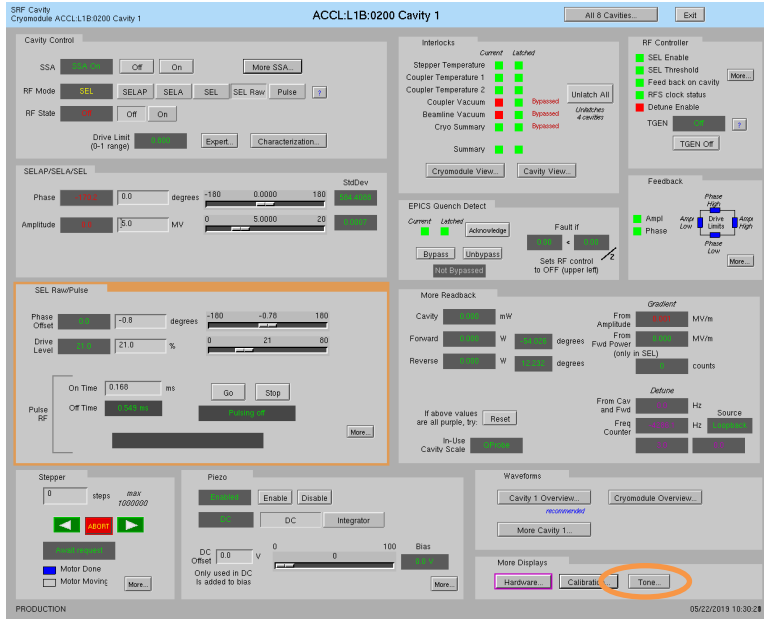
Recommended piezo workflow:

1. Start with piezo disabled.
2. The bias voltage is used to keep the piezo operating near the middle of its range. Set *Bias* to a reasonable value, nominally 25 V. This is not expected to change often (if at all).
3. Set piezo to DC mode. Enable piezo.
4. Adjust steppers and piezo DC offset to zero detune frequency.
5. Set piezo to Integrator mode. Using the setting from 2 as a starting point, firmware continuously adjusts the piezo as needed to zero detune frequency. Note that the *Detune from RFS* must be Valid for the integrator to function.
6. If you observe an offset (if you can see in the phase waveforms that the detune frequency is not exactly zero but *Detune from RFS* shows 0 Hz), you may enter an *Integrator Setpoint* to compensate.

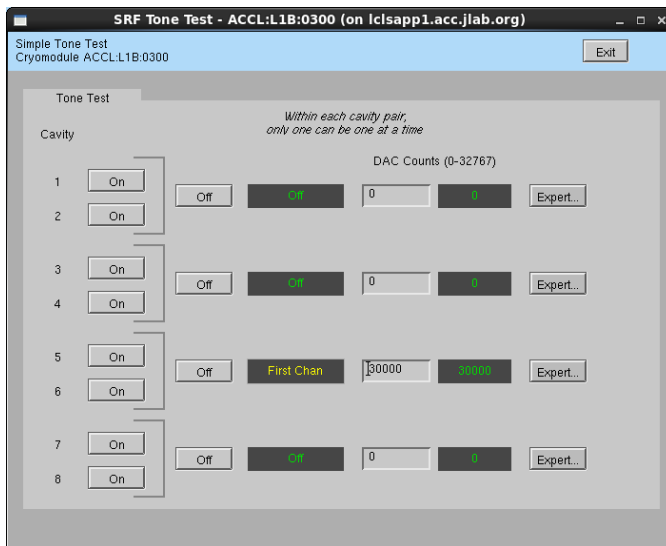
WARNING: The transition from Integrator to DC is not yet smooth. The DAC output will jump to the DC setting. This will be fixed in a future FW/SW release.



13. Drive Cavity With Simple Tone Signal



a. Click on *Tone...*



b. For desired cavity, click on *On*, then enter number of *DAC Counts*...

c. When done, click on *Off*

Note that these controls override the RF Mode and Off/On settings. When you turn the tone off, the RF will return to its previous state.

14. Interlocks

The interlock/resonance chassis executes the interlock logic and sends a per-cavity RF Permit to the RFS chassis. If that permit is not set, the RFS inhibits LLRF drive. Interlocks latch and must be unlatched by a user before RF is again permitted.

All interlocks use hardware signals with the exception of the cryo interlock, which read 2 EPICS PVs from the JLab control system. The interlock is faulted if either of these PVs is offline.

The cavity overview display provides high-level interlock status and unlatch.



Logic details, temperature thresholds, and bypass control are available on the individual cavity or cryomodule interlock displays.

SRF Cavity Interlocks - Expert
Cryomodule ACCL1B.02 Cavity 2

Cryomodule Interlocks... Temperature Expert... Exit

Interlock Logic

Note on which cavities bypasses affect
Coupler Vac, Beamline Vac, Cryo Sum: cavities 1 - 4
CHL Ready and He Level: cavities 1 - 8
Temperatures: just this cavity

CHL Ready: Source PV LLRF Mirror OK

He Level: OK

He Pressure: Future OK

Coupler Vac: Bypassed

Beamline Vac: Bypassed

Cryo Sum: Bypassed

Cavity 2 Summary: Bypassed

Unlatch All: Unlatches 4 cavities
Must unlatch to clear after interlock bypass

	Value	Low Threshold [V]	High Threshold [V]	Status	Action
Stepper Temp	0.0000	0.0000	0.0000	Not Bypassed	Not Bypassed
Coupler Temp 1	0.0000	0.0000	0.0000	Not Bypassed	Not Bypassed
Coupler Temp 2	0.0000	0.0000	0.0000	Not Bypassed	Not Bypassed

RF Inhibit: Res Link Indk Permit Permit Check Active RFS RF Permit

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SRF Interlocks
Cryomodule ACCL1B.0200

Interlock Diagram

Cryomodule Unlatch All: Must unlatch to clear after interlock bypass

Cryomodule Vacuum and CHL Ready (Rack A Status)

Cryo Sum: Not Bypassed

Coupler Vac: Bypassed

Beamline Vac: Bypassed

Cavity 1 Temps: Stepper Not Bypassed, Coupler 1 Not Bypassed, Coupler 2 Not Bypassed

Cavity 2 Temps: Stepper Not Bypassed, Coupler 1 Not Bypassed, Coupler 2 Not Bypassed

Cavity 3 Temps: Stepper Not Bypassed, Coupler 1 Not Bypassed, Coupler 2 Not Bypassed

Cavity 4 Temps: Stepper Not Bypassed, Coupler 1 Not Bypassed, Coupler 2 Not Bypassed

Cryomodule Vacuum and CHL Ready (Rack B Status)

Cryo Sum: Not Bypassed

Coupler Vac: Not Bypassed

Beamline Vac: Not Bypassed

Cavity 5 Temps: Stepper Not Bypassed, Coupler 1 Not Bypassed, Coupler 2 Not Bypassed

Cavity 6 Temps: Stepper Not Bypassed, Coupler 1 Not Bypassed, Coupler 2 Not Bypassed

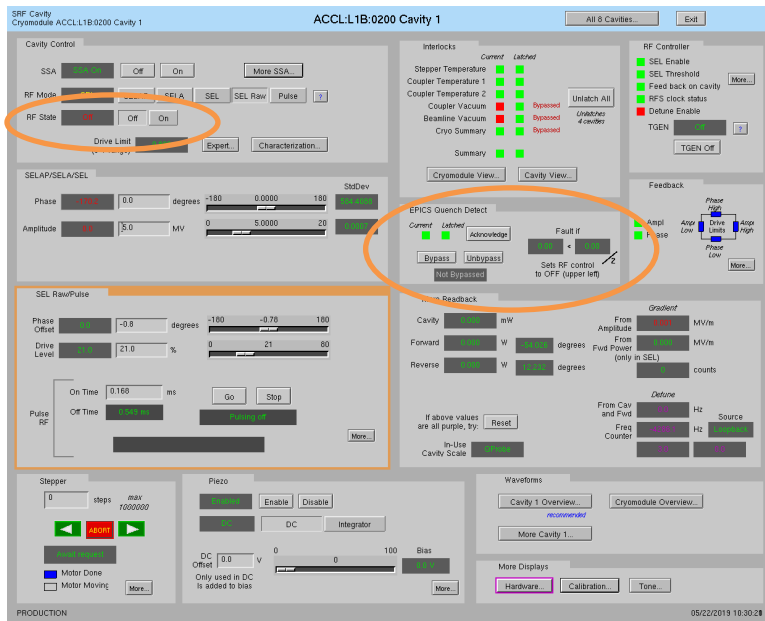
Cavity 7 Temps: Stepper Not Bypassed, Coupler 1 Not Bypassed, Coupler 2 Not Bypassed

Cavity 8 Temps: Stepper Not Bypassed, Coupler 1 Not Bypassed, Coupler 2 Not Bypassed

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15. EPICS Quench Detection

Quench detection will eventually be implemented in firmware, but for now we have a simple EPICS level check that is used. Because this was a quick temporary solution, this fault does not use the standard interlock shutoff path, but simply sets *RF State* to *Off*. To recover RF, click the on *Acknowledge* and then set *RF State* to *On*.



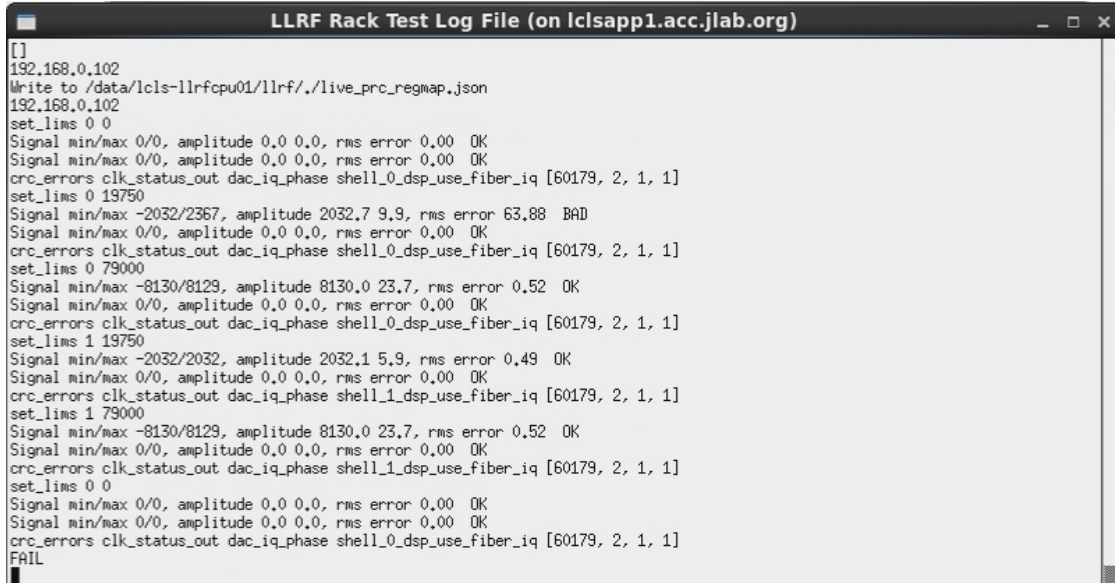
This check compares the measured cavity probe amplitude signal with a calculated cavity amplitude that is based on forward power. If the cavity probe value is less than half of the value calculated from forward power, it is a fault.

Idiosyncrasies of this check: Latched status is provided to notify users of a recent fault, but the fault does not need to be acknowledged in order to turn the RF back on. It is recommended to acknowledge the fault before turning on RF so any future transient fault is caught.

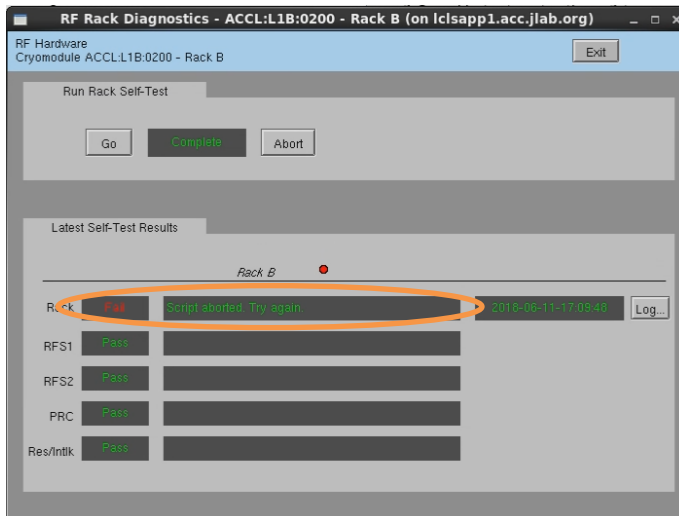
II. Occasional Issues

1. Mystery Rack Checkout Error

We occasionally see a problem during the first cryomodule rack A checkout. This is what it looks like:



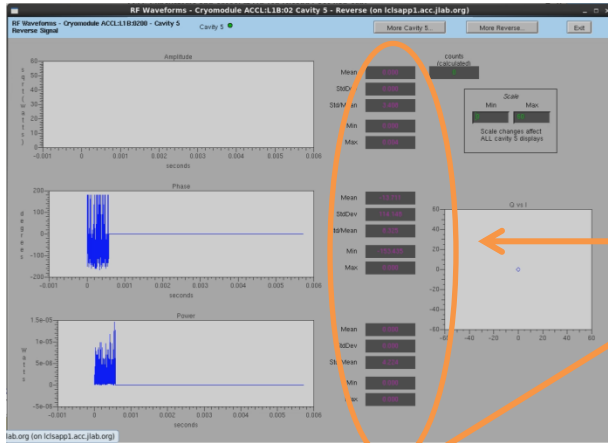
```
[ ]
192.168.0.102
Write to /data/lcls-llrfcpu01/llrf/./live_prc_regmap.json
192.168.0.102
set_lims 0 0
Signal min/max 0/0, amplitude 0.0 0.0, rms error 0.00 OK
Signal min/max 0/0, amplitude 0.0 0.0, rms error 0.00 OK
crc_errors clk_status_out dac_iq_phase shell_0_dsp_use_fiber_iq [60179, 2, 1, 1]
set_lims 0 19750
Signal min/max -2032/2367, amplitude 2032.7 9.9, rms error 63.88 BAD
Signal min/max 0/0, amplitude 0.0 0.0, rms error 0.00 OK
crc_errors clk_status_out dac_iq_phase shell_0_dsp_use_fiber_iq [60179, 2, 1, 1]
set_lims 0 79000
Signal min/max -8150/8129, amplitude 8150.0 23.7, rms error 0.52 OK
Signal min/max 0/0, amplitude 0.0 0.0, rms error 0.00 OK
crc_errors clk_status_out dac_iq_phase shell_0_dsp_use_fiber_iq [60179, 2, 1, 1]
set_lims 1 19750
Signal min/max -2032/2032, amplitude 2032.1 5.9, rms error 0.49 OK
Signal min/max 0/0, amplitude 0.0 0.0, rms error 0.00 OK
crc_errors clk_status_out dac_iq_phase shell_1_dsp_use_fiber_iq [60179, 2, 1, 1]
set_lims 1 79000
Signal min/max -8150/8129, amplitude 8150.0 23.7, rms error 0.52 OK
Signal min/max 0/0, amplitude 0.0 0.0, rms error 0.00 OK
crc_errors clk_status_out dac_iq_phase shell_1_dsp_use_fiber_iq [60179, 2, 1, 1]
set_lims 0 0
Signal min/max 0/0, amplitude 0.0 0.0, rms error 0.00 OK
Signal min/max 0/0, amplitude 0.0 0.0, rms error 0.00 OK
crc_errors clk_status_out dac_iq_phase shell_0_dsp_use_fiber_iq [60179, 2, 1, 1]
FAIL
```



It is an intermittent failure and is not understood. You'll have to simply re-run rack checkout and hope it passes. (We have observed that if the system was previously set up correctly and there has been no outage/hardware swap since, it will probably work fine in spite of this error.)

2. Recover Non-Updating EPICS Waveforms

Once in a while, I've seen the EPICS waveform data stop updating. Displays will look like this:



Waveforms frozen

Readback values purple (INVALID)

EPICS-to-RFS communication status OK



If you see this and nothing else seems to be wrong, try clicking the *Reset* button on the cavity display. This will briefly halt and then reset communication between the software and all LLRF chassis in this cryomodule.

3. Ping Test

To test if a chassis pings from a CPU:

- a. Log into LERF workstation or server
(lcls01/2/3/ lclsapp1 with individual user id)
- b. Log into cpu (using CPU Node Name from Section 1):

iocConsole <cpuname>

OR

ssh laci@<cpuname>

(If prompted for login, type 'laci' and hit enter.)

- c. Type: ping <ip>

4. View the EPICS IOC Console

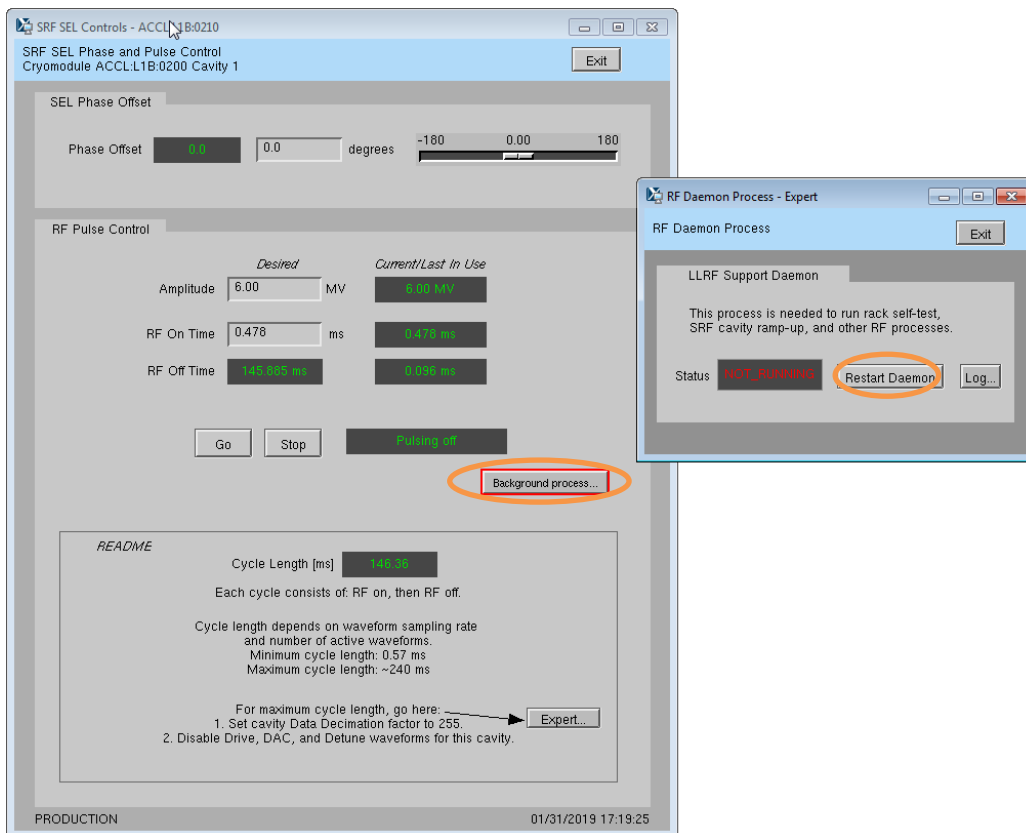
- a. Log into LERF workstation or server
(lcls01/2/3/lclsapp1 with individual user id)
- b. iocConsole <iocname>
- c. To exit viewer, press these 3 keys together: **Ctrl, a, d**.
- d. To scroll up in viewer, press these 3 keys together: **Ctrl, a, [**. Then use arrows to move up/down. To exit scroll mode, press these 3 keys together: **Ctrl, a,]**.

(If you inadvertently kill the ioc, you can restart it using the instructions in section 2.)

5. RF 'Background Process'

Much of the current RF functionality (rack checkout, pulse control, cavity ramp, etc.) is performed by scripts external to the EPICS IOC. This is facilitated by a continuously running background process that is driven by EPICS PVs. This allows us to execute these functions from EPICS PVs on EDM displays—and not have to manually run scripts from the command line.

On every display that relies on this, there is a button titled *Background process*. If the process is not running, there will be a red rectangle around that button. Click on that button to open a display from which you can start/restart the process. Example:



This process will not successfully launch if the EPICS PVs it relies on are not all online. Both LLRF EPICS IOCs must be on.