LERF RF User Guide

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I. Standard Controls and Information

1. CPUs and IOCs

JLab Cryomodule Number	LCLS-II Cryomodule Name	CPU Node Name*	EPICS IOC Name*
1	ACCL:L1B:0200	lcls-llrfcpu01	sioc-l1b-rf01
2	ACCL:L1B:0300	lcls-llrfcpu02	sioc-l1b-rf02

*CPU Node Name is referred to as <cpuname>in the commands shown below. EPICS IOC Name is referred to as <iocname> in the commands shown below.

2. Chassis IPs

These are the IP addresses used in the LLRF internal network. They are the same for each cryomodule.

Rack	Chassis	IP
Cavities 1-4 (aka Rack A)	RES	192.168.0.100
Cavities 1-4 (aka Rack A)	RFS1 (cavities 1,2)	192.168.0.101
Cavities 1-4 (aka Rack A)	RFS2 (cavities 3,4)	192.168.0.102
Cavities 1-4 (aka Rack A)	PRC	192.168.0.103
Cavities 5-8 (aka Rack B)	RES	192.168.0.200
Cavities 5-8 (aka Rack B)	RFS1 (cavities 5,6)	192.168.0.201
Cavities 5-8 (aka Rack B)	RFS2 (cavities 7,8)	192.168.0.202
Cavities 5-8 (aka Rack B)	PRC	192.168.0.203

PRC=Precision Receiver Chassis

Reads cavity probe signals

RFS=RF Station

Provides RF drive; reads forward , reverse, detune signals

RES=Resonance/Interlock Chassis

Controls tuners; performs interlock logic

3. Start/Restart the EPICS IOC

- Log into LERF workstation or server (lcls01/2/3/lclsapp1 with individual user id)
- 2. Type lerfhome&

🔳 LCLS2 Home Screen: Electron Bear	m Systems (on Iclsa 💶 🗆 🗙
LCLS-II LERF Home Screen	Home Screen Exit
Applications Global	L1B
Magnet	
RF	—
Cryo System	—
Network	
Vacuum	

3. Click on box intersecting Network and L1B

F Subsystems	and Areas:	Network and IOCs	Home Screen	Ex
	Global L18			
All Magnet RF	Cryo SIOC:DB01:CR01			
Cryo System Network Vacuum	Magnet SIOCL18:MG01			
	HF SIDCL1B RF01 SIDCL1B RF02 SIDCL1B SSA01 SIDCL1B SSA02	CM 1 LIP CM 1 234 CM 1 254 CM 1 554		
	Vacuum SIOC:L1B:VA01			

4. Click on IOC of interest



5. Click on Reboot... Then click on Reboot Now!

4. View RF EDM displays

- a. Log into LERF workstation or server (lcls01/2/3/lclsapp1 with individual user id)
- b. Type lerfhome&

🔳 LCLS2 Home	Screen: Electror	ı Bean	n Systems (on Iclsa _	o x
LCLS-II LERF	Home Screen		Home Screen Exit	
	Applications	Global	L1B	
	Magnet			
	RF			
	Cryo System			
	Network			
	Vacuum		-	

c. Click on box intersecting RF and L1B

S-II Subsystem	s and Areas:	RF System Help_ Home Screen
	Globel GUNB LOB HTR	18 BC18 128 BC28 L3B EXT DOG BYP SLTH BSYH LTUH UNDH DMPH FEEH SLTS BSYS LTUS UNDS DUMPT FEES NEH FEH
All	Map and Status	
BPM/Toro/FC/BLen		
Feedback		
Magnet	Cavity	Cavity Cavity Cavity Cavity Cavity Cavity
Profile Monitor		
Wire Scanner		
Collimator/Motion	Cryomodule 2 - ACCL	4.18:0200
Laser		
RF		
Cryo System		
Event		1 2 3 4. 5. 6 7 8
Network		
Natr/Pwr/Gas/Smok		Oryomodule 3 - ACCL:L1B:0300
Vacuum	Cryomodule Displays	Waveforms
Temperature	Cavity Control	Hardware, Calibration, Cryo-
MPS		module 2
PPS	SSAs	Cryo- Sinale Cavity Cryomotivie
BCS		module 3 cryoinduite
ADS/X-Ray/Misc		
IOC:SYS0:AL00:M		rf_th_main.edl <sioc.sys2.al00.to< td=""></sioc.sys2.al00.to<>

L1B Overview Display

F Cavity omodule ACCL1.18.0200 Cavity 1	ACCL:L1B:0200 Cavity 1	All 8 Cavilies. Edit
Cardy Cardol SSA OF On More SSA. OF More SSLAF SSLA SSLA SSLA OF Sole OF On More SSA. Pare OF More SSLAF SSLA SSLA SSLA Pare OF Sole OF OF OF Description Pare OF Sole OF OF Description Description Description	Interfacts Conner 30 Apport Transmission Coupter Transmission Coupter Transmission Coupter Transmission Coupter Transmission Coupter Viscoum Bastrike Viscoum City Summary Storm. Summary	Cacher Cacher December
SEL4792EL/SEL Phare 0.00 degrees 100 0.000 waphude 0.000 150 MV 0.0000	StDer 188 20 EFICS Guerch Detect Cover daher Ausenburg EFICS Guerch Detect Cover daher Ausenburg EFICS Guerch Detect Cover daher Ausenburg EFICS Guerch Detect	Contry View. Fault if Self IF control 10 OFF (peet ref)
SEL RawPulse Phase Const. Cons	Mere Readback	M From Stations' MV/In Arg10.06 Prop. MV/In Prop. Station Prop. Station (Station Stations) (Station Station St
On Time 0118 ns Oo Stop Pulse Off Time 01018	If above values and all pupels by: In-Use Cavity Scale	Eron Car and Frid H Frid Country Hz Source H Frid Country
Stypper 0 tops //www. 2 tops //www	Disable Integrator	Randoms Cavaly 1 Overstew moceanedd Mare Cavaly 1

Single Cavity Display

5. Initialize/Checkout LLRF Hardware

Needed after power outage, hardware swap, etc.

RF System - Cryomodule Racks	s (on Iclsapp1.acc.jlab.org) 💷 🗆 🗙		
RF Hardware Cryomodule ACCL:L1B:0300	Exit		
Schematic	_		
	RF Private Network		
Rack A	Rack B		
Rack Hardware Init and Test	Rack Hardware Init and Test		
Resonance/Interlock (RES) Cavity 1 Cavity 2 Cavity 3	Resonance/Interlock (RES) Cavity 5 Cavity 6 Cavity 7		
30 Cavity 4	30 Cavity 8		
Power Supply	Power Supply		
26	26	DE Underen billelinden and Test	
LO Distribution	LO Distribution	RF Hardware Initialization and Test Cryomodule ACCL:L1B:0200 - Rack A •	Background process Exit
23	23	RFS and PRC	
RF Station (RFS2) • Cavity 1 Cavity 2	RF Station (RF52) • Cavity 5 Cavity 6	Run RFS/PR Rack Init and Te	
19	19		
(RFS1) Cavity 4	(RFS1) Cavity 8	Pass Rack Uneckout complete	
15	15	Resonance/Interlock	
Precision Receiver Chassis (PRC) • Cavity 1 Cavity 2 Cavity 3 11 Cavity 4	Precision Receiver Chassis (PRC) • Cavity 6 Cavity 7 Cavity 8	Initialize Chassis Go Complete Log]
		SW-FW Communication	_
RF CPU		Halt SW Comm Reset SW Comm	
		PRODUCTION	01/24/2019 16:18:48

a. Click on *Hardware…* (from either L1B Overview or Single Cavity display—see above).

- b. For appropriate rack (A or B), open display labelled Rack Hardware Init and Test...
- c. Execute RFS/PRC initialization and checkout. Click on Go

(The script will disable and then re-enable communication with EPICS.)

To view the rack test script output, click on Log...

١

It will open an xterm window and display the script output as it progresses.

	LLRF Rack Test Lo	File (on icisapp1.acc.jlab.org) _ 🗆
Computer Ref Rack Diagnostic F Haddwar Chydroddie ACCL L18 (200 - Rac Run Rack Self-Test Go	In add much bifiles to PROL In add much bifiles In add much bifin	File Contract plant(c)(nb.org)
Latest Self-Test Results	Defaulting device selection in chain from [ICODE Bavice selected for programming is in chain location; 0 Xilinx Kintex 7 interface selected Programming 932 Board IB packet format; 0	
Rack Running Law	ing cho could for rack A	Log
RFS1 Past		
RFS2		and the second s
PRC Pass		State of Concession, Name
Res/Intik PESS		
		LLRF Rack Test Log File (on Iclsapp1.acc.jlab.org)

RF Hardware Initialization and Cryomodule ACCL:L1B:0200	Test - Rack A ●	Background p	WOC633	Exit
RFS and PRC				_
Run RFS/PRC Rack Init and Test	Go Complete			
Pass Rack (checkout complete	20	19-01-24-15:16:	Log
Resonance/Interlock				_
Initialize Chassis	GoComplete	Log		
SW-FW Communication				
Hait SW Co	mm Reset SW Comm			
PRODUCTION			01	/24/2019 16:18:48

d. Initialize RES chassis. Click on Go

(The script will disable and then re-enable communication with EPICS.)

There are currently no automated checks for RFS<->RES communication. You'll need to look at the diagnostic display. From the Hardware display, for the appropriate rack, click on an individual chassis, then click on *Comm Diag...*

RF Hardwa Cryomodul	ire e ACCL:L1B:0200	Exit
	Schematic	
		RF Private Network
	Rack A	Rack B
	Rack Hardware Init and Test	Rack Hardware Init and Test
	Resonance/Interlock Cavity 1 (RES) Cavity 2 Cavity 3	Resonance/Interlock (RES) ● Cavity 6 Cavity 6
30	Cavity 4	30 Cavity 8
26	Power Supply	Power Supply 26
	LO Distribution	LO Distribution
23		23
	RF Station (RFS2) Cavity 3 Cavity 4	RF Station Cavity 7 (RFS2) Cavity 8
19		19
	RF Station Cavity 1 (RFS1) Cavity 2	RF Station Cavity 5 (RFS1) Cavity 6
15		15
	Precision Receiver Cavity 1 Chassis (PRC) Cavity 2 Cavity 2	Precision Receiver Cavity 5 Chassis Cavity 6 (PRC) Ocustu 7
11	Cavity 4	11 Cavity 8
	RF CPU	





The top row shows the RES status; the bottom the RFS status. In the *Rx* sections, the *Link Error* bit is set (blue) if there is a problem. (This snapshot shows no communication errors.) There is other useful data on this display too: the detune frequency measured by the RFS and a bit indicating if that value is valid and should be used; the permit bit sent from the Resonance/Interlock chassis to the RFS.

6. Cavity Characterization and Setup

There are a set of scripts used during initial cavity setup.

These are accessible from the *Characterization...* display. They are listed in the order in which they should be run.



With the exception of SEL phase offset, the calculated characterization parameters must be accepted by the user before they are 'in use', i.e. pushed to the primary EPICS PVs and used by software.

SSA Calibration

This measures the SSA output/input slope. The Results Summary will indicate if the scan was successful. The user may need to iteratively adjust the *SSA Drive Max* and re-run the scan. (This SSA Drive Max is also used as the upper limit when setting RF amplitude via the usual cavity controls.)

```
User Inputs:

SSA stimulus amplitude

Script Actions:

Drive SSA for about 200 microseconds.

At end of scan, leave RF off.

Script Results:

(action required to use)

SSA slope - ratio of output to input in normalized units

This value written to Newly Calculated; user must press Push to accept new

value
```

Detune Frequency Scan

Measure detune frequency offset from 1300 MHz. The scan range is +/- 10 kHz so it is recommended to use this when the cavity frequency offset is within that range. (At LERF, that initial tuning is done using a network analyzer and the frequency offset brought to about 1 kHz.)

User Inputs:

Scan Freq Offset: offset from 1300 MHz to use as scan center Drive Level: LLRF drive level

Script Actions:

Scan +/- 10 kHz about desired offset.

At end of scan, leave RF off.

Script Results:

(informational)

Measured detune frequency offset from 1300 MHz Measured cavity amplitude at that detune frequency

Pulsed SEL Calibration

Measures optimal SEL phase offset, cavity probe signal scale factor, and loaded Q. Leaves the cavity on in pulsed SEL mode

User Inputs:

LLRF drive level

Script Actions:

Run pulsed SEL RF at requested drive level.

At end of scan, leave RF in pulsed SEL.

Script Results:

(action required to use)

Cavity amplitude scale factor (rev wf method)

Loaded Q

These values written to *Newly Calculated*; user must press *Push* to accept new value(s)

(immediately in use)

SEL phase offset

Cavity Ramp-Up

Brings cavity on in CW SELAP mode by starting in pulsed SEL, increasing pulse length and amplitude, and locking amplitude and phase. Like Pulsed SEL Calibration, it also measures optimal SEL phase offset, cavity probe signal scale factor, and loaded Q. Leaves the cavity on in CW SELAP.

User Inputs:

Cavity amplitude goal Script Actions: Run pulsed SEL RF Incrementally lengthen pulse, until in SEL CW Switch to CW SELAP, locking phase and amplitude loops At end of scan, leave RF in CW SELAP at amplitude goal Script Results: (action required to use) Cavity amplitude scale factor (RevCal method) Loaded Q These values written to Newly Calculated; user must press Push to accept new value(s)

7. Basic LLRF Controls

When turning on a cavity, first select the desired *RF Mode* from these options:

- **SELAP** CW Self-Excited Loop with amplitude and phase locked. Functionally identical to GDR when the cavity detuning is small enough to allow lock. Unlike traditional GDR mode, it temporarily falls back to SELA when detuning increases.
- **SELA** CW Self-Excited Loop with amplitude locked. Tracks cavity natural resonant frequency.
- **SEL** CW Self-Excited Loop. Tracks cavity natural resonance frequency.
- **SEL Raw** CW Self-Excited Loop with raw amplitude control. Set amplitude using % of full drive scale instead of relying on the calibrated values used in ADES.
- **Pulse** Pulsed Self-Excited Loop. Set amplitude using % of full drive scale. Then use pulsed Go/Stop buttons.

Then set RF State to On.

The amplitude and phase controls are different between (a) modes SELAP, SELA, SEL and (b) SEL Raw, Pulse. On the cavity screen, the appropriate phase/amplitude control block will be highlighted in orange



See sections 9 and 10 for more details on SEL Raw and Pulse controls.

8. View RF Waveform Plots



Cavity Overview -- Cavity, Forward, Reverse signals for single cavity *Cryomodule Overview* -- Cavity, Forward, Reverse signals for all 8 cavities *More Cavity* -- Drop-down menu for single-cavity single-signal display From those displays, you can navigate to other cavities, other signals, or display a single signal for all 8 cavities. Example display shots:



9. Raw SEL Amplitude Control

If the SSA parameters and cavity signals are not yet fully calibrated, it may be desirable to run in SEL mode using raw drive control.



- a. Set *RF Mode* to *SEL Raw*
- b. Set RF State to On
- c. Set *Drive Level*. *Drive Level* is set in percentage of full drive scale. Its upper limit is slaved to the SSA max drive level, which can be set from the Expert phase/amplitude display. Modifying that limit is an expert function.





- a. Set *RF Mode* to *Pulse*.
- b. Set RF State to On.
- c. In the SEL Raw/Pulse block, set Drive Level and On Time. Click on Go.
- d. When done, click on Stop.
- e. To update *Drive Level* or *On Time*, enter new values and then click on *Go* again. The *Go* button will be highlighted in yellow to remind you of this.

Note that the total pulse on/off cycle length is determined by the waveform configuration settings. Click on *More...* for the SEL controls display, which has more detail on this:





11. Control Stepper Motor Tuner

From the *Stepper* block you can enter number of steps and then click the green arrow to go in one direction or the other. (Relationship between direction and frequency is not yet known.) Click on *More...* for the detailed single tuner display.



12. Control Piezo Tuner

From the *Piezo* block you can control piezo enable/disable, mode, and DC offset. Click on *More...* for the detailed piezo tuner display.

Recommended piezo workflow:

1. Start with piezo disabled.

2. The bias voltage is used to keep the piezo operating near the middle of its range. Set *Bias* to a reasonable value, nominally 25 V. This is not expected to change often (if at all).

3. Set piezo to DC mode. Enable piezo.

4. Adjust steppers and piezo DC offset to zero detune frequency.

5. Set piezo to Integrator mode. Using the setting from 2 as a starting point, firmware continuously adjusts the piezo as needed to zero detune frequency. Note that the *Detune from RFS* must be Valid for the integrator to function.

SRF Cavity Tuner Control - Piezo Cryomodule ACCL:L1B:02100 Cavity 1		All 6 Cavities Exit
Piezo Tuner	_	DC Offset
Enabled Enable Disable	,	Only used in DC mode is added to bias
DC DC Ir	ntegrator	0 100
Control Word	Status Word	0.0 V 0
eff read DAC Continuous DAC Sync Error Reset Debug Mode Debug Mode Debug Mode DAC Enable m Board Enable 0.0 V Integrator 0.0 Hz	ADC Errors DAC Busy ADC Busy ADC Busy	Info Recommended workflow: 1. Start with piezo disabled. 2. Set hias voltage to reasonable value. This is not expected to change often (rif at al). 3. Set piezo to DC mode. Enable piezo 4. Adjust steppers and piezo DC offset to zero deture frequency. 5. Set piezo to DC - Indegrador Using the bit them continuously adjust piezo as needed to zero deture frequency. WARING. The transition tom DC-Integrator to adjump to the DC - setting This will be bod in a future FVSW release.
Detune from RFS 0.0 Hz Not val	d	
Diagnostic Readback		
Controller Select Detane Source Integrator Enable Bias Bias Piezo Source DC Offset Raw	Nopali/ - 01 - 02 - 02 - 02 - 0 - 0 - 0 - 0 - 0 - 0 - 0 - 0	Integrator Max
PRODUCTION		05/22/2019 10:53:33

6. If you observe an offset (if you can see in the phase waveforms that the detune frequency is not exactly zero but *Detune from RFS* shows 0 Hz), you may enter an *Integrator Setpoint* to compensate.

WARNING: The transition from Integrator to DC is not yet smooth. The DAC output will jump to the DC setting. This will be fixed in a future FW/SW release.

State Production (State Production (StateProduction (State Production (State Production (State Production (13. Drive	Cavity	With Sir	nple T	one Signa
Schulp Codel India SSA OF OF India SSA SSA OF OF More SSA FF More SSA	SRF Cavity Cryomodule ACCL:L1B:0200 Cavity 1	ACCL:L1B:0200) Cavity 1	All 8 Cavitie:	Exit
SEL RawPute Description Cave Rababac Cave	Canly Contol SSA OF ON MARKES NP Molo SSE SELA SELA SEL SSE MARK S PP State OF ON OP 1 margo Dev 1 margo SELAP/SELA/SEL Phase 100 00 00 Amprilude 10 50 00 00 0 00 00 0 00 00 0 00 00 0 00 00 0 00 0	A use 7	Hinfold Couplet Temperature Couplet Temperature Couplet Temperature Couplet Temperature Couplet Temperature Couplet Temperature Couplet Temperature Couplet Couplet Couplet Couplet Couplet Couplet Couplet Couplet Couplet Couplet Couplet Couplet Couplet Couplet	And Unlach All Depender Depender Cavity View.	RF Createrier SEL Enable SEL Enable SEL Enable SEL Enable SEL Enable Market SEL Enable SEL Ena
On Time 0.166 mm 0.0 500p Price Of Time 0.000 Find 0.000 None Details Carter Carter Stepper Preco Carter Carter Image: Carter Disable Carter More Carter Image: Carter Disable More Carter More Carter Image: Carter Disable More Carter More Carter Image: Carter None Tomo More Carter	SEL RawPute Phase -0.3 degrees -100 -0.76 Office 21.0 % 0 21 Level 21.0 % 0 21	180	More Readback Cavity Constant MW Forward Constant W Reverse Constant W	From Amplitude From Gegrees Fvid Powe (only degrees	Gradent DOT MV/m in SEL) Counts
Stepper Pieco Wandoms 9 taps 5000000 Enable Disable Cave 1 Crysmadule Overview. 0 taps 000	On Time 0.155 ms Go Step Putre Off Time 0.000 (0.000) 0.000 (0.000)	More	If above values are all purple, try: In-Use Cavity Scale	From Cas and Five Free Counte	Detune Hz Source Hz Source
		le Disable DC Integrator 0	0 Blas 7 More Hardy	forms ty 1 Overview cryce reconverview ore Cavity 1 tsplays vare Calibratic	msdale Overview_

a. Click on Tone...

SRF To	ne Test - AC	CL:L1B:0300 (o	on lclsapp1.acc.jlab.org) _ 🗆 ×
Simple Tone Test Cryomodule ACCL:L1B:030	00			Exit
Tone Test				
Cavity		Within each o only one can be	cavity pair, one at a time	
	1		DAC Counts (0-32767)	
1 <u>On</u>	Off	Off	0 0	Expert
2 <u>On</u>				_
3 On				
4 On	Off	Off	0	Expert
]			
5 <u>On</u>	Off	First Chan	30000 30000	Expert
6 <u>On</u>				
7 On]			
8 On	Off	Off	0	Expert
	1			

- b. For desired cavity, click on On, then enter number of DAC Counts...
- c. When done, click on Off

Note that these controls override the RF Mode and Off/On settings. When you turn the tone off, the RF will return to its previous state.

14. Interlocks

The interlock/resonance chassis executes the interlock logic and sends a per-cavity RF Permit to the RFS chassis. If that permit is not set, the RFS inhibits LLRF drive. Interlocks latch and must be unlatched by a user before RF is again permitted.

All interlocks use hardware signals with the exception of the cryo interlock, which read 2 EPICS PVs from the JLab control system. The interlock is faulted if either of these PVs is offline.

The cavity overview display provides high-level interlock status and unlatch.

SRF Cavity Cryomodule ACCL:L1B:0200 Cavity 1	ACCL:L1B:0200 Cavity 1	All 8 Cavities Exit
Cavity Control	Interlocks	RF Controller
SSA OF ON More SSA. RF Mode SEL SELAP SELA SEL SEL Raw Purse RF State OF ON Depart. Characterization	Corre Steper Tenperature 1 Coupler Tenperature 2 Coupler Vacuum Beanline Vacuum Cryo Summary	More Catheory SEE Enable SEE Enab
(0-1 raige)	Summary	
SELEVISE VOE: Phase 0000 Amplifude 0000 [\$0 Mrv 0 5000	SdDev 180 EPICS Guench Detect 20 Carrent Lather Lather Regess Unterpas	Fead and Four Fourt in South Fourter and the second of t
SEL Raw/Pulse	More Readback	Gradient
Phase -0.8 degrees 180 -0.76 Office 21.0 % 0 21	180 Cavity Course 80 Forward Reverse Course	mW From Amploude MV/m Amploude MV/m W compared degrees Fud Power (only in SEL) counts
On Time 0.160 ms Go Stop Pulse Of Time 0.00110 0.00010 0.00010	If above values are all purple, try. R In-Use Cavity Scale	Counter From Cavity and Pave Free Counter Counter Counter
Stepper 0 tops room 0 tops ro	isable Integrator 0 Bias	Waveforms Cetylogramma Crystmodule Overview. Wore Cevity 1. More Contry 1.
Motor Moving More_ Is added to blas	Mare	Hardware Calibration Tone
PRODUCTION		05/22/2019 10:30:20

Logic details, temperature thresholds, and bypass control are available on the individual cavity or cryomodule interlock displays.



15. EPICS Quench Detection

Quench detection will eventually be implemented in firmware, but for now we have a simple EPICS level check that is used. Because this was a quick temporary solution, this fault does not use the standard interlock shutoff path, but simply sets *RF State* to *Off*. To recover RF, click the on *Acknowledge* and then set *RF State* to *On*.

SRF Cavity Cryomodule ACCL:L1B:0200 Cavity 1	ACCL:L1B:0200 C	Cavity 1	All 8 Cavities Exit
Carity Control SSA COT On RF Mode RF State Cotton C	More SSA. SEL SEL Raw Pulse 7 Expert. Characterization.	Interfacts Current Cathod Stepper Temperature 1 Coupter Temperature 1 Coupter Yacoustance 2 Coupter Yacoustanc	Unlach All Coabors 4 control W
Phase 1712 0.0 degrees Amplitude 10.0 [5.0 MV	-180 0.0080 180 StdDev	EPICS Guench Detect Commit Lather Advocation Bypass Unhypass Not Evypasse Not Evypasse Sets F	Anpi Anpi F control F control
SEL RawPulse Prise Creat Leve Leve Deve Deve Con Time Con Time Con Time Con Time Con Time Con Time Control	-100 -0.70 100 0 21 00 0 300p 100 101 Meres	Revolución Caroly million Porvand W Carol o Reverse W Carol o If above values are all popole, by Revert	Ordiner Applicate From Carbon Graff Poor Graff Poor Graff Poor Graff Poor Graff Poor Graff Poor From Carbon From Carbon Counter
Stepper	Pleco Ensole Dwates DC Integrator of the second data of the second dat	Bias Wore Displays	ree. Cryomsdute Overview. www.de L. Calderation. Tone. 05/2/2011 10:30:24

This check compares the measured cavity probe amplitude signal with a calculated cavity amplitude that is based on forward power. If the cavity probe value is less than half of the value calculated from forward power, it is a fault.

Idiosyncrasies of this check: Latched status is provided to notify users of a recent fault, but the fault does not need to be acknowledged in order to turn the RF back on. It is recommended to acknowledge the fault before turning on RF so any future transient fault is caught.

II. Occasional Issues

1. Mystery Rack Checkout Error

We occasionally see a problem during the first cryomodule rack A checkout. This is what it looks like:

LLRF Rack Test Log File (on lclsapp1.acc.jlab.org)	_	×
132.168,0,102 Mrite to /data/lcls=llrfcpu01/llrf/./live pro regmap.ison		
192.168.0.102		
set_lims 0 0		
Signal min/max 0/0, amplitude 0.0 0.0, rms error 0.00 0K		
Signal min/max 0/0, amplitude 0,0 0,0, rms error 0,00 0k		
crc_errors cik_status_out dac_iq_phase shell_U_dsp_use_tiber_iq [601/3, 2, 1, 1]		
Signal win/max -2032/2367, amplitude 2032.7 9.9, rms error 63.88 BAD		
Signal min/max 0/0, amplitude 0.0 0.0, rms error 0.00 OK		
crc_errors clk_status_out dac_iq_phase shell_0_dsp_use_fiber_iq [60179, 2, 1, 1]		
set_lims 0 79000		
Signal min/max -6130/8123, amplitude 8130,0 23,7, rms error 0.52 UK		
Signal min/max 0/0, amplitude 0,0 0,0, rms error 0,00 0k		
set lins 1 19750		
Signal min/max -2032/2032, amplitude 2032.1 5.9, rms error 0.49 OK		
Signal min/max 0/0, amplitude 0.0 0.0, rms error 0.00 OK		
crc_errors clk_status_out dac_iq_phase shell_1_dsp_use_fiber_iq [60179, 2, 1, 1]		
set_liws 1 /9000 Signal pin (any -9170/2019) analituda 9170 0 27 7 pro apren 0 52 0K		
Signal win/wax Cols/Colls, amplitude ols/, 23,7, rms error 0,32, uk Signal win/wax (0,0, amplitude 0,0,0, rms error 0,0,0 K		
che errors clk status out dae ig phase shell 1 ds use fiber ig [60179. 2. 1. 1]		
set_lims 0 0		
Signal min/max 0/0, amplitude 0.0 0.0, rms error 0.00 DK		
Signal min/max 0/0, amplitude 0.0 0.0, rms error 0.00 OK		
crc_errors clK_status_out dac_iq_phase shell_v_dsp_use_fiber_iq [601/9, 2, 1, 1] cri		
		30000

RF Rack Diagnostics - ACCL:L1B:0200 - Rack B (on lclsapp1.acc.jlab.org)	
RF Hardware Cryomodule ACCL:L1B:0200 - Rack B Exit	
Run Rack Self-Test	
Go Complete Abort	
Latest Self-Test Results	
Rack B	_
RCC Pat Script aborted. Try again. 2018-06-11-17:09-48	Log
RFS1 Pass	
RFS2 Pass	
PRC Pass	
Res/Intik Pass	

It is an intermittent failure and is not understood. You'll have to simply re-run rack checkout and hope it passes. (We have observed that if the system was previously set up correctly and there has been no outage/hardware swap since, it will probably work fine in spite of this error.)

2. Recover Non-Updating EPICS Waveforms

Once in a while, I've seen the EPICS waveform data stop updating. Displays will look like this:



If you see this and nothing else seems to be wrong, try clicking the *Reset* button on the cavity display. This will briefly halt and then reset communication between the software and all LLRF chassis in this cryomodule.

3. Ping Test

To test if a chassis pings from a CPU:

- Log into LERF workstation or server (lcls01/2/3/ lclsapp1 with individual user id)
- b. Log into cpu (using CPU Node Name from Section 1):

iocConsole <cpuname>

OR

ssh laci@<cpuname>

(If prompted for login, type 'laci' and hit enter.)

c. Type: ping <ip>

4. View the EPICS IOC Console

- a. Log into LERF workstation or server (lcls01/2/3/lclsapp1 with individual user id)
- b. iocConsole <iocname>
- c. To exit viewer, press these 3 keys together: Ctrl, a, d.
- d. To scroll up in viewer, press these 3 keys together: Ctrl, a, [. Then use arrows to move up/down. To exit scroll mode, press these 3 keys together: Ctrl, a,].

(If you inadvertently kill the ioc, you can restart it using the instructions in section 2.)

5. RF 'Background Process'

Much of the current RF functionality (rack checkout, pulse control, cavity ramp, etc.) is performed by scripts external to the EPICS IOC. This is facilitated by a continuously running background process that is driven by EPICS PVs. This allows us to execute these functions from EPICS PVs on EDM displays—and not have to manually run scripts from the command line.

On every display that relies on this, there is a button *titled Background process*. If the process is not running, there will be a red rectangle around that button. Click on that button to open a display from which you can start/restart the process. Example:



This process will not successfully launch if the EPICS PVs it relies on are not all online. Both LLRF EPICS IOCs must be on.