LERF RF User Guide

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I. Standard Controls and Information

1. CPUs and IOCs

JLab Cryomodule Number	LCLS-II Cryomodule Name	CPU Node Name*	EPICS IOC Name*
1	ACCL:L1B:0200	lcls-llrfcpu01	sioc-l1b-rf01
2	ACCL:L1B:0300	lcls-llrfcpu02	sioc-l1b-rf02

*CPU Node Name is referred to as <cpuname>in the commands shown below. EPICS IOC Name is referred to as <iocname> in the commands shown below.

2. Chassis IPs

These are the IP addresses used in the LLRF internal network. They are the same for each cryomodule.

Rack	Chassis	IP
Cavities 1-4 (aka Rack A)	RES	192.168.0.100
Cavities 1-4 (aka Rack A)	RFS1 (cavities 1,2)	192.168.0.101
Cavities 1-4 (aka Rack A)	RFS2 (cavities 3,4)	192.168.0.102
Cavities 1-4 (aka Rack A)	PRC	192.168.0.103
Cavities 5-8 (aka Rack B)	RES	192.168.0.200
Cavities 5-8 (aka Rack B)	RFS1 (cavities 5,6)	192.168.0.201
Cavities 5-8 (aka Rack B)	RFS2 (cavities 7,8)	192.168.0.202
Cavities 5-8 (aka Rack B)	PRC	192.168.0.203

PRC=Precision Receiver Chassis

Reads cavity probe signals

RFS=RF Station

Provides RF drive; reads forward , reverse, detune signals

RES=Resonance/Interlock Chassis

Controls tuners; performs interlock logic

3. Start/Restart the EPICS IOC

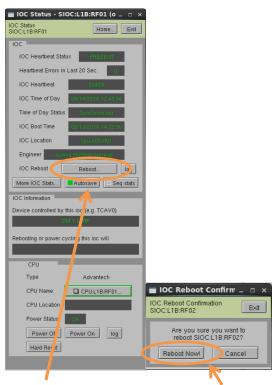
- Log into LERF workstation or server (lcls01/2/3/lclsapp1 with individual user id)
- 2. Type lerfhome&

LCLS2 Home Screen: Electron Bea .CLS-II LERF Home Screen	Home Screen
Applications Globa Magnet	d L1B
RF Cryo System	
Network	
Vacuum	

3. Click on box intersecting Network and L1B

F Subsystems and Areas:	Network and IOCs	Home Screen
All Magett Br Cryo System Network Vacuum	CH I SOM CH I SOM	
ODUCTION	rðvik_116_main.edi	08/20/2018 17.43

4. Click on IOC of interest



5. Click on 'Reboot'. Then click on 'Reboot Now!'

4. View RF EDM screens

- Log into LERF workstation or server (lcls01/2/3/lclsapp1 with individual user id)
- b. Type lerfhome&

🔳 LCLS2 Home Sc	reen: Electro	n Bean	n Systems (on Iclsa	×
LCLS-II LERF Ho	me Screen		Home Screen Exit	
	Applications	Global	L1B	
	Magnet			
	RF			
	Cryo System		—	
	Network			
	Vacuum		-	
	-			

c. Click on box intersecting RF and L1B

All May and Statur - BPM/TorP/CRen Feedback Magnet Profile Nonitor Were Scame Collimator/Motion Later RF Cytyo System Event Network	8 HTR 116 BC18 L28 BC28 L38 EXT DOG BVP	SUTH BOWH LTUH UNCH DMPH PEEN SUTS BOYS LTUS	UNDS DUMPT FEES NEH FEHI
BPM/TaroF/OBLen Feedback: Magnet Profile Monitor Wite Scame Profile Monitor Wite Scame RF Cyto System Event Nethork Vacuum Temperature NPS ESex	Certy Certy Carty Carty Cart		
Magnet Profile Nontroc Wins Scanner Collimater/Arction Later RF Cryo System Event Nethorock WattiPwrdox Mather Profile PPS Cryoensolute Displ Cryoensolute Displ Cryo	Centry Centry Centry Centry Centry Centry Centry 5-		
Magnet Profile Nonitor Wen Scanner Collimator/Motion Laser RF Cryo System Event Network. WathPwrdas/Smok Vacuum Temperature NPS PPS SEAS	Cavity Cavity Cavity Cavity Cavity 5		
Profile Monitor Wrs Scanner Collimate/Monitor RF Cryo System Event Network WettPer/Urs/Sas/Snot Vacuum Temperature NPS PPS Essis	Cevity Ce		
Profile Nonitor Ware Scanner Constant/Action Learer RF Cyto System Event Network Wate/Fwr/CaaS/mok Vacuum Temperature NPS PPS Esers		rity Cavity Cavity Cavity Cavity	
Collinator/Motion Laiser RF Cyto System Event Network Wate/Purch/Gal/Smok Vacuum Temperature NPS PPS Savis		• • • • • • • • • • • • • • • • • • •	
Colimator/Motion Laver PF Cryo System Event Neteronik MattiPhur/Gas/Sinok Vacuum Temperature MPS PPS			
RF Cryg System Event Network Vacuum Temperature NPS PPS	e 2 - ACCL:L1 B:8280		
Cryo System Event Network Watr/Mw/Gas/Smok Vacuum Temperature MPS SSAt			
Event Network Vatr/Wr/Gas/Snok Vacuum Temperature MPS SSAs			
Network Vatu/Pwr/Kas/Smok Vatu/Pwr/Kas/Smok Temperature NPS PPS SSAs	Cavity Cavity	Cavity Cavity Cavity Cavity	Cavity Cavity
Watr/Pwr//Gas/Smok Vacuum Temperature MPS PPS SSAs	1 2	Cavity Cavity Cavity 6	7
Vacuum Cryomedule Disple Temperature Cavity Co MPS SSAs			
Temperature Cavity Co MPS PPS SSAs	Cryomodule 3 - ACCL:L1B:0300		
MPS Cavity Co	ays	Waveforms	
PPS SSAs	ontrel Hardware Calibration	Cryo- module 2 Single Cavit	v Crvomodule
PP5		module 2	
BCS	han	Cryo- Single Cavit	y Cryomodule
		modulé 3 Single Cave	
ADS/X-Ray/Misc			
SIOC:SYS0:AL00:M		rf_11b_main.edl	<sioc:sys2:al00:to< td=""></sioc:sys2:al00:to<>





Single Cavity Display

5. Initialize/Checkout LLRF Hardware

Needed after power outage, hardware swap, etc.

a. Click on Hardware... (from either L1B Overview or Single Cavity display—see above).

RF System - Cryomodule Racks (on Iclsapp1.acc.jla	ab.org) _ 🗆 🗙	
RF Hardware Cryomodule ACCL:L1B:0300	Exit	
Schematic		
RF Priv	ate Network	
Rack A Rack B		
Resonance/Interlock Cavity 1 Ravity 2 Civity 3 Resonance/Interlock. 30 C vity 4 7 Power Supply 26 26	Cavity 5 Cavity 6 Cavity 7 Cavity 8	
LO Distribution 23 RF Station	Cavity 5 Cavity 6 Cavity 7	BF Hardware Initialization and Test Badground process. Exit Cryomodule ACCLL1B:0200 - Rack A Badground process. Exit
RF Station Cavity 3 (RFS1) Cavity 4 15 Cavity 4 Precision Receiver Cavity 1 Cavity 2 Cavity 2 (PRC) Cavity 3 11 Cavity 4	Cavity 8 Cavity 5 Cavity 6 Cavity 7 Cavity 8	Resonance/Interlock Initialize Chassis Go Complete Log
RF CPU		SW-FW Communication Halt SW Comm Reset SW Comm
		PRODUCTION 01/24/2019 16:18:46

b. For appropriate rack (A or B), open display labelled Rack Hardware Init and Test...

c. Execute RFS/PRC initialization and checkout. Click Go

(The script will disable and then re-enable communication with EPICS.)

To view the rack test script output, click on Log...

It will open an xterm window and display the script output as it progresses.

	LLRF Rack Test Log File (on IcIsapp1.acc.jlab.org) _ 🗆 ×
	Will load new bitfiles to FPGAs
Computer	Back R Hill execute Icls2_rack.sh from /usr/local/cls/package/Icls2_llf/software/prc Hill source /usr/local/cls/spics/ioc/wanov/Ascility/GafythenLinuRT.sh Hill writefiles to /data/icls=Infequd/Infe
~	Path to UF2PRE files is /usr/local/lcls/package/of2pre
RF Rack Diagnostics -	Will write status to BCCL+L1E+0200+PBCKB+SELETEST MSC
RF Hardware	Beginning checkout for radk R System () is in Junal?, Setting puthon LLLIBMPK/PARH before proceeding. /uur/local/icityAckage/loig_lift/software/pro Bowd IB packs format; 0
Cryomodule ACCL118.0200 - Rack A	There are 1 devices in the chain:
Run Rack Self-Test	0x384c093 - Xilinx Kintex 7 180T
	Loading bitfile: /uor/local/lcls/package/lcls2_llrf/software/prc/,,/,./firwware/prc/prc-qf2-20180406b.bit Bergin name; prc/User1000FFFFFFFFFFFFFFFferion=2017.1 Bergin name; fl200ffg5f
Go Flatting	Build date: 2018/04/06 Build date: 2018/04/06
	Length: 6692572 bits
	Befaulting device selection in chain from IBODE Device selected for programming is in chain location; 0 (link Kinter, Tinteface selected
Latest Self-Test Results	Xiinx Kintez / Interface selected Programming
	992 Board ID packet forwat: 0
Rack Running Edward	Checkand for racking 2016 doi:1110.0011 Log
RFS1	
RFS2	
PRC Rest	
Res/Indik Fast	
	LLRF Rack Test Log File (on IcIsapp1.acc.jlab.org)
RF Hardware Initialization and	
Cryomodule ACCL:L1B:0200	
Cryomodule ACCL:L1B:0200	
Cryomodule ACCL:L1B:0200 RFS and PRC	
Cryomodule ACCL:L1B:0200	
Cryomodule ACCL:L18:0200 RFS and PRC Run RFS/PRC	- Rack A • Exit
Cryomodule ACCL:L18:0200 RFS and PRC Run RFS/PRC Rack Init and Test	Go Company
Cryomodule ACCL:L18:0200 RFS and PRC Run RFS/PRC Rack Init and Test	- Rack A • Exit
Cryomodule ACCL:L18:0200 RFS and PRC Run RFS/PRC Rack Init and Test	Go Company
Cryomodule ACCL:L18:0200 RFS and PRC Run RFS/PRC Rack Init and Test	Go Company
Cryomodule ACCL:L1B:0200 RFS and PRC Run RFS/PRC Rack init and Test	Go Company
Cryomodule ACCL:L1B:0200 RFS and PRC Run RFS/PRC Rack init and Test	- Rack A
Cryomodule ACCL-L1B-0200 RFS and PRC Run RFS/PRC Rack Init and Test [Past 1997] Resonance/Interlock	Go Company
Cryomodule ACCL:L18:0200 RFS and PRC Run RFS/PRC Rack Init and Test Resonance/Interlock Initialize	- Rack A
Cryomodule ACCL:L18:0200 RFS and PRC Run RFS/PRC Resonance/Interlock Initialize Chassis	- Rack A
Cryomodule ACCL:L18:0200 RFS and PRC Run RFS/PRC Rack Init and Test Resonance/Interlock Initialize	- Rack A
Cryomodule ACCL-L18-0200 RFS and PRC Run RFS/PRC Rack Init and Test Resonance/Interlock Initialize Chassis SW-FW Communication	- Rack A • Barlyround process. Ext Go Complete 2015-01-01-11 Log. Go Complete Log. Image: Complete Complete
Cryomodule ACCL:L18:0200 RFS and PRC Run RFS/PRC Resonance/Interlock Initialize Chassis	- Rack A • Barlyround process. Ext Go Complete 2015-01-01-11 Log. Go Complete Log. Image: Complete Complete
Cryomodule ACCL-L18-0200 RFS and PRC Run RFS/PRC Rack Init and Test Resonance/Interlock Initialize Chassis SW-FW Communication	- Rack A • Barlyround process. Ext Go Complete 2015-01-01-11 Log. Go Complete Log. Image: Complete Complete
Cryomodule ACCL-L18-0200 RFS and PRC Run RFS/PRC Rack Init and Test Resonance/Interlock Initialize Chassis SW-FW Communication	- Rack A • Barlyround process. Ext Go Complete 2015-01-01-11 Log. Go Complete Log. Image: Complete Complete

d. Initialize RES chassis. Click Go

(The script will disable and then re-enable communication with EPICS.)

6. View RF Waveform Plots

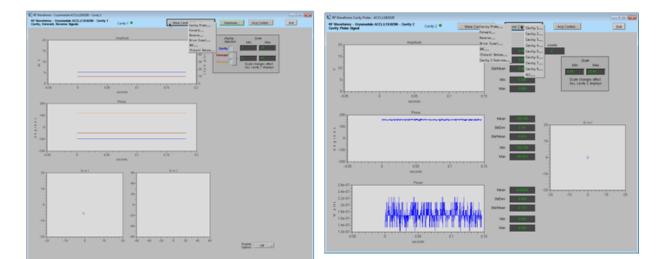
SRF Cavity - ACCL:L1B:0210		
SRF Cavity Cryomodule ACCL:L1B:0200 Cavity 1		All 8 Cavities Exit
Cavity Control	Interlocks	
Phase 1872 0.0 degrees 180 Amplitude 00 6.0 MV 0 RF State 01 Orr On RF Mode 56L SELAP SELA SEL 7 Expert. SSA More SSA. Cavity	0 0000 180 Stepper Temperature 6 0000 20 Coupler Temperature 1 Coupler Temperature 2 Coupler Vacuum Beamine Vacuum CHL Ready CHL Ready Future He Izevel Future He Pressure Summary	Unlatch All Unlatches
Readback	Detune	Cryomodule View Cavity View
Cavity Gradient 0003 MV/m Forward Power 0000 Watts Forward Phase 00000 Reverse Power 00000 Watts Reverse Phase 000000	degrees more coming soon	Tum off
Veronorms Cavity 1 Overview Cavity Proverview Cryomodule Overview Prove Coo	al falibration Piezo Tuner	av Characterization Tone Test SEL Phase & Pulse Feedback Parms
PRODUCTION IAC.		01/29/2019 09:51:15

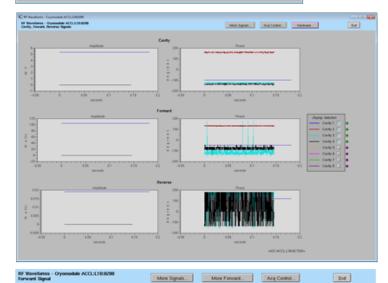
Cavity Overview -- Cavity, Forward, Reverse signals for single cavity

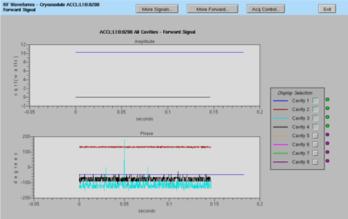
Cryomodule Overview -- Cavity, Forward, Reverse signals for all 8 cavities

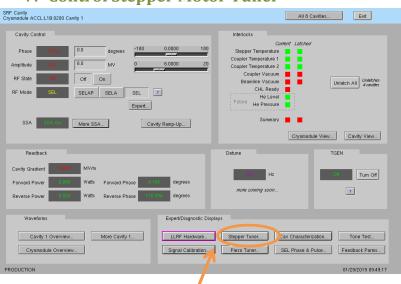
More Cavity -- Drop-down menu for single-cavity single-signal screen

From those screens, you can navigate to other cavities, other signals, or display a single signal for all 8 cavities. Example screenshots:



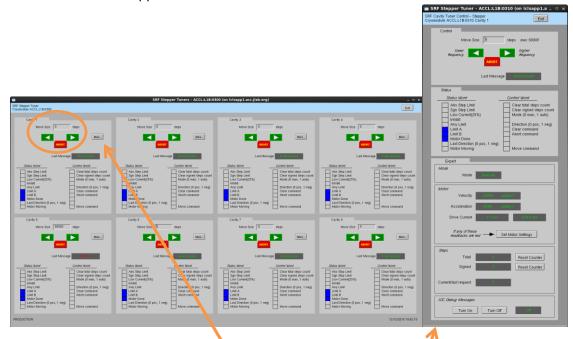






7. Control Stepper Motor Tuner

a. Click on Stepper Tuner...



b. 8-cavity screen. From here you can enter number of steps and then click the green arrow to go in one direction or the other. (Relationship between direction and frequency is not yet known.) Click More... for single tuner screen

8. Control Piezo Tuner

SRF Cavity Cryomodule ACCL:L1B:0200 Cavity 1	All 8 Cavities Exit
Cavity Control Phase 182.2 0.0 degrees Ampitude 00 8.0 MV 0 6.0000 20 8.0 RF State 0ff 0ff 0ff RF Mode SEL SSA SEL More SSA. Cavity Ramp-Up	Interlocks Current Latched Stepper Temperature Coupler Temperature Coupler Vacuum Beamline Vacuum CHL Ready Future He Everi Summary Cryconodule View Cavity View
Readback Cavity Gradient MV/m Forward Power Watts Forward Phase degrees Reverse Power Watts Reverse Phase degrees	Detune TGEN
Waveforms Expert/Diagnostic Displa Cavity 1 Overview Cryomodule Overview Signal Calibration.	ys Stenner Tuner Cav Characterization Tone Test. Plezo Tuner SEL Phase & Pulse Feedback Parms
PRODUCTION	01/29/2019 09:49:17

a. Click on Piezo Tuner...

SRF Piezo T		Tuners - AC	CL:L1B:0300 (on Iclsapp	1.acc.jlak	o.org)	_ □ >
Cryomodule	ACCL:L1B:03	00					Exit
Piez	o Control						
	Enabl	ie resets DAC se	etpoint to 0		DAC Setpoir	nt	
1	Enable	Disable	Not enabled	<u>)</u> 0.0	V	.o v 🛛	More
2	Enable	Disable	Not enabled	0.0	V (.0 V	More
3	Enable	Disable	Notenabled	0.0	V	.0 V	More
4	Enable	Disable	Not enailed	0.0	V	.0 V	More
5	Enable	Disable	Not enabled	0.0	V	.0 V	More
6	Enable	Disable	Not enabled	0.0	V	.0 V	More
7	Enable	Disable	Not enabled	0	V	.0 V 0.	More
8	Enable	Disable	Not enabled	0.0	_ v	0.0 V	More

b. 8-cavity screen. From here you can enable the piezo tuner and enter a DC DAC voltage. Click More... for single piezo tuner screen

		-	0
SRF Cavity Cryomodule ACCL:L1B:0200 Cavity 1			All 8 Cavities Exit
Cavity Control	A SEL ?	180 Interlocks 20 Stepper Temperature 20 Coupler Temperature 1 20 Coupler Temperature 2 Coupler Vacuum Beamline Vacuum CHL Ready Future He Pressure	urrent Latched Unlatch All Undethes 4 eavities
SSA More SSA	Expert	Summary	Cryomodule View Cavity View
Cavity Gradient 0.003 MV/m Forward Power 0.009 Watts For	ward Phase degrees erse Phase tites degrees	Hz more coming soon	Tum Off
Waveforms Cavity 1 Overview More Cryomodule Overview PRODUCTION	Expert/Diagnos Cavity 1 Signal Calibra	are Stepper Tuner	Cav Characterization Tone Test SEL Phene & Pulse Feedback Parms 01/29/2019 0949:17

9. Drive Cavity With Simple Tone Signal

a. Click on Tone Test...

SRF To Simple Tone Test	ne Test - ACCL	.:L1B:0300 (a	on Iclsapp1.acc.jlab.org	
Cryomodule ACCL:L1B:030	10			Exit
Tone Test		Within each o	ouitu poir	
Cavity		only one can be	one at a time	
1 <u>On</u> 2 <u>On</u>		Off	DAC Counts (0-32767)	Expert
3 On 4 On	or 📕	Off	0 0	Expert
5 On 6 On	Off	First Chan	30000 30000	Expert
7 <u>On</u> 8 <u>On</u>		Off	0 0	Expert

- b. Turn desired cavity 'On', then enter number of DAC counts...
- c. When done, click 'Off'

10. Run RF	In SEL Pulsed Mode	
SRF Cavity Cryomodule ACCL:L1B:0200 Cavity 1	All 8 Cavities Exit	
Cavity Control Phase 100 Amplitude 0 1 B 0 MV 0 FF State 0 0 0 0 MV 0 FF Mode SEL SELAP SELA Expert SSA 1 More SSA	0.0000 180 0.0000 180 0.0000 20 Coupler Temperature 1 1 Coupler Temperature 2 1 Cutter Temperature 2 1 Cavity Ramp-Up. Summary Cavity View Cavity View	
Readback Cavity Gradient Could Gradient Forward Power Reverse Power Could Gradient Reverse Power Reve	Detune TGEN Detune TGEN I to to degrees more coming soon	
Waveforms Cavity 1 Overview	Expert/Diagnostic Displays LLRF Hardware Stepper Tuner Cav Characterization Tone Test Signal Calibration Piezo Tuner SEL Phase & Pulse Feedback Parms	
PRODUCTION	01/29/2019 09:49:17	

a. Click on SEL Phase & Pulse...

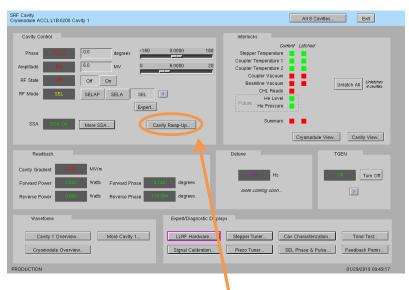
The settings/options for pulsed mode are more complicated than you'd think. It's a good idea to read the README at the bottom of the screen.



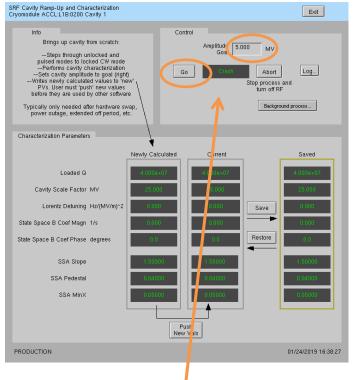
- b. Enter desired amplitude (settings will be 'yellow' if they do not match Current/Last In Use)
- c. Enter desired RF pulse length
- d. Click Go
- e. When done, click Stop
- f. To update amplitude or time settings, enter new values and then click Go again

11. Ramp Cavity to CW/SELAP and Perform Cavity Characterization

This is used to bring up a cavity 'from scratch' or if there is some need to re-characterize the cavity/SSA. You do not need to run this every time you turn a cavity on.



a. Click on Cavity Ramp-Up...



- b. Set Amplitude Goal and click Go
- c. Future (not yet done 1/24/2010): the script will write is calculated characterization parameters to the Newly Calculated values on the screen. You can review these and if they seem reasonable, click Push New Vals. You can also save the Current values as a known good set—to possibly restore in future.

II. Occasional Issues

1. Mystery Rack Checkout Error

We occasionally see a problem during the first cryomodule rack A checkout. This is what it looks like:

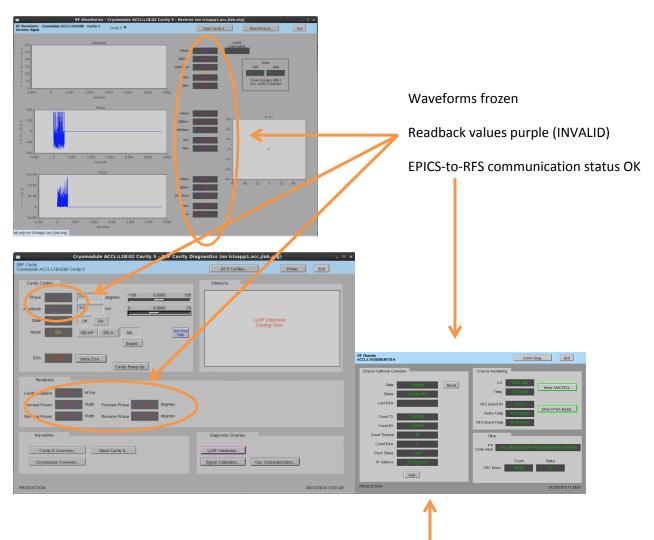
LLRF Rack Test Log File (on lclsapp1.acc.jlab.org)	×
[]	
192,168,0,102	
Write to /data/lcls-llrfcpu01/llrf/./live_prc_regmap.json	
192,168,0,102	
set_lins 0 0	
Signal min/max 0/0, amplitude 0.0 0.0, rms error 0.00 0K	
Signal min/max 0/0, amplitude 0.0 0.0, rms error 0.00 OK crc_errors clk_status_out dac_iq_phase shell_0_dsp_use_fiber_iq [60179, 2, 1, 1]	
cercements cincstatus_out dat_iq_prase sheri_o_dsp_use_riber_iq [ovi/3, 2, 1, 1]	
Signal min/max -2032/2367, amplitude 2032.7 9.9, rms error 63.88 BAD	
Signal min/max 2002/2007, amplitude 0.00, rms error 0.00 DK	
crc errors clk status out dae ig phase shell 0 dsp use fiber ig [60179, 2, 1, 1]	
set ins 0 79000	
Signal win/max -8130/8129, amplitude 8130.0 23.7, rms error 0.52 OK	
Signal min/max 0/0, amplitude 0.0 0.0, rms error 0.00 OK	
crc errors clk status out dac ig phase shell 0 dsp use fiber ig [60179, 2, 1, 1]	
set_lims 1 19750	
Signal min/max -2032/2032, amplitude 2032.1 5.9, rms error 0.49 OK	
Signal min/max 0/0, amplitude 0.0 0.0, rms error 0.00 OK	
crc_errors clk_status_out dac_iq_phase shell_1_dsp_use_fiber_iq [60179, 2, 1, 1]	
set_lims 1 79000	
Signal min/max -8130/8129, amplitude 8130.0 23.7, rms error 0.52 OK	
Signal min/max 0/0, amplitude 0.0 0.0, rms error 0.00 OK	
crc_errors clk_status_out dac_iq_phase shell_1_dsp_use_fiber_iq [60179, 2, 1, 1]	
set_lims 0 0	
Signal min/max 0/0, amplitude 0.0 0.0, rms error 0.00 DK	
Signal min/max 0/0, amplitude 0.0 0.0, rms error 0.00 OK	
crc_errors clk_status_out dac_iq_phase shell_0_dsp_use_fiber_iq [60179, 2, 1, 1] FAIL	

RF Rack Diagnostics - ACCL:L1B	0200 - Rack B (on Iclsapp1.acc.jlab.org) 💷 🛛 🗙
RF Hardware Cryomodule ACCL:L1B:0200 - Rack B	Exit
Run Rack Self-Test	
Go Complete Abo	t
Latest Self-Test Results	
Rack B	•
R.ck Ful Script aborted. Try again	
RFS1 Pass	
RFS2 Pass	
PRC Pass	
Res/Intik Pass	

It is an intermittent failure and is not understood. You'll have to simply re-run rack checkout and hope it passes. (We have observed that if the system was previously set up correctly and there has been no outage/hardware swap since, it will probably work fine in spite of this error.)

2. Recover Non-Updating EPICS Waveforms

Once in a while, I've seen the EPICS waveform data stop updating. Displays will look like this:



If you see this and nothing else seems to be wrong, try pressing 'Halt', then 'Reset' on the appropriate RFS screen. If that does not recover it, then there is a problem somewhere else.

3. Ping Test

To test if a chassis pings from a CPU:

- Log into LERF workstation or server (lcls01/2/3/ lclsapp1 with individual user id)
- b. Log into cpu (using CPU Node Name from Section 1):

iocConsole <cpuname>

OR

ssh laci@<cpuname>

(If prompted for login, type 'laci' and hit enter.)

c. Type: ping <ip>

4. View the EPICS IOC Console

- a. Log into LERF workstation or server (lcls01/2/3/lclsapp1 with individual user id)
- b. iocConsole <iocname>
- c. To exit viewer, press these 3 keys together: Ctrl, a, d.
- d. To scroll up in viewer, press these 3 keys together: Ctrl, a, [. Then use arrows to move up/down. To exit scroll mode, press these 3 keys together: Ctrl, a,].

(If you inadvertently kill the ioc, you can restart it using the instructions in section 2.)

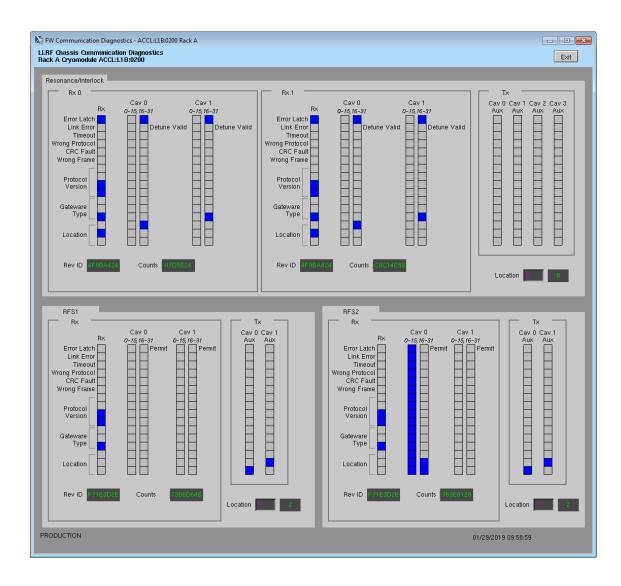
Schem	atic					
				RF Pr	ivate Network	
	Rack A			Rack I	3	
	ick Hardware it and Test	•		Rack Hardwa Init and Test.	re 	
Resonand (RES)	e/Interlock	Cavity 1 Cavity 2 Cavity 3 Cavity 4	30	Resonance/Interlock (RES)	Cavity 5 Cavity 6 Cavity 7 Cavity 8	
Power Su	pply			Power Supply		
26			26			
LO Distril	bution		23	LO Distribution		
RF Statio (RFS2)	n	Cavity 3 Cavity 4		RF Station (RFS2) O	Cavity 7 Cavity 8	
19			19			
RF Statio (RFS1)	n	Cavity 1		RF Station (RFS1) •	Cavity 5 Cavity 6	
15			15			
Precision Chassis (PRC)		Cavity 1 Cavity 2 Cavity 3 Cavity 4		Precision Receiver Crantis (PRC)	Cavity 5 Cavity 6 Cavity 7 Cavity 8	
		Cavity 4			Cavity o	

5. Troubleshoot RFS<->Res/Intlk Communication

a. Open Hardware screen. For the appropriate rack, click on an individual chassis

RF Chassis ACCL:L1B:0200:RFS1A				Cor m E	Diag Exit
Chassis Software Co	ntroller		Chassis Monitoring	-1-	
State	Running	Reset	LO	15 ő dBm	More AMC7823
Status	NO_ALARM		Temp	7.6 DegF	
Last Error			QF2 Board 6V	6.22 V	More FPGA Board
Count TX	3149250			43.12 DegC 30.56 DegC	
Count RX	3149182		GP2 Boan Temp	30.56 DegC	
Count Timeout	65		Other	_	_
Count Error	0		FW afecco	14035a2b099131	6935aa694409b1688e540
Clock Status	Valid		Code Hash		
IP Address	192.168.0.101		_	Count	Status
	Halt		CRC Errors	58685	Ok
PRODUCTION					01/28/2019 11:56:5

b. Click on 'Comm Diag...'



III. Expert Operations

These should be rarely/never needed. If you do need to perform any of these operations, please also just send a note to Sonya Hoobler (<u>sonya@slac.stanford.edu</u>) so it's on our radar.

1. Change IP Address of FPGA board (QF2pre)

Avoid two QF2pres with the same IP address on the LLRF internal network at the same time. So if you need to swap IPs between two boards, called X and Y below, you should:

- i. Following instructions from Section 6, halt communication between EPICS and relevant chassis
- ii. Disconnect X from the LLRF network
- iii. Update the IP address for Y (instructions below)
- iv. Disconnect Y from the LLRF network
- v. Reconnect X to the LLRF network
- vi. Update the IP address for X
- vii. Reconnect Y to the LLRF network

Instructions to change IP:

- a. Following instructions from Section 6, halt communication between EPICS and relevant chassis
- Log into LERF workstation or server (lcls01/2/3/ lclsapp1 with individual user id)
- c. Log into cpu (using CPU Node Name from Section 1):

iocConsole <cpuname>

OR

ssh laci@<cpuname>

(If prompted for login, type 'laci' and hit enter.)

d. Change directory:

cd /usr/local/lcls/package/qf2pre

- e. Execute these commands:
- 1. python -m qf2_python.scripts.update_spartan_6_configuration -X -t <old ip> -s IPV4_UNICAST_IP=<new ip>
- 2. python -m qf2_python.scripts.verify_spartan_6_configuration -X -t <old ip>
- 3. Repeat 1. removing "- X"
- 4. Repeat 2. removing "- X"
 - f. Power-cycle chassis
 - g. Execute command 2 but with *new* IP

- h. Execute command 4. but with *new* IP
- i. Ping chassis and verify response
- j. If board does NOT have AUTOBOOT_TO_RUNTIME set to 1 (and all LERF chassis should have that set), then execute:

python -m qf2_python.scripts.reboot_to_runtime -t <new ip> -v

k. Perform other checkout if desired/possible. For example, for a RFS or PRC, run prc.py or run rack checkout.

2. Verify QF2-pre Network Settings

From John Jones:

I suggest you disconnect all but one board in the system then work through each board in turn, running:

python -m qf2_python.scripts.verify_spartan_6_image -X -t [CURRENT_IP] for the bootloader settings and:

python -m qf2_python.scripts.verify_spartan_6_image -t [CURRENT_IP] for the runtime, and make sure that:

a) The bootloader and runtime images have the same settings for IP and MAC.b) That they are unique in the overall network.