LERF RF User Guide

Contents

I.	St	andard Controls and Information2
	1.	CPUs and IOCs2
	2.	Chassis IPs2
	3.	Start/Restart the EPICS IOC
	4.	View RF EDM screens
	5.	Initialize/Checkout LLRF Hardware
	6.	View RF Waveform Plots
	7.	Control Stepper Motor Tuner
	8.	Control Piezo Tuner
	9.	Drive Cavity With Simple Tone Signal
	10.	Run RF In SEL Pulsed Mode11
	11.	Ramp Cavity to CW/SELAP and Perform Cavity Characterization12
11.	0	ccasional Issues13
	1.	Mystery Rack Checkout Error
	2.	Recover Non-Updating EPICS Waveforms
	3.	Ping Test15
	4.	View the EPICS IOC Console
	5.	Troubleshoot RFS<->Res/Intlk Communication
Ш	. Ex	pert Operations
	1.	Change IP Address of FPGA board (QF2pre)
	2.	Verify QF2-pre Network Settings

I. Standard Controls and Information

1. CPUs and IOCs

JLab Cryomodule Number	LCLS-II Cryomodule Name	CPU Node Name*	EPICS IOC Name*
?	ACCL:L1B:0200	lcls-llrfcpu01	sioc-l1b-rf01
?	ACCL:L1B:0300	lcls-llrfcpu02	sioc-l1b-rf02

*CPU Node Name is referred to as <cpuname>in the commands shown below. EPICS IOC Name is referred to as <iocname> in the commands shown below.

2. Chassis IPs

These are the IP addresses used in the LLRF internal network. They are the same for each cryomodule.

Rack	Chassis	IP
Cavities 1-4 (aka Rack A)	RES	192.168.0.100
Cavities 1-4 (aka Rack A)	RFS1 (cavities 1,2)	192.168.0.101
Cavities 1-4 (aka Rack A)	RFS2 (cavities 3,4)	192.168.0.102
Cavities 1-4 (aka Rack A)	PRC	192.168.0.103
Cavities 5-8 (aka Rack B)	RES	192.168.0.200
Cavities 5-8 (aka Rack B)	RFS1 (cavities 5,6)	192.168.0.201
Cavities 5-8 (aka Rack B)	RFS2 (cavities 7,8)	192.168.0.202
Cavities 5-8 (aka Rack B)	PRC	192.168.0.203

PRC=Precision Receiver Chassis

Reads cavity probe signals

RFS=RF Station

Provides RF drive; reads forward , reverse, detune signals

RES=Resonance/Interlock Chassis

Controls tuners; performs interlock logic

3. Start/Restart the EPICS IOC

- Log into LERF workstation or server (lcls01/2/3/lclsapp1 with individual user id)
- 2. Type lerfhome&

LCLS2 Home	Screen: Electro	n Bean	n Systems (on Iclsa 🗕 🗆	×
LCLS-II LERF I	Home Screen		Home Screen Exit	
	Applications	Global	L1B	
	Magnet		-	
	RF			
	Cryo System		_	
	Network			
	Vacuum			
				_

3. Click on box intersecting Network and L1B

F Subsystems and Areas:	Network and IOCs	Home Screen
All Cro Magett B Cryo System Vacuum Vacuum	CH I SOM CH I SOM	
ODUCTION	zává 11. máin adl	08/20/2018 12:43

4. Click on IOC of interest



5. Click on 'Reboot'. Then click on 'Reboot Now!'

4. View RF EDM screens

- Log into LERF workstation or server (lcls01/2/3/lclsapp1 with individual user id)
- b. Type lerfhome&

🔳 LCLS2 Home Scr	een: Electroi	n Bean	n Systems (on Icisa _	□ × □
LCLS-II LERF Hon	ne Screen		Home Screen Exit	
	Applications	Global	L1B	
	Magnet			
	RF			
	Cryo System		—	
	Network			
	Vacuum			

c. Click on box intersecting RF and L1B

S-II Subsystem:	and Areas:	RF System		Help Home Screen
	Global GUNB LOB HT	L18 8C18 L28 8C28 L38 EXT DOG BYP	SLTH BSYH LTUH UNDH DMPH FEEH SLTS BSYS LTUS U	NDS DUMPE FEES NEH FEHT
All	Map and Status			
BPM/Toro/FC/BLen				
Feedback				
Magnet	Cevity	Cavity Cavity Cavity Cavity	Cavity Davity Cavity	
Profile Monitor	1.0	2.00 - S.00 - S.00	. <u></u>	1
Wire Scanner				
Collimator/Motion	Cryomodule 2 - A	CL:L1 B:0200		3
Laser				
RF				
Cryo System		Carda Carda	Carlos Carlos Carlos Carlos	N CAR
Event		1 2	3 4 5 6 7.	8
Network				
Vatr/Pwr/Gas/Smok		Cryomodule 3 - ACCL:L1B:0300		
Vacuum	Cryomodule Displays		Waveforms	
Temperature	Caulty Cantrol	Lieutuare Catibustian	Cryo-	Curementule
MPS	Cavity Compt.	Cantraine	module 2 Sargre Carrier.	Cryonoudre
PPS	SSAs	J	Cryo-	
BCS			module 3 Single Cavity	Cryonodule
ADS/X-Ray/Misc				
IOC:SYS0.AL00:M			r[_IIb_main.ed]	<sioc:sys2:al00:t0< td=""></sioc:sys2:al00:t0<>

L1B Overview Display



Single Cavity Display

5. Initialize/Checkout LLRF Hardware

Needed after power outage, hardware swap, etc.

- 📕 RF System Cryomodule Racks (on Iclsapp1.acc.jlab.org) 💷 🗆 🗙 RF Hardware Cryomodule ACCL:L1B:0300 Exit Schematic Rack A Rack B Rack Hardware Init and Test... Rack Hardware Init and Test... Resonance/Interlock... (RES) Resonance/Interlock. (RES) Cavity 1 Cavity 2 Cavity 5 Cavity 6 Cavity 7 wity 3 Cavity 8 C vity 4 wer Supply ower Supply RF Hardware Initialization and Test Cryomodule ACCL:L1B:0200 - Rack A • Exit Background process... O Distribution LO Distribution RFS and PRC Cavity 5 Cavity 6 Cavity 1 Cavity 2 RF Station... (RFS2) RF Station... (RFS2) 0 Run RFS/PR Go Complete Cavity 3 Cavity 4 Cavity 7 Cavity 8 Log... RF Station. (RFS1) RF Station... (RFS1) 0 0 Resonance/Interlock Cavity 5 Cavity 6 Cavity 7 Cavity 8 Cavity 1 Precision Rei Chassis... (PRC) Cavity 2 Cavity 3 Cavity 4 Chassie (PRC) 0 0 Initialize Chassis Go Complete Log... SW-FW Communication Halt SW Comm Reset SW Comm RF CPU
- a. Click on Hardware... (from either L1B Overview or Single Cavity display—see above).

- b. For appropriate rack (A or B), open display labelled Rack Hardware Init and Test...
- c. Execute RFS/PRC initialization and checkout. Click Go

(The script will disable and then re-enable communication with EPICS.)

To view the rack test script output, click on Log...

It will open an xterm window and display the script output as it progresses.

_	LLRF Rack Test Lo	n icisapp1.acc.jlab.org) _
	Will load new bitfiles to FPGAs	
Computer	Will execute Icls2_rack.sh from /usr/local/Icls/package_cls2_llr Will source /usr/local/Icls/epics/inc/amen/facilitu/Sof them in	f/software/prc wRT.sh
	Will write files to /data/lcls-llrfcpu01/llrf Path to UF2PRE files is /usr/lscal/lcls/package/gf2pre	
	Vill write status to ACCL:L18:0200:RACKA:SELFTEST_MSG Beginning checkout for rack A	
RF Rack Diagnostics	System 05 is linuxRT. Setting python LD_LIBRARY_PATH before proce /usr/local/lcls/package/lcls2_llrf/software/prc	eeding.
Cryomodule ACCL:L1B:0200 - Rac	A Board ID packet format: 0 There are 1 devices in the chain:	
Run Rack Self-Test	0x364c093 - Xilinx Kintex 7 160T	
	Loading bitfile: /usr/local/lcls/package/lcls2_llrf/software/prc/	/,,/,./firmware/prc/prc-qF2-20180406b.bit
Go	Design name: profiber ID=00FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF	
	Build time: 08:2704/06 Build time: 08:2704	
	Defaultion device relection in chain from LICODE	
Latest Self-Test Results	Device selected for programming is in chain location; 0 Kiliny Kintex 7 interface selected	
	Programming	
-	992 Board ID packet forwat: 0	
Rack Running Edward	10 5 6 6 5 6 10 10 10 10 10 10 10 10 10 10 10 10 10	Log
RFS1 Rest		
HP-52		Contraction of the local distance of the loc
PRC BASS		
Res/Indik Rass		
		LLRF Rack Test Log File (on Iclsapp1.acc.jlab.org)

RF Hardware Initialization and Test Cryomodule ACCL:L1B:0200 - Rack A •	Background process
RFS and PRC	
Run RFS//PRC Rack Init and Test Go Complete	
Pass Rack checkout complete	2019-01-24-15:18:14 Log
Resonance/Interlock	
Initialize Chassis Go Complete	<u>g.</u>
SW-FW Communication	
Halt SW Comm Reset SW Comm	
PRODUCTION	01/24/2019 16:18:48

d. Initialize RES chassis. Click Go

(The script will disable and then re-enable communication with EPICS.)

SRF Cavity - ACCL:L1B:0210	
SRF Cavity Cryomodule ACCL:L1B:0200 Cavity 1	All 8 Cavities Exit
Cavity Control Phase 0.0 degrees -180 0.0000 180 Amplitude 0.0 6.0 MV 0 6.0000 20 RF State 0 0.0 0 0.0 20 RF Mode SEL SEL Expert. SSA 1000 More SSA Cavity Ramp-Up	Interlocks Cument Latched Stopper Temperature 1 Coupler Temperature 1 Coupler Temperature 2 Coupler Vacuum Beamine Vacuum CHL Ready He Level Summary Cryomodule View. Cavity View.
Readback	Detune TGEN
Cavity Gradient 0000 MV/m Forward Power 0000 Walls Forward Phase 0000 degrees Reverse Power 00000 Walls Reverse Phase 0000000 degrees	Hz Turn Off
We work Expert/Diagnostic Displays Cavity 1 Overview More Cavity Problem. Cryomodule Overview Forward Reverse Forward Reverse Prive (Loop)	Stepper Tuner Cav Characterization Tone Test Piezo Tuner SEL Phase & Pulse Feedback Parms

6. View RF Waveform Plots

Cavity Overview -- Cavity, Forward, Reverse signals for single cavity

Cryomodule Overview -- Cavity, Forward, Reverse signals for all 8 cavities

More Cavity -- Drop-down menu for single-cavity single-signal screen

From those screens, you can navigate to other cavities, other signals, or display a single signal for all 8 cavities. Example screenshots:









7. Control Stepper Motor Tuner

a. Click on Stepper Tuner...



b. 8-cavity screen. From here you can enter number of steps and then click the green arrow to go in one direction or the other. (Relationship between direction and frequency is not yet known.) Click More... for single tuner screen

8. Control Piezo Tuner

SRF Cavity Cryomodule ACCL:L1B:0200 Cavity 1	All 8 Cavities Exit
Cavity Control Phase 182.2 0.0 degrees -180 0.0000 Ampitude 000 6.0 MV 0 6.0000 RF State Off Off Off RF Mode SEL SSA SSA More SSA. Cavity Ramp-Up	Interlocks Current Latched Stepper Temperature Coupler Temperature Coupler Vacuum Beamline Vacuum CHL Ready Future He Everi Summary Cryconodule View Cavity View
Readback Cavity Gradient Cavity Gradient Forward Power Forward Power Reverse Power Watts Reverse Power Reverse Power Gradient Reverse Power Reverse Power	Detune TGEN
Waveforms Expert/Diagnostic Displa Cavity 1 Overview More Cavity 1 Cryomodule Overview Signal Calibration	ys Stenner Tuner Cav Characterization Tone Test. Plezo Tuner SEL Phase & Pulse Feedback Parms
PRODUCTION	01/29/2019 09:49:17

a. Click on Piezo Tuner...

SRF Piezo Tuners - ACCL:L1B:0300 (on lclsapp1.acc.jlab.org) _ 🗆 🗙									
SRF Piezo Tu Cryomodule /	SRF Piezo Tuner Cryomodule ACCL:L1B:0300								
Piezo	Piezo Control								
	Enable	e resets DAC se	etpoint to 0		DAC Setpoint				
1	Enable	Disable	Not enabled	(0.0	V 0.0	More			
2	Enable	Disable	Not enabled	0.0	V 0.0	More			
3	Enable	Disable	Notenabled	0.0	V 0.0	More			
4	Enable	Disable	Not enailed	0.0	V 0.0	More			
5	Enable	Disable	Not enabled	0.0	V 0.0	More			
6	Enable	Disable	Not enabled	0.0	V 0.0	More			
7	Enable	Disable	Not enabled	0	V 0.0	More			
8	Enable	Disable	Not enabled	0.0	V 0.0	More			

b. 8-cavity screen. From here you can enable the piezo tuner and enter a DC DAC voltage. Click More... for single piezo tuner screen

		-	0
SRF Cavity Cryomodule ACCL:L1B:0200 Cavity 1			All 8 Cavities Exit
Cavity Control Phase Cavity Control	ogrees -180 0.0000 V 0 6.0000	180 Interlocks 20 Stepper Temperature 20 Coupler Temperature 2 Coupler Temperature 2 Coupler Vacuum Beanine Vacuum CHL Ready He Level Foture He Presure	urrent Latched Unlatch All Undethes 4 eavities
SSA More SSA	Expert	Summary	Cryomodule View Cavity View
Cavity Gradient 1005 MV/m Forward Power Watts For Reverse Power Watts Rev	ward Phase degrees erse Phase tites degrees	Hz more coming soon	Tum Off
Waveforms Cavity 1 Overview More Cryomodule Overview PRODUCTION	Expert/Diagnos Cavity 1 Signal Calibra	iic Displays ureStepper Tuner	Cav Characterization Tone Test SEL Phene & Pulse Feedback Parms 01/29/2019 0949:17

9. Drive Cavity With Simple Tone Signal

a. Click on Tone Test...

SRF To	ne Test - ACCL:L1B:030	00 (on Iclsapp1.acc.jlab.org	I) _ 🗆 ×
Simple Tone Test Cryomodule ACCL:L1B:030	0		Exit
Tone Test			
Cavity	Within e only one c	each cavity pair, an be one at a time	
	1	DAC Counts (0-32767)	
1 <u>On</u>	Off Off	0 0	Expert
2 <u>On</u>			
3 On			
4 On	Off Off	0 0	Expert
5 On	Off Eirst Chan	30000 30000	Expert
6 On		-	Laperta
7 <u>On</u>	Off Off	0 0	Expert
8 <u>On</u>			

- b. Turn desired cavity 'On', then enter number of DAC counts...
- c. When done, click 'Off'

10. Run RF	In SEL Pulsed Mode	
SRF Cavity Cryomodule ACCL:L1B:0200 Cavity 1	All 8 Cavities Exit	
Cavity Control Phase 100 Amplitude 0 1 B 0 MV 0 FF State 0 0 0 0 MV 0 FF Mode SEL SELAP SELA SEL Expert SSA 1 1 More SSA	0.0000 180 0.0000 20 0.0000 20 Coupler Temperature 1 0 0.0000 20 Coupler Temperature 2 0 Cutter View 0 Future He Pressure 2 0 Cavity Ramp-Up 0 Cavity View 0	
Readback Cavity Gradient Could Gradient Forward Power Reverse Power Could Gradient Reverse Power Reve	Detune TGEN Detune TGEN I to to degrees more coming soon	
Waveforms Cavity 1 Overview	Expert/Diagnostic Displays LLRF Hardware Stepper Tuner Cav Characterization Tone Test Signal Calibration Piezo Tuner SEL Phase & Pulse Feedback Parms	
PRODUCTION	01/29/2019 09:49:17	

a. Click on SEL Phase & Pulse...

The settings/options for pulsed mode are more complicated than you'd think. It's a good idea to read the README at the bottom of the screen.



- b. Enter desired amplitude (settings will be 'yellow' if they do not match Current/Last In Use)
- c. Enter desired RF pulse length
- d. Click Go
- e. When done, click Stop
- f. To update amplitude or time settings, enter new values and then click Go again

11. Ramp Cavity to CW/SELAP and Perform Cavity Characterization

This is used to bring up a cavity 'from scratch' or if there is some need to re-characterize the cavity/SSA. You do not need to run this every time you turn a cavity on.



a. Click on Cavity Ramp-Up...



- b. Set Amplitude Goal and click Go
- c. Future (not yet done 1/29/2019): the script will write is calculated characterization parameters to the Newly Calculated values on the screen. You can review these and if they seem reasonable, click Push New Vals. You can also save the Current values as a known good set—to possibly restore in future.

II. Occasional Issues

1. Mystery Rack Checkout Error

We occasionally see a problem during the first cryomodule rack A checkout. This is what it looks like:

LLRF Rack Test Log File (on lclsapp1.acc.jlab.org)	_	×
192,168,0,102		
Write to /data/lcls-llrfcpu01/llrf/./live_prc_regmap.json		
132.168.0.102		
set_lims 0 0		
Signal min/max 0/0, amplitude 0.0 0.0, rms error 0.00 DK		
Signal min/max 0/0, amplitude 0.0 0.0, rms error 0.00 DK		
crc_errors clk_status_out dac_iq_phase shell_0_dsp_use_fiber_iq [60179, 2, 1, 1]		
set_lims 0 19/50		
Signal min/max -2032/2367, amplitude 2032.7 9.9, rms error 53.88 BAD		
Signal min/max 0/0, amplitude 0.0 0.0, rms error 0.00 UK		
crc_errors clk_status_out dac_iq_phase shell_0_dsp_use_fiber_iq [601/9, 2, 1, 1]		
Signal Min/Max -8130/8129, amplitude 8130.0 23.7, PMS error 0.52 UK		
Signal min/max 0/0, amplitude 0.0 0.0, rms error 0.00 0K		
Crc_errors cik_status_out dac_iq_phase shell_v_dsp_use_fiber_iq [601/3, 2, 1, 1]		
Set_1105 1 13700 Sional min/may -2022/2022 -amplitude 2022 1 5 9, pms appen 0 49, 0V		
Signal with wat 2002/2002, amplitude 2002,10,3, mis error 0,40 on		
Signal Minumax ovo, amplitude 0,0 0,0, mis error 0,00 km		
at line 1 7900		
Storal min/may -8130/8129 amplitude 8130 0 23 7 rms error 0 52 0K		
Signal min/max 0100 0123, amplitude 010, 0 23, 7 ms error 0,00 0K		
and white what we shall all a choice of the state of the		
et line ()		
Signal min/max 0/0, amplitude 0.0 0.0, rms error 0.00 RK		
Signal min/max 0/0, amplitude 0.0.0.0, rms error 0.00 DK		
orc errors clk status out dac ig phase shell 0 dsp use fiber ig [60179, 2, 1, 1]		
FAIL		
1-		P-00000

RF Rack Diagnostics - AC	CL:L1B:0200 - Rack B (on ici	sapp1.acc.jlab.org) _ 🗆 🔅
RF Hardware Cryomodule ACCL:L1B:0200 - Rack B		Exit
Run Rack Self-Test		
Go Complete	Abort	
Latest Self-Test Results		
	Rack B	
RCK Fai Script aborted	i. Try again.	2018-06-11-17:09:48 Log
RFS1 Pass		
RFS2 Pass		
PRC Pass		
Res/Intik Pass		

It is an intermittent failure and is not understood. You'll have to simply re-run rack checkout and hope it passes. (We have observed that if the system was previously set up correctly and there has been no outage/hardware swap since, it will probably work fine in spite of this error.)

2. Recover Non-Updating EPICS Waveforms

Once in a while, I've seen the EPICS waveform data stop updating. Displays will look like this:



If you see this and nothing else seems to be wrong, try pressing 'Halt', then 'Reset' on the appropriate RFS screen. If that does not recover it, then there is a problem somewhere else.

3. Ping Test

To test if a chassis pings from a CPU:

- Log into LERF workstation or server (lcls01/2/3/ lclsapp1 with individual user id)
- b. Log into cpu (using CPU Node Name from Section 1):

iocConsole <cpuname>

OR

ssh laci@<cpuname>

(If prompted for login, type 'laci' and hit enter.)

c. Type: ping <ip>

4. View the EPICS IOC Console

- a. Log into LERF workstation or server (lcls01/2/3/lclsapp1 with individual user id)
- b. iocConsole <iocname>
- c. To exit viewer, press these 3 keys together: Ctrl, a, d.
- d. To scroll up in viewer, press these 3 keys together: Ctrl, a, [. Then use arrows to move up/down. To exit scroll mode, press these 3 keys together: Ctrl, a,].

(If you inadvertently kill the ioc, you can restart it using the instructions in section 2.)

Schem	atic					
				RF Pr	ivate Network	
	Rack A			Rack I	3	
Ra	ick Hardware it and Test	•		Rack Hardwa Init and Test.	re 	
Resonand (RES)	e/Interlock	Cavity 1 Cavity 2 Cavity 3 Cavity 4	30	Resonance/Interlock (RES)	Cavity 5 Cavity 6 Cavity 7 Cavity 8	
Power Su	pply			Power Supply		
26			26			
LO Distri	bution		29	LO Distribution		
RF Statio (RFS2)	n	Cavity 3 Cavity 4		RF Station (RFS2) O	Cavity 7 Cavity 8	
19			19			
RF Statio (RFS1)	n	Cavity 1		RF Station (RFS1) •	Cavity 5 Cavity 6	
15			15			
Precision Chassis (PRC)	Receiver	Cavity 1 Cavity 2 Cavity 3 Cavity 4		Precision Receiver Crantis (PRC)	Cavity 5 Cavity 6 Cavity 7 Cavity 8	
		Cavity 4			Cavity o	

5. Troubleshoot RFS<->Res/Intlk Communication

a. Open Hardware screen. For the appropriate rack, click on an individual chassis

RF Chassis ACCL:L1B:0200:RFS1A				Cor m E	Diag Exit
Chassis Software Co	ntroller		Chassis Monitoring	-1-	
State	Running	Reset	LO	15 ő dBm	More AMC7823
Status	NO_ALARM		Temp	7.6 DegF	
Last Error			QF2 Board 6V	6.22 V	More FPGA Board
Count TX	3149250		Kintex Temp	43.12 DegC	
Count RX	3149182		GP2 Boan Temp	30.56 DegC	
Count Timeout	65		Other	_	_
Count Error	0		FW afecco	14035a2b099131	6935aa694409b1688e540
Clock Status	Valid		Code Hash		
IP Address	192.168.0.101		_	Count	Status
	Halt		CRC Errors	58685	Ok
PRODUCTION					01/28/2019 11:56:5

b. Click on 'Comm Diag...'



III. Expert Operations

These should be rarely/never needed. If you do need to perform any of these operations, please also just send a note to Sonya Hoobler (<u>sonya@slac.stanford.edu</u>) so it's on our radar.

1. Change IP Address of FPGA board (QF2pre)

Avoid two QF2pres with the same IP address on the LLRF internal network at the same time. So if you need to swap IPs between two boards, called X and Y below, you should:

- i. Following instructions from Section 6, halt communication between EPICS and relevant chassis
- ii. Disconnect X from the LLRF network
- iii. Update the IP address for Y (instructions below)
- iv. Disconnect Y from the LLRF network
- v. Reconnect X to the LLRF network
- vi. Update the IP address for X
- vii. Reconnect Y to the LLRF network

Instructions to change IP:

- a. Following instructions from Section 6, halt communication between EPICS and relevant chassis
- Log into LERF workstation or server (lcls01/2/3/ lclsapp1 with individual user id)
- c. Log into cpu (using CPU Node Name from Section 1):

iocConsole <cpuname>

OR

ssh laci@<cpuname>

(If prompted for login, type 'laci' and hit enter.)

d. Change directory:

cd /usr/local/lcls/package/qf2pre

- e. Execute these commands:
- 1. python -m qf2_python.scripts.update_spartan_6_configuration -X -t <old ip> -s IPV4_UNICAST_IP=<new ip>
- 2. python -m qf2_python.scripts.verify_spartan_6_configuration -X -t <old ip>
- 3. Repeat 1. removing "- X"
- 4. Repeat 2. removing "- X"
 - f. Power-cycle chassis
 - g. Execute command 2 but with *new* IP

- h. Execute command 4. but with *new* IP
- i. Ping chassis and verify response
- j. If board does NOT have AUTOBOOT_TO_RUNTIME set to 1 (and all LERF chassis should have that set), then execute:

python -m qf2_python.scripts.reboot_to_runtime -t <new ip> -v

k. Perform other checkout if desired/possible. For example, for a RFS or PRC, run prc.py or run rack checkout.

2. Verify QF2-pre Network Settings

From John Jones:

I suggest you disconnect all but one board in the system then work through each board in turn, running:

python -m qf2_python.scripts.verify_spartan_6_image -X -t [CURRENT_IP] for the bootloader settings and:

python -m qf2_python.scripts.verify_spartan_6_image -t [CURRENT_IP] for the runtime, and make sure that:

a) The bootloader and runtime images have the same settings for IP and MAC.b) That they are unique in the overall network.