LERF RF User Guide

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I. Standard Controls and Information

1. CPUs and IOCs

JLab Cryomodule Number	LCLS-II Cryomodule Name	CPU Node Name*	EPICS IOC Name*
1	ACCL:L1B:0200	lcls-llrfcpu01	sioc-l1b-rf01
2	ACCL:L1B:0300	lcls-llrfcpu02	sioc-l1b-rf02

*CPU Node Name is referred to as <cpuname>in the commands shown below. EPICS IOC Name is referred to as <iocname> in the commands shown below.

2. Chassis IPs

These are the IP addresses used in the LLRF internal network. They are the same for each cryomodule.

Rack	Chassis	IP
Cavities 1-4 (aka Rack A)	RES	192.168.0.100
Cavities 1-4 (aka Rack A)	RFS1 (cavities 1,2)	192.168.0.101
Cavities 1-4 (aka Rack A)	RFS2 (cavities 3,4)	192.168.0.102
Cavities 1-4 (aka Rack A)	PRC	192.168.0.103
Cavities 5-8 (aka Rack B)	RES	192.168.0.200
Cavities 5-8 (aka Rack B)	RFS1 (cavities 5,6)	192.168.0.201
Cavities 5-8 (aka Rack B)	RFS2 (cavities 7,8)	192.168.0.202
Cavities 5-8 (aka Rack B)	PRC	192.168.0.203

PRC=Precision Receiver Chassis

Reads cavity probe signals

RFS=RF Station

Provides RF drive; reads forward , reverse, detune signals

RES=Resonance/Interlock Chassis

Controls tuners; performs interlock logic

3. Start/Restart the EPICS IOC

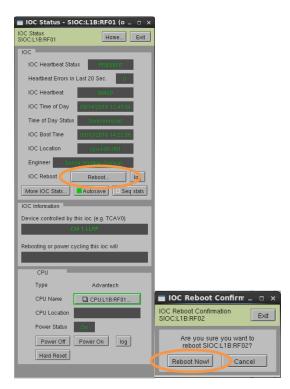
- Log into LERF workstation or server (lcls01/2/3/lclsapp1 with individual user id)
- 2. Type lerfhome&

🔳 LCLS2 Home Screen: Electron Be	eam Systems (on Iclsa 💷 🗆 🗙
LCLS-II LERF Home Screen	Home Screen Exit
Applications	bal L1B
Magnet	
RF	
Cryo System	
Network	
Vacuum	

3. Click on box intersecting Network and L1B

	LCLS Subsystems and Areas: ntwk I1b (on IcIsapp1.acc.jlab.org)	- 0
RF Subsystems and Are	as: Network and IOCs	Home Screen
Global	18	
All Cryst Magnet SIG	C 0601 (R01]	
Cryo System Magn Network sc	H ICL18M007	
• sic	CLIBRAGI CLIBRAGI CLIBSANI CLIBSANI CLIBSANI	
Vacuu Site	a VCL18 VA81	
RODUCTION	ntex, JTD, main ed	08/20/2018 17:43.3

4. Click on IOC of interest



5. Click on 'Reboot'. Then click on 'Reboot Now!'

4. View RF EDM screens

- a. Log into LERF workstation or server (lcls01/2/3/lclsapp1 with individual user id)
- b. Type lerfhome&

🔳 LCLS2 Home Screen: Electro	on Beam	Systems (on Iclsa	_ = ×
LCLS-II LERF Home Screen		Home Screen Exit	
Applications	Global	L1B	
Magnet			
RF	i 🗖		
Cryo System	į 🗖		
Network		-	
Vacuum			

c. Click on box intersecting RF and L1B

S-II Subsystem	s and Areas:	RF System		Help Home Screen
	Global GUNB LOB HTR	L18 BC18 L28 BC28 L38 EXT DOG BYP SL1	TH BSYM LTUM UNDH OMPH FEEH SLTS BSYS LTUS	UNDS DUMPE FEES NEH FEHT
All	Map and Status			
BPM/Toro/FC/BLen				
Feedback				
Magnet	Cavity	Cavity Cavity Cavity Cavity Cavity S	Davity Davity Cavity 6 7 8	
Profile Monitor	1	And And And	• • • • • • • • • • • • • • • • • • •	
Wire Scanner				
Collimator/Motion	Cryomodule 2 - ACC	L:L1B:0200		
Laser				
RF				
Cryo System		Cavity Cavity	Cavity Cavity Cavity C	avity Cavity
Event		1 2	Cavity Ca	avity Cavity 7 8
Network				
Vatr/Pwr/Gas/Smok		Cryomodule 3 - ACCL:L1B:0300		
Vacuum	Cryomodule Displays		Waveforms	
Temperature	Cavity Control	Hardware Calibration	Cryo- module 2 Single Cavity.	Cryomodule
MPS		Cantraine	module 2 Single Cavity.	Cryonoudre
PPS	SSAs		Cryo- Single Cavity	Cryomodule
BCS			module 3 Single Cavity.	Cryonodure
ADS/X-Ray/Misc				
IOC:SYS0.AL00.M			rf_11b_main.edl	<sidc:sys2:al00:to< td=""></sidc:sys2:al00:to<>

L1B Overview Display



Single Cavity Display

5. Initialize/Checkout LLRF Hardware

Needed after power outage, hardware swap, etc.

RF System - Cryomodule Racks	(on lclsapp1.acc.jlab.org) _ 🗆 🗙		
RF Hardware Cryomodule ACCL:L1B:0300	Exit		
Schematic			
	RF Private Network		
Rack A	Rack B		
Rack Hardware Init and Test	Rack Hardware Init and Test		
Rack A Rack Hardware Init and Test Resonance/Interlock	Resonance/Interlock Cavity 5 (RES) • Cavity 6		
Cavity 3 30 Cavity 4	Cavity 7 30 Cavity 8		
Power Supply	Power Supply		
26	26	RF Hardware Initialization and Test	
LO Distribution	LO Distribution	Cryomodule ACCL:L1B:0200 - Rack A •	Background process Exit
23 BE Station	23 BE Station	RFS and PRC	
RF Station (RFS2) Cavity 1 Cavity 2	RF Station Cavity 5 (RFS2) Cavity 6	Run RFS/PR Rack Init and Te	
19	19		
RF Station Cavity 3 (RFS1) Cavity 4	RF Station Cavity 7 (RFS1) Cavity 8	Pass Rack checkout complete	2019-01-24-15:16 Log
15	15	Resonance/Interlock	
Precision Receiver Chassis (PRC) • Cavity 1 Cavity 2 Cavity 3 11 Cavity 4	Precision Receiver Chassis (PRC) 11 Cavity 6 Cavity 7 Cavity 8	Initialize Chassis Go Complete Log	J
		SW-FW Communication	
RF CPU		Hait SW Comm Reset SW Comm	
		PRODUCTION	01/24/2019 16:18:48

a. Click on Hardware... (from either L1B Overview or Single Cavity display—see above).

- b. For appropriate rack (A or B), open display labelled Rack Hardware Init and Test...
- c. Execute RFS/PRC initialization and checkout. Click Go

(The script will disable and then re-enable communication with EPICS.)

To view the rack test script output, click on Log...

١

It will open an xterm window and display the script output as it progresses.

_	LLRF Rack Test Lo	e (on icisapp1.acc.jlab.org) _
	Will load new bitfiles to FPGAs	
Computer	Will execute lcls2_rack_sh from /usr/local/lcls/package cls Will source /usr/local/lcls/epics/iocCommon/facilitu/Got tho	2_11rf/software/prc ni reu®T sh
	Will write files to /data/lcls-llrfcpu01/llrf Path to DE2PRE files is /ur/lccal/lcls/package/gf2pre	
	Vill write status to ACCL:L1B:0200:RACKA:SELFTEST_MSG	
RF Rack Diagnostics RF Hardware	/usr/local/lcls/package/lcls2_llrf/software/prc	proceeding.
Cryomodule ACCL:L1B:0200 - Rac	A Board ID packet format: 0 There are 1 devices in the chain:	
Run Rack Self-Test	0x364c093 - Xilinx Kintex 7 1607	
	Loading bitfile: /usr/local/lcls/package/lcls2_llrf/software Design name: pro:UserID=00FFFFFFF;Version=2017.1	/prc/,,/,./firmware/prc/prc-qf2-20180406b.bit
Go	Design name: pr://derill=00/FFFFFF/Version=2017.1 Device name: 7k160tfg676 Build date: 2018/04/06	
	Build the: 08:59:04 Length: 68:2572 bits	
	Defaulting device selection in chain from [ICODE	
Latest Self-Test Results	Device selected for programming is in chain location; 0 Xilinx Kintex 7 interface selected	
	Programming	
	992 Board ID packet format: 0	
Rack Running Bateriet	19 Chestold for rack A	Log
RFS1 Patt		
RFS2		Contract of the second
PRC PAIL		And Street of St
Res/Intik		
		LLRF Rack Test Log File (on Iclsapp1.acc.jlab.org)

RF Hardware Initialization and Test Cryomodule ACCL:L1B:0200 - Rack A O	Background process
RFS and PRC	
Run RFS/PRC Rack Init and Test Go Complete	
Pass Rack checkout complete	2019-01-24-15:16:14 Log
Resonance/Interlock	
Initialize Go Complete	Log
SW-FW Communication	
Halt SW Comm Reset SW Comm	
PRODUCTION	01/24/2019 16:18:48

d. Initialize RES chassis. Click Go

(The script will disable and then re-enable communication with EPICS.)

SRF Cavity - ACCL:L1B:0210	
SRF Cavity Cryomodule ACCL:L1B:0200 Cavity 1	All 8 Cavities Exit
Cavity Control Phase	Interlocks Current Latched Stopper Temperature 1 Coupler Temperature 2 Coupler Temperat
SSA Cavity Ramp-Up	Cryomodule View Cavity View Detune TGEN
Cavity Gradient B 0005 MV/m Fonward Power B 0007 Watts Forward Phase B 0007 degrees Reverse Power B 0007 Watts Reverse Phase B 0007 degrees	Hz Turn Off
We countrie Expert/Diagnostic Display Cavity 1 Overview More Cavity In Cavity Probe Cryomodule Overview Forward Reverse Probe Prover (coop) Proverse	Stepper Tuner Cav Characterization Tone Test Piezo Tuner SEL Phase & Pulse Feedback Parms
PRODUCTION	01/29/2019 09:51:15

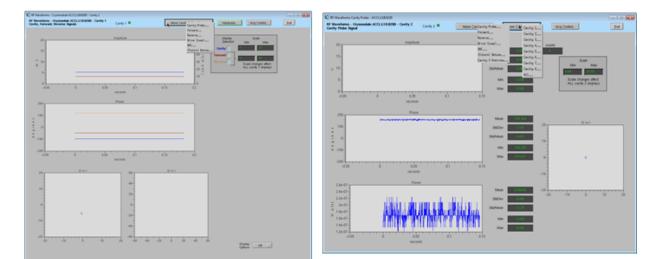
6. View RF Waveform Plots

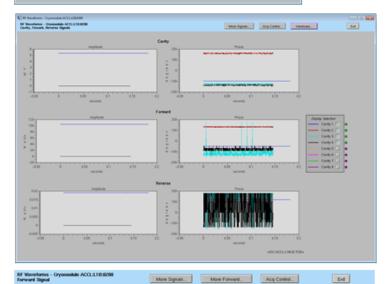
Cavity Overview -- Cavity, Forward, Reverse signals for single cavity

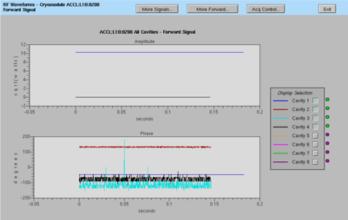
Cryomodule Overview -- Cavity, Forward, Reverse signals for all 8 cavities

More Cavity -- Drop-down menu for single-cavity single-signal screen

From those screens, you can navigate to other cavities, other signals, or display a single signal for all 8 cavities. Example screenshots:

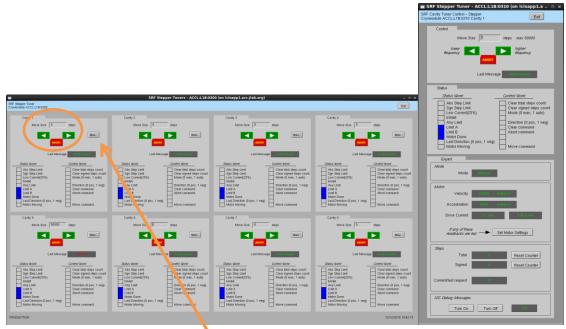






7. Control Stepper Motor Tuner SRF Cavity Cryomodule ACCL:L1B:0200 Cavity 1 All 8 Cavities... Exit Cavity Control Interlock 0.0 Phase Stepper Temperature ature 1 6.0 мv ature 2 Coupler Vacuum RF State Off On Unlatch All Unlatches 4 cavities CHI Re RF Mode SELAP SELA SEL ? Expert... SSA More SSA... Cavity Ramp-Up... Cryomodule View... Cavity View... Readback Detune TGEN MV/m Cavity Gradient Tum Off Forward Powe Watts degrees ? Reve Watts degree Waveform Expert/Diagnostic Display Cavity 1 Overview... More Cavity 1... LLRF Hardware.... Stepper Tuner... Cav Characterization... Tone Test... Signal Calibration.... Piezo Tuner... SEL Phase & Pulse... Feedback Parms... Cryomodule Overview... 19 09:49:17

a. Click on Stepper Tuner...



b. 8-cavity screen. From here you can enter number of steps and then click the green arrow to go in one direction or the other. (Relationship between direction and frequency is not yet known.) Click More... for single tuner screen

8. Control Piezo Tuner

SRF Cavity Cryomodule ACCL:L1B:0200 Cavity 1	All 8 Cavities Exit
Cavity Control Phase 1972 0.0 degrees -180 0.0000 180 Amplitude 199 6.0 MV 0 6.0000 20 RF State 109 Of On RF Mode SEL SELAP SELA SEL Expert. SSA More SSA. Cavity Ramp-Up	Interlocks Current Latched Stepper Temperature Coupler Temperature Coupler Temperature Coupler Vacuum Beamline Vacuum He Level Summary Cryoendule View Cavity View
Readback. Cavity Gradient 0003 MV/m Forward Power 00000 Watts Forward Phase 0000 degrees Reverse Power 00000 Watts Reverse Phase 00000 degrees	Detune TGEN TGEN TGEN Turn Off more coming scon
Waveforms Expert/Diagnostic Display Cavity 1 Overview Cryomodule Overview Signal Calibration	ys Stenner Tumer Cav Characterization Tone Test Piezo Tuner SEL Phase & Pulse Feedback Parms
PRODUCTION	01/29/2019 09:49:17

a. Click on Piezo Tuner...

				1.acc.jlab.org)	
Cryomodule ACCI					Exit
Piezo Con	ntrol Enable resets DAC	cetaoiat to D		DAC Setpoint	
	Linable resers DHO	supern to o		DHC Selpoint	
1 E	nable Disable	Not enabled	0.0	V 0.0 V	More
2 E	nable Disable	Not enabled	0.0	V 0.0 V	More
3 E	nable Disable	Not enabled	0.0	V 0.0 V	More
4 E	nable Disable	Not enabled	0.0	V 0.0 V	More
5 E	nable Disable	Not enabled	0.0	V 0.0 V	More
6 E	nable Disable	Not enabled	0.0	V 0.0 V	More
7 E	nable Disable	Not enabled	0.0	V 0.0 V	More
8 E	nable Disable	Not enabled	0.0	V 0.0 V	More

b. 8-cavity screen. From here you can enable the piezo tuner and enter a DC DAC voltage. Click More... for single piezo tuner screen

SRF Cavity Cryomodule ACCL:L1B:0200 Cavity 1	All 8 Cavities Exit
Cavity Control Phase 107.2 0.0 degrees -180 0.0000 180 Amplitude 000 6.0 MV 0 6.0000 20 RF State 001 0 0 0 0 20 RF Mode SEL SELAP SELA SEL P SSA More SSA. Cavity Ramp-Up	Interlocks Current Latched Stepper Temperature Coupler Temperature Coupler Temperature Coupler Vacuum Beanline Vacuum CHL Ready Future He Level Summary Cruce Ressure Current Vacuum Cur
Readback Cavity Gradient 0.0003 MV/m Forward Power 0.000 Walts Forward Phase 0.000 degrees Reverse Power 0.000 Walts Reverse Phase 0.0000 degrees	Detune TGEN TGEN TGEN Tgen Tum Off Tum Off To the second s
Waveforms Cavity 1 Overview Cryomodule Overview PRODUCTION Expert/Diagnostic Display Expert/Display Expert/Diagnostic Display Expert/Display Expert/Display	/s Stepper Tuner Cav Characterization Tone Test Piezo Tuner SEL Phase & Pulse Feedback Parms 01/29/2019 03:43:17

9. Drive Cavity With Simple Tone Signal

a. Click on Tone Test...

SRF To	ne Test - ACCL:L1B:030	0 (on lclsapp1.acc.jlab.org	j) _ = ×
Simple Tone Test Cryomodule ACCL:L1B:030	00		Exit
Tone Test			
Cavity	Within e only one ca	ach cavity pair, n be one at a time	
1 <u>On</u>	Off Off	DAC Counts (0-32767)	Expert
2 <u>On</u>]		
3 <u>On</u> 4 <u>On</u>	Off Off	0.	Expert
5 <u>On</u> 6 On	Off First Chan	30000 30000	Expert
7 On 8 On		00	Expert

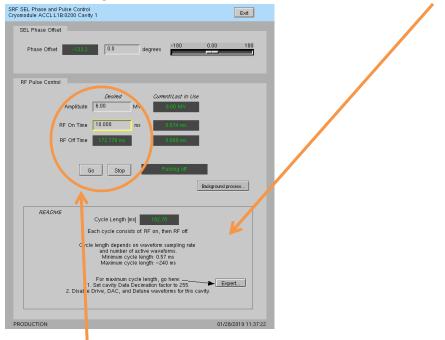
- b. Turn desired cavity 'On', then enter number of DAC counts...
- c. When done, click 'Off'

SRF Cavity Cryomodule ACCL:L1B:0200 Cavity 1	All 8 Cavities Exit
Cavity Control Phase 0.0 degrees -180 0.0000 180 Amplitude 0.0 6.0 MV 0 6.0000 20	Interlocks Current Latched Stepper Temperature Coupler Temperature Coupler Temperature 2
RF State Off On RF Mode SEL SELAP SELA SEL ? Expert.	Coupler Vacuum Unlatch All Unlatch All Unlatch All Unlatch All Unlatch All He Level Acavites
SSA More SSA Cavity Remp-Up	Summary Cryomodule View Cavity View
Readback	Detune TGEN
Cavity Gradient 0005 MV/m Forward Power 0005 Watts Forward Phase 0006 degrees Reverse Power 0005 Watts Reverse Phase 0005 degrees	Hz Turn Off
Waveforms Expert/Diagnostic Displays Cavity 1 Overview More Cavity 1 Cryomodule Overview Signal Calibration	Stepper Turner Cav Characterization Tone Test Piezo Tuner SEL Phase & Pulse Feedback Parms
PRODUCTION	01/29/2019 09:49:17

10. Run RF In SEL Pulsed Mode

a. Click on SEL Phase & Pulse...

The settings/options for pulsed mode are more complicated than you'd think. It's a good idea to read the README at the bottom of the screen.



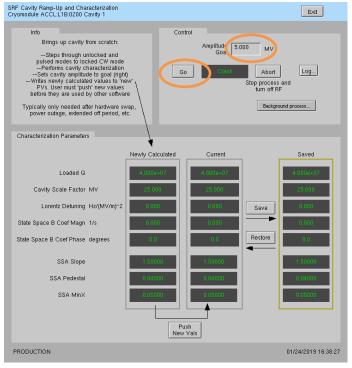
- b. Enter desired amplitude (settings will be 'yellow' if they do not match Current/Last In Use)
- c. Enter desired RF pulse length
- d. Click Go
- e. When done, click Stop
- f. To update amplitude or time settings, enter new values and then click Go again

11. Ramp Cavity to CW/SELAP and Perform Cavity Characterization

This is used to bring up a cavity 'from scratch' or if there is some need to re-characterize the cavity/SSA. You do not need to run this every time you turn a cavity on.



a. Click on Cavity Ramp-Up...



- b. Set Amplitude Goal and click Go
- c. Future (not yet done 1/29/2019): the script will write is calculated characterization parameters to the Newly Calculated values on the screen. You can review these and if they seem reasonable, click Push New Vals. You can also save the Current values as a known good set—to possibly restore in future.

II. Occasional Issues

1. Mystery Rack Checkout Error

We occasionally see a problem during the first cryomodule rack A checkout. This is what it looks like:

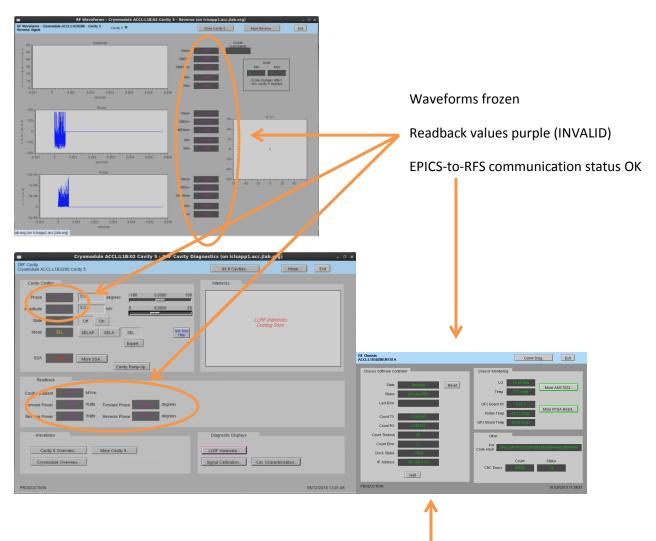
LLRF Rack Test Log File (on lclsapp1.acc.jlab.org)	x
192,168,0,102	
Write to /data/lcls-llrfcpu01/llrf/./live_prc_regmap.json	
192.168.0.102	
set_lims 0 0	
Signal min/max 0/0, amplitude 0.0 0.0, rms error 0.00 DK	
Signal min/max 0/0, amplitude 0.0 0.0, rms error 0.00 OK crc_errors clk_status_out dac_iq_phase shell_0_dsp_use_fiber_iq [60179, 2, 1, 1]	
cercements city_status_out_dat_iq_prase_shell_o_dsp_use_riber_iq_tour/s, 2, 1, 1] set lins 0 19750	
Signal win/max -2032/2367, amplitude 2032.7 9.9, rms error 63.88 BAD	
Signal min/max 0/0, amplitude 0.0 0.0, rms error 0.00 DK	
crc errors clk status out dac ig phase shell 0 dsp use fiber ig [60179, 2, 1, 1]	
set_lims 0 79000	
Signal min/max -8130/8129, amplitude 8130.0 23.7, rms error 0.52 OK	
Signal min/max 0/0, amplitude 0.0 0.0, rms error 0.00 OK	
crc_errors clk_status_out dac_iq_phase shell_0_dsp_use_fiber_iq [60179, 2, 1, 1]	
set_lims 1 19750	
Signal min/max -2032/2032, amplitude 2032,1 5.9, rms error 0.49 OK Signal min/max 0/0, amplitude 0.0 0.0, rms error 0.00 OK	
Signal wird/wax w/d, ampiridue 0.000, rms error 0.000 bk crc errors clk status out dac ig phase shell 1 das use fiber ig [60179. 2, 1, 1]	
set lins 1 7900	
Signal win/max -8130/8129, amplitude 8130.0 23.7, rms error 0.52 DK	
Signal min/max 0/0, amplitude 0.0 0.0, rms error 0.00 OK	
crc_errors clk_status_out dac_iq_phase shell_1_dsp_use_fiber_iq [60179, 2, 1, 1]	
set_lims 0 0	
Signal min/max 0/0, amplitude 0.0 0.0, rms error 0.00 OK	
Signal min/max 0/0, amplitude 0.0 0.0, rms error 0.00 DK	
crc_errors clk_status_out dac_iq_phase shell_0_dsp_use_fiber_iq [60179, 2, 1, 1]	
FAIL	

RF Rack Diagnostics - ACCL:L1B:0200 - Rack B (on lclsapp1.acc.jlab.org)	
RF Hardware Cryomodule ACCL:L1B:0200 - Rack B	it
Run Rack Self-Test	
Go Complete Abort	
Latest Self-Test Results	
Rack B	
R.ck File Script aborted. Try again. 2018-06-11-17:08:4	8 Log
RFS1 Pass	
RFS2 Pass	
PRC Pass	
Res/Intik Pass	

It is an intermittent failure and is not understood. You'll have to simply re-run rack checkout and hope it passes. (We have observed that if the system was previously set up correctly and there has been no outage/hardware swap since, it will probably work fine in spite of this error.)

2. Recover Non-Updating EPICS Waveforms

Once in a while, I've seen the EPICS waveform data stop updating. Displays will look like this:



If you see this and nothing else seems to be wrong, try pressing 'Halt', then 'Reset' on the appropriate RFS screen. If that does not recover it, then there is a problem somewhere else.

3. Ping Test

To test if a chassis pings from a CPU:

- Log into LERF workstation or server (lcls01/2/3/ lclsapp1 with individual user id)
- b. Log into cpu (using CPU Node Name from Section 1):

iocConsole <cpuname>

OR

ssh laci@<cpuname>

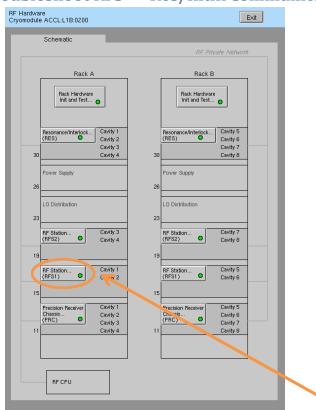
(If prompted for login, type 'laci' and hit enter.)

c. Type: ping <ip>

4. View the EPICS IOC Console

- a. Log into LERF workstation or server (lcls01/2/3/lclsapp1 with individual user id)
- b. iocConsole <iocname>
- c. To exit viewer, press these 3 keys together: Ctrl, a, d.
- d. To scroll up in viewer, press these 3 keys together: Ctrl, a, [. Then use arrows to move up/down. To exit scroll mode, press these 3 keys together: Ctrl, a,].

(If you inadvertently kill the ioc, you can restart it using the instructions in section 2.)



5. Troubleshoot RFS<->Res/Intlk Communication

a. Open Hardware screen. For the appropriate rack, click on an individual chassis



b. Click on 'Comm Diag...'



6. RF 'Background Process'

Much of the current RF functionality (rack checkout, pulse control, cavity ramp, etc.) is performed by scripts external to the EPICS IOC. This is facilitated by a continuously running background process that is driven by EPICS PVs. This allows us to execute these functions from EPICS PVs on EDM screens—and not have to manually run scripts from the command line.

On every display that relies on this, there is a button titled 'Background process...'. If that process is not running, there will be a red rectangle around it. Click on that button to open a display from which you can start/restart the process. Example:

SRF SEL Controls - ACCL B:0210	
SRF SEL Phase and Pulse Control Cryomodule ACCL:L1B:0200 Cavity 1	Exit
SEL Phase Offset	
Phase Offset 0.0 0.0 degrees -160 0.0	0 180
	🕅 🗠 RF Daemon Process - Expert
RF Pulse Control	RF Daemon Process
Desired Current/Last In Use Amplitude 6.00 MV 6.00 MV	LLRF Support Daemon
RF On Time 0.478 ms 0.478 ms	This process is needed to run rack self-test, SRF cavity ramp-up, and other RF processes.
RF Off Time 145 665 ms 0.196 ms	Status Dorf Butwilling Restart Daemon Log
Go Stop Pulsing of	
Backg	ound process
README	
Cycle Length [ms]	
Each cycle consists of: RF on, then RF off.	
Cycle length depends on waveform sampling rate and number of active waveforms. Minimum cycle length: 0.57 ms Maximum cycle length: ~240 ms	
For maximum cycle length, go here: 1. Set cavity Data Decimation factor to 255. 2. Disable Drive, DAC, and Detune waveforms for this cavity.	Expert
PRODUCTION	01/31/2019 17:19:25

This process will not successfully launch if the EPICS PVs it relies on are not all online. Both LLRF EPICS IOCs must be on.