# *APV25-SRS Electronics with 10 Gb Ethernet (Optical link) for PRad*

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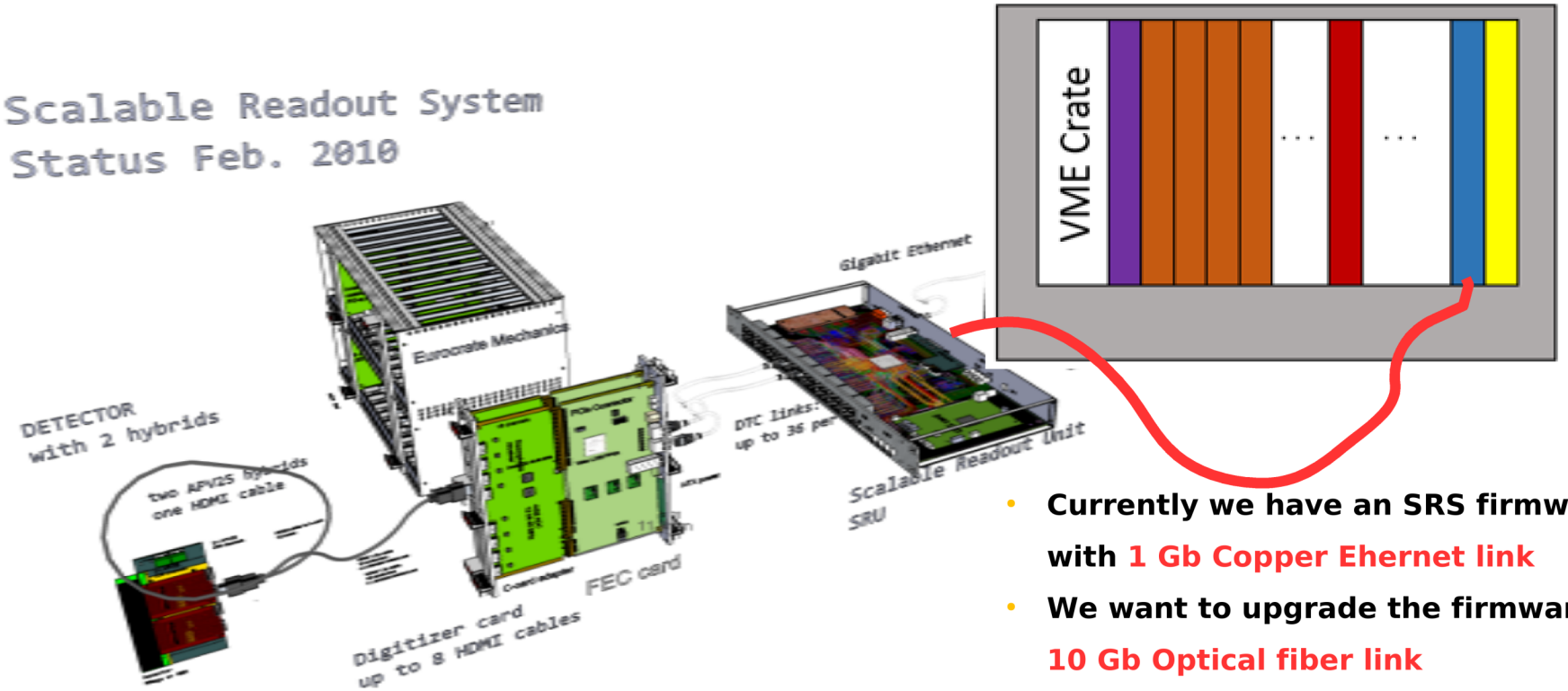
# Development needed for PRad SRS Electronics

- Integration of the SRS with CODA is ongoing by Krishna & Chao, In the current system, UDP data are sent to the DAQ PC via 1 Gb Copper link, this is the bottleneck for pRad @ 5kHz.
- We can upgrade the data transfer to 10 Gb optical fiber link. Mostly firmware part need some development ⇨ SRS Hardware capability is already there and I assume the VME base CPU is also able to handle 10 Gb link
- A version of the firmware with 10 Gb link is available (developed and tested at CERN but this version is not compatible with the current firmware readout the APV25 electronics




- **Currently we have an SRS firmware with 1 Gb Copper Ehernet link**
- **We want to upgrade the firmware to 10 Gb Optical fiber link**

# Performances of APV25-SRS with 1 Gb Link @ UVa

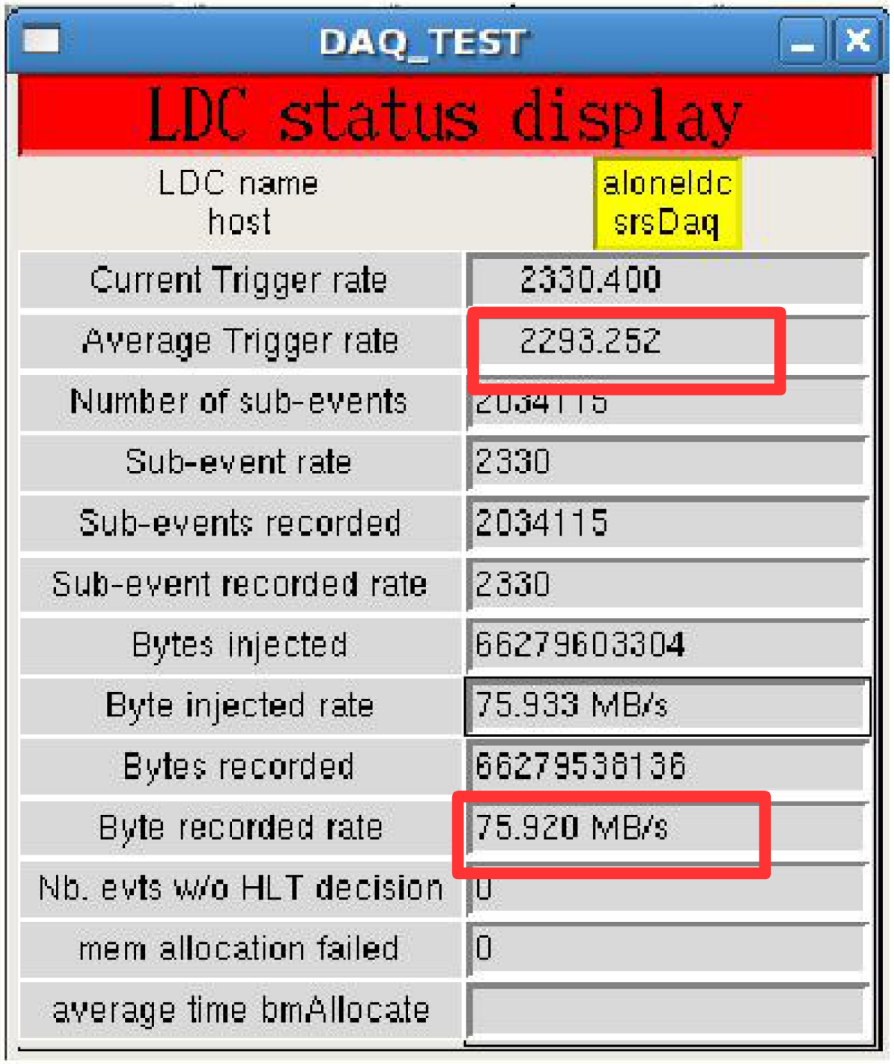
## with Firmware compatible with APV25 electronics

Measured maximum trigger rate

| | 32 APVs | 64 APVs |
|---|---|---|
| 3 TS | 2.3 kHz | 1.2 kHz |
| 6 TS | 1.15 kHz | PRad 1 kHz at 125 MB |
| 12 TS | 0.6 kHz | |

- High rate means less APV25 cards and/or less time samples (TS)
- 2.3 kHz trigger rate with 3 time samples with 32 APV25 cards
- Very similar to the pRad requirements for the readout electronic

**2.3 kHz @ 32 APV25 (4096 chs) and 75 MB/s**

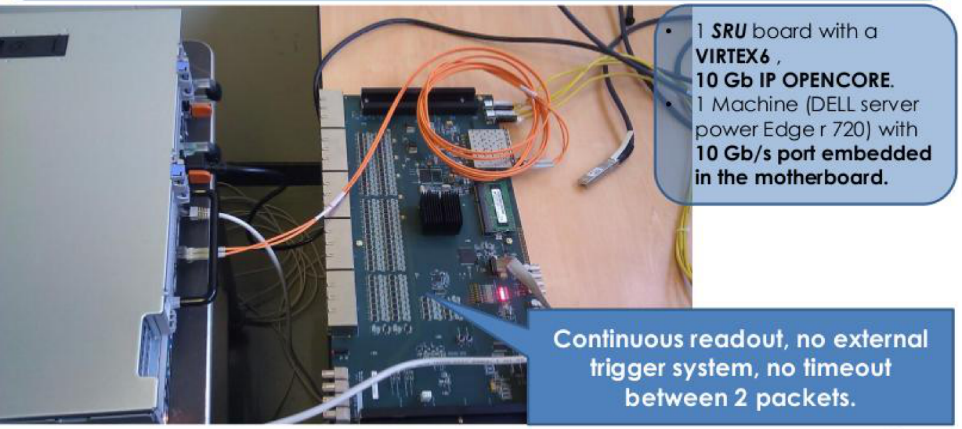


# Performances of SRS with 10 Gb optical Link

**(Filippo Costa, ALICE DAQ - CERN)**

## UDP Ethernet 10Gb

The evaluation for UDP Ethernet data transmission protocol has already started.
Preliminary tests have been performed together with RD51 collaboration (***Hans MULLER, Alfonso TARAZONA MARTINEZ***).
A test system has been prepared:



- 1 ***SRU*** board with a **VIRTEX6** , **10 Gb IP OPENCORE.**
- 1 Machine (DELL server power Edge r 720) with **10 Gb/s port embedded in the motherboard.**

**Continuous readout, no external trigger system, no timeout between 2 packets.**

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**Courtesy Filippo Costa, ALICE DAQ group @ CERN**

Test with **software generated test data**

10 Gb firmware does not have the APV25 implementation

**100 kHz @10 kB ⇨ 10 kHz for 100 kB**

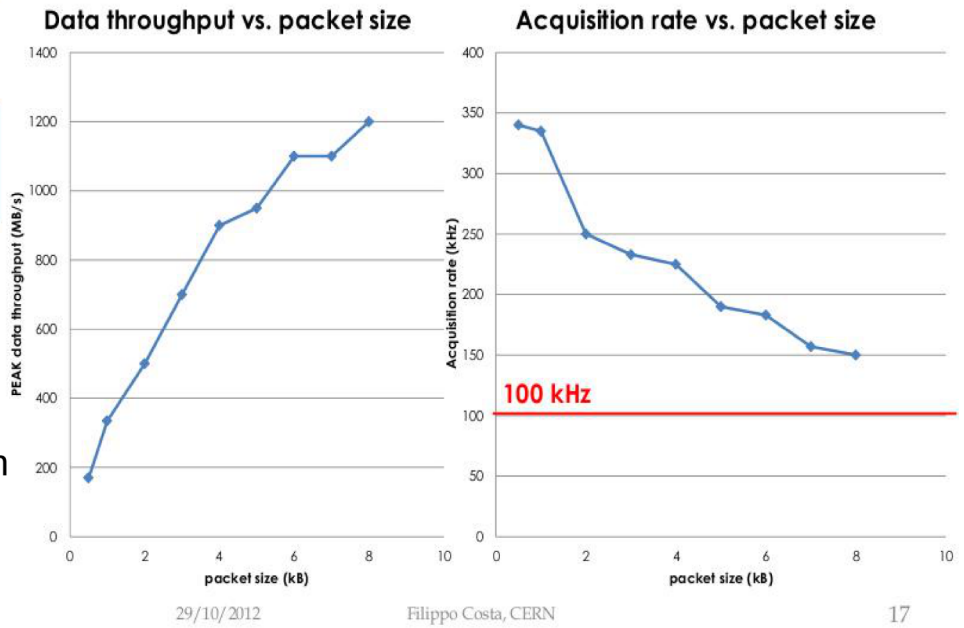
**100 kHz @10 kB ⇨ 10 kHz for 100 kB**

I00 – 200 kB event size @ 5 kHz trigger rate expected for PRad GEMs

Both 10Gb firmware & APV25-1Gb firmware available

**Need some work to merge the two into a 10Gb APV25-compatible firmware**

## UDP Ethernet

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# Implementation of the 10 Gb link for PRad

- I Met with Ben Raydo on Wednesday Nov 18 to discuss the possibility to implement the 10 Gb firmware for PRad APV25-SRS electronics
- I sent the firmware to Ben after the meeting and from preliminary evaluation, it seems like the amount of work that he needs in not crazy
  - We are projecting some preliminary tests with the hardware in the first week of December.
  - I would then bring part of UVa-SRS to Jlab, need the SRU (so far not part of Krishna setup)
- The effort by Krishna / Chao … to improve the acquisition rate will be carried out independently and in parallel with the 10 Gb implementation but will converge at the end.
  - We would also need to test the readout list code with multiple FECs + SRU
- Ben also raised a few issues/point that we would need to look at:
  - How we deal with UDP packet loss at high rate?
    - Do we have some handshake mechanism in place for that?
  - How to deal with large data being copied to the disk/tape … ?
- Recommend that these issues are brought to Sergey...

# Checking and dealing with UDP packet drop

- Fortunately, there was a group in the RD51 collaboration that develop some software/firmware for the SRS electronics to deal precisely with the possibility of UDB dropping packet at high rate
- I am going to get in touch with this group and try to see if we can benefit from what they have develop and how it would fit with our need
  - Might be that additional firmware development might be required in that case we would still be requesting the help from Ben
  - Definitely part of software development and might be at readout list level in the VME-CPU

# Zero suppression: Firmware or software

We also discussed whether the implementation of the zero suppression in order to reduce the GEM event data size and increase the DAQ rate

- Zero suppression in the firmware (FEC FPGA) is currently under test/development within RD51

  **BUT:**

  - It is a pre-beta version that would not have been thoroughly tested for when PRad need it
  - It does not deal with the common mode correction which is critical with APV25 electronics
  - Was developed for the latest FEC version FECv6 which has FPGA Virtex 6 more ressources and memory that the FEC v3 that we had at UVa for Prad.
  - I am going to get in touch with this group and try to see if we can benefit from what they have develop and how it would fit with our need

- However a software version of the zero suppression could be implemented at the VME-CPU level
  - I guess the readout list or CODA utilities could take care of that
  - then we could still achieve the huge data reduction
  - But we would need to evaluate the required performance of the CPU module ...