PRad GEM and DAQ integration

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University of Virginia

On behalf of the PRad Collaboration

Outline

- **PRad GEM Chamber**
  - **Chamber design & Construction**
  - **Preliminary results of Chamber I**
- **Readout Electronics and DAQ system**
  - **The Scalable Readout system (SRS)**
  - **Integration into Jlab DAQ CODA**

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- PRad GEM Chamber
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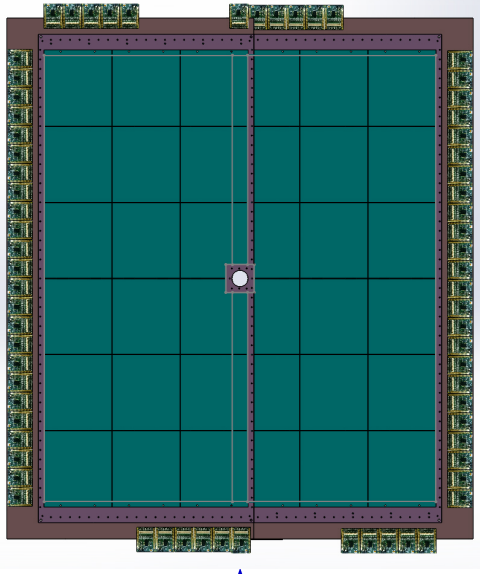
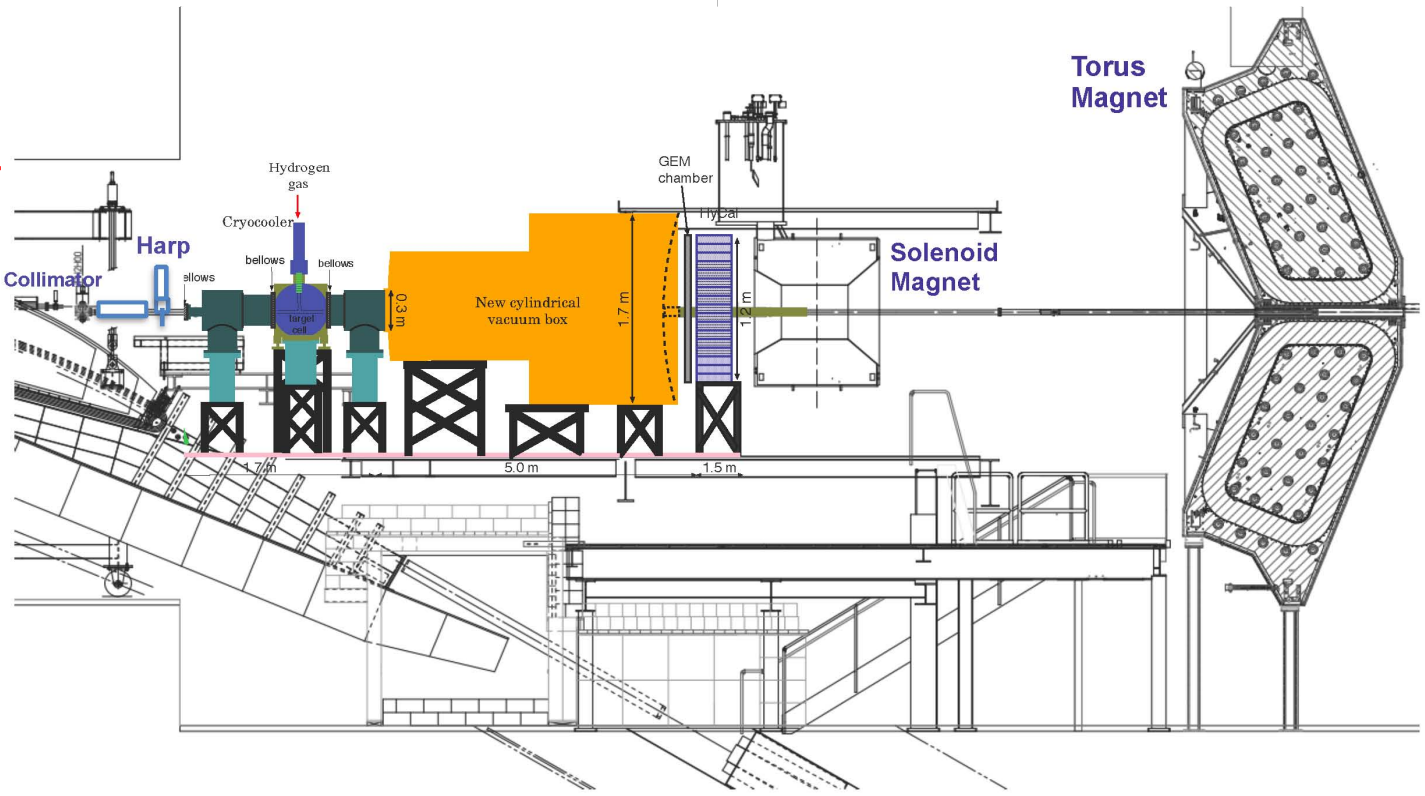
GEMs for PRad Experiment in Hall A @ JLab

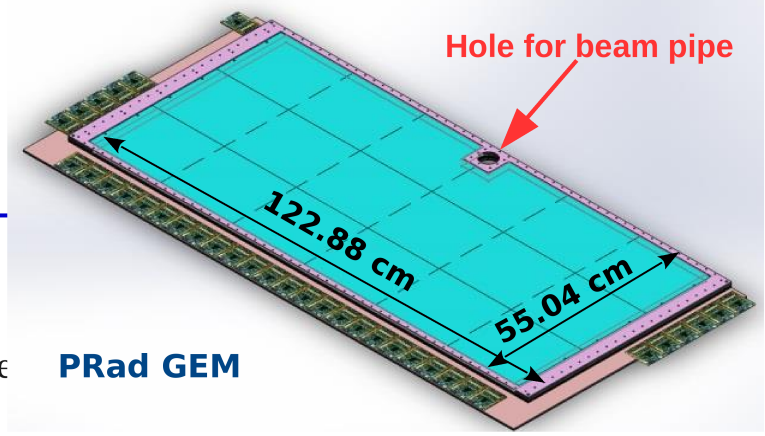
PRad GEM chamber





Distance: 2H00 wire harp to Solenoid support frame ~13.7 m

× 2



PRad GEM

PRad GEM Chamber design

PRad GEM chambers

Triple-GEM detector based on the so called (3-2-2-2)-COMPASS GEM design

2D (X-Y) COMPASS style readout board

Specific features of the chambers

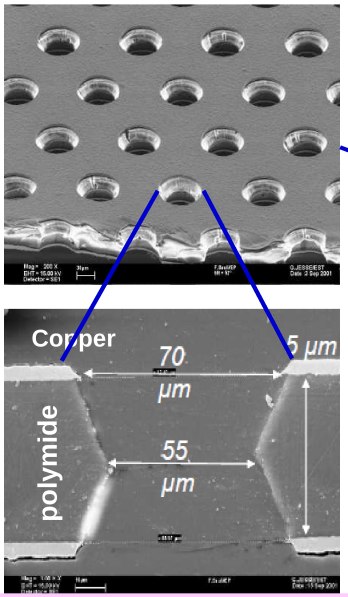
GEM foils & readout glued to support frames

Framed GEMs are NOT glued together

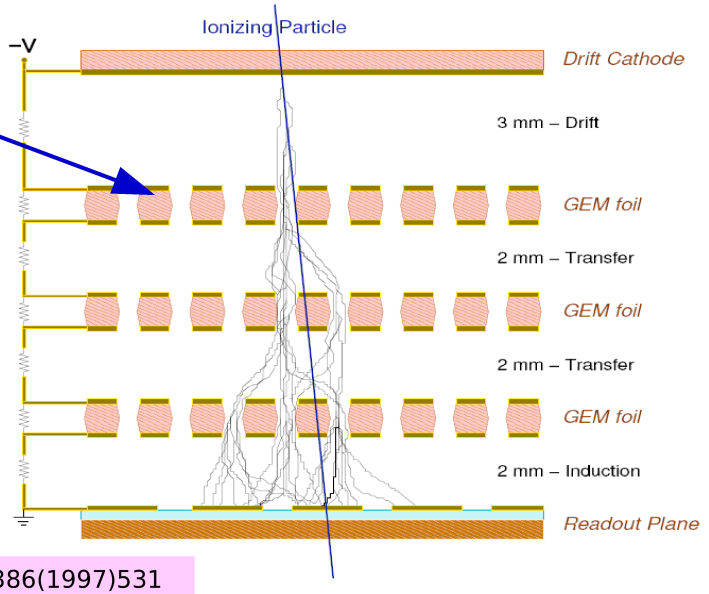
Chamber is closed and sealed with a set of screws and O-ring

Allow the possibility to re-open the chamber to replace part if necessary

GEM foil

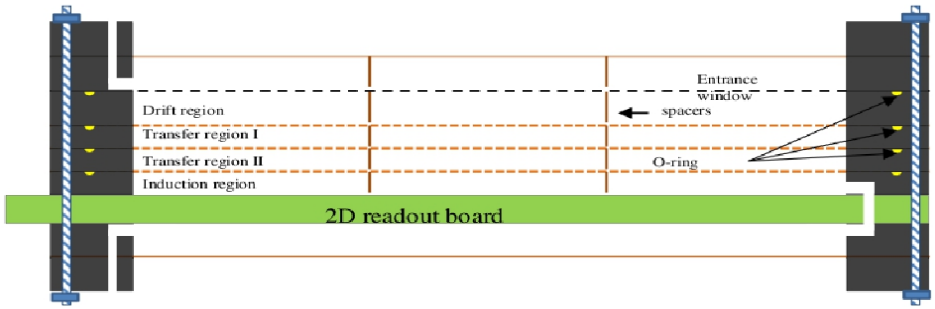


COMPASS triple-GEM design

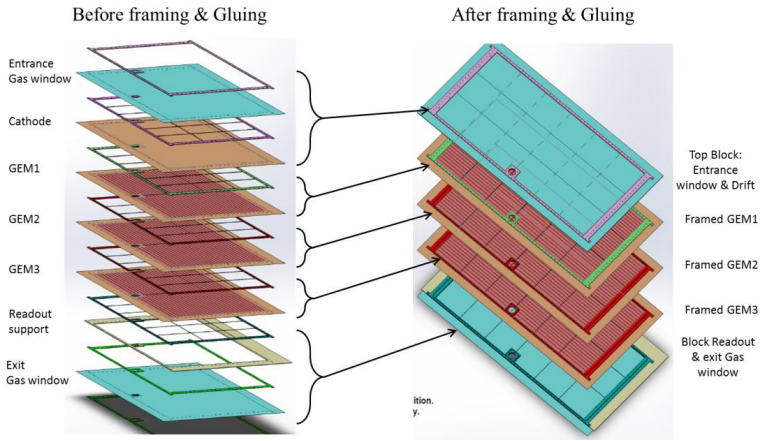


F. Sauli, Nucl. Instr. and Meth. A386(1997)531

Cross sectional view of PRad triple-GEM With O-ring and screw to seal the chamber



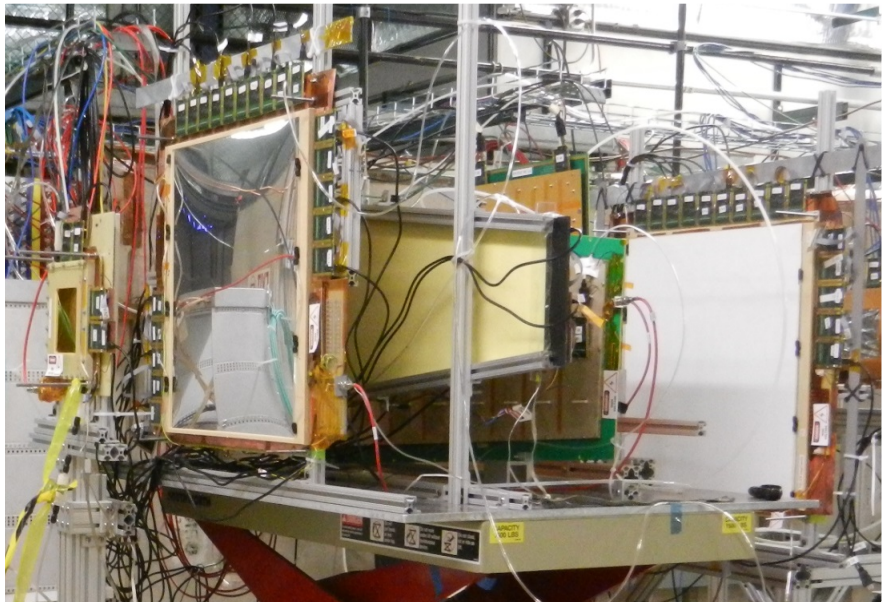
3D view of the PRad triple-GEM



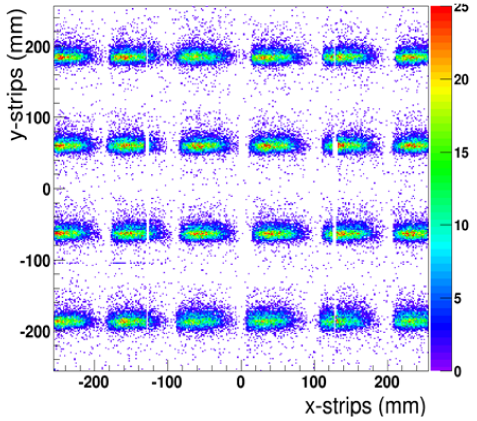
Performances of Triple-GEM in Test Beam

- ✔ **GEM prototypes similar to the PRad GEMs, built for Super Bigbite Spectrometer (SBS), were tested at FNAL in 2013**
- ✔ **The SRS electronic was used to read out the prototypes at trigger rate 400 Hz during the test beam**

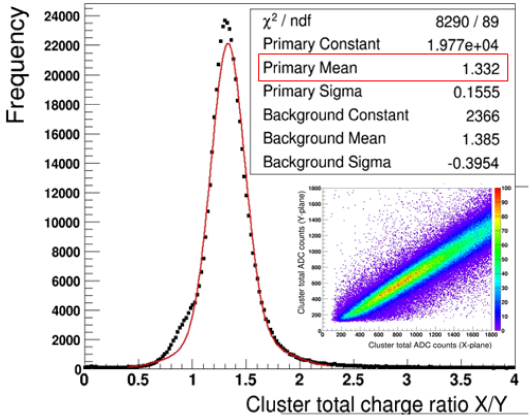
SBS GEM prototypes in test beam @ Fermilab Test Beam Facility (FTBF) in Oct. 2013



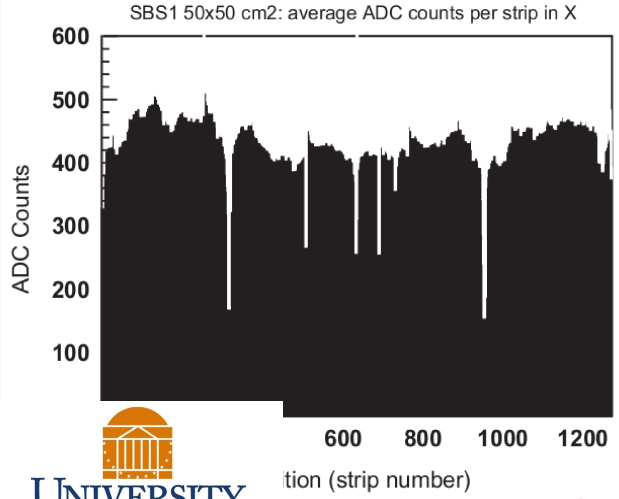
Hadron beam reconstruction

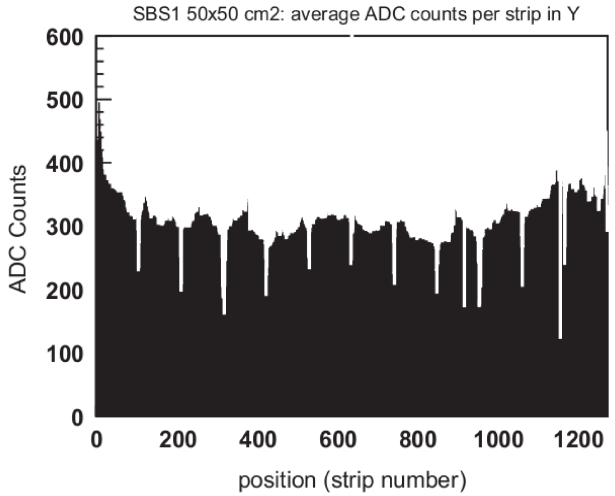


Charge sharing

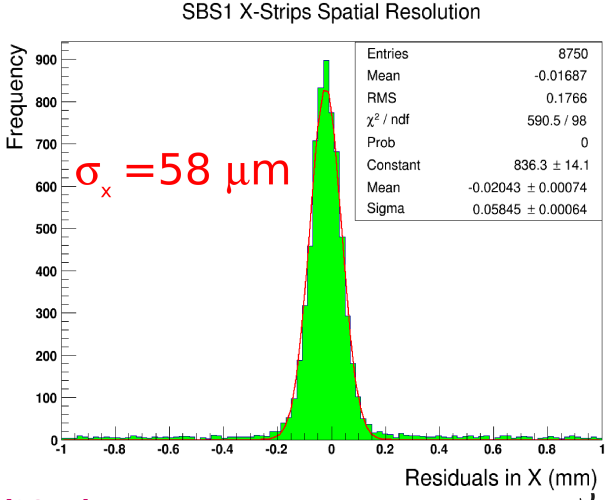


Gain uniformity





Spatial resolution



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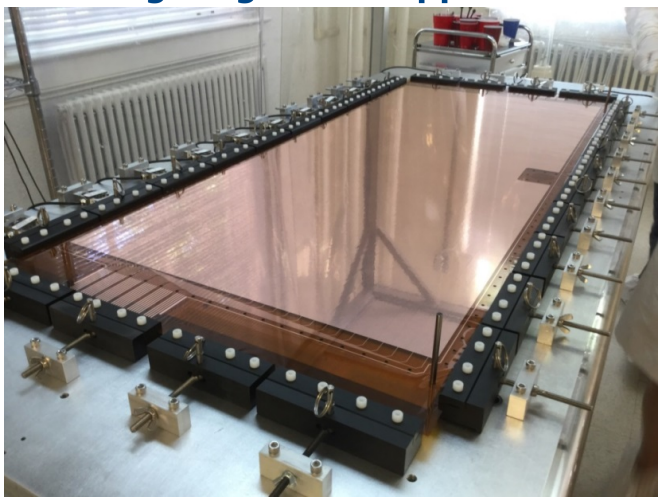
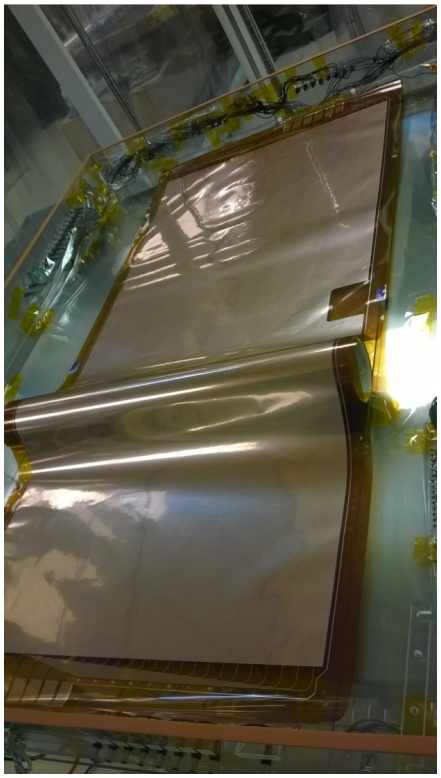
K. Gnanvo et al. Nucl. Inst. and Meth., A782, 77-86 (2015)

Construction of PRad GEM Chamber I

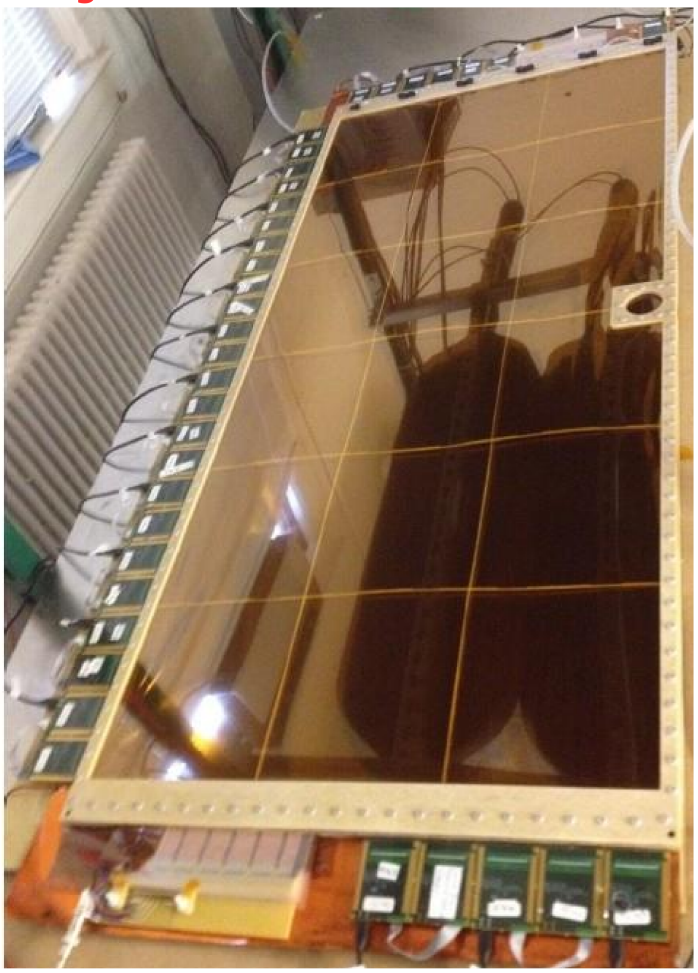
GEM foil on mechanical stretcher before gluing to its support frame



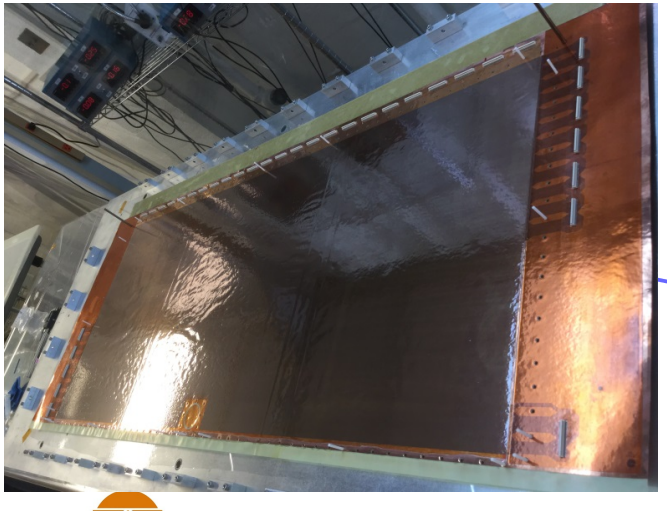
HV test of GEM foil in N2 environment

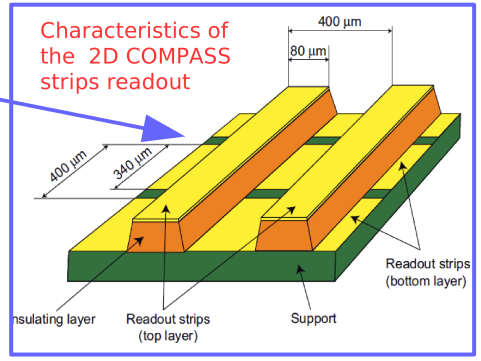


Completed Prad GEM chamber I
Largest GEM detector ever built



2D X-Y strips flexible readout





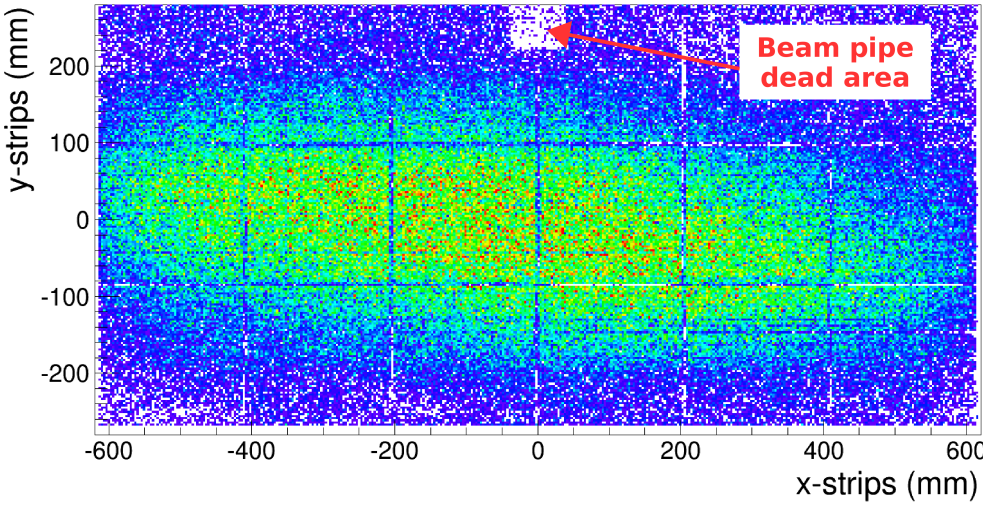
- **GEM foils & readout board fabricated at CERN PCB workshop**
- **Support frames made of G10 fiberglass by RESARM, Belgium**

Preliminary Results of PRad Chamber I with cosmics

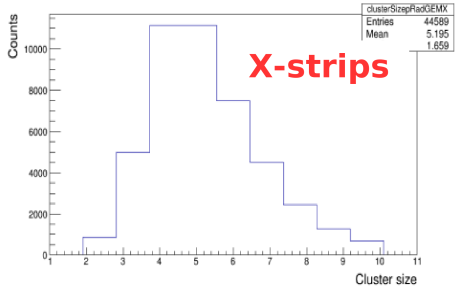
PRoton Radius

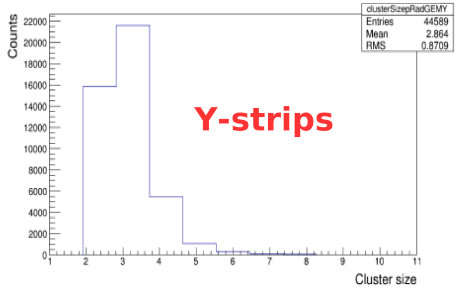
Cosmic bench setup for PRad GEM setup

Cosmic hits cluster position map

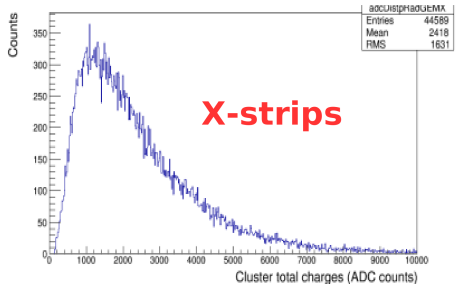


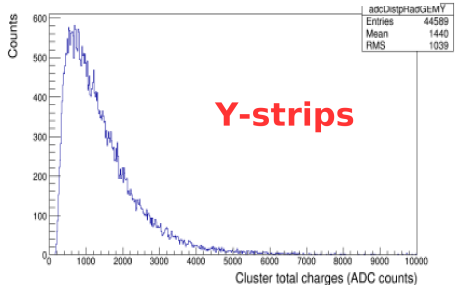
Cluster size (avg. nb strips above threshold)





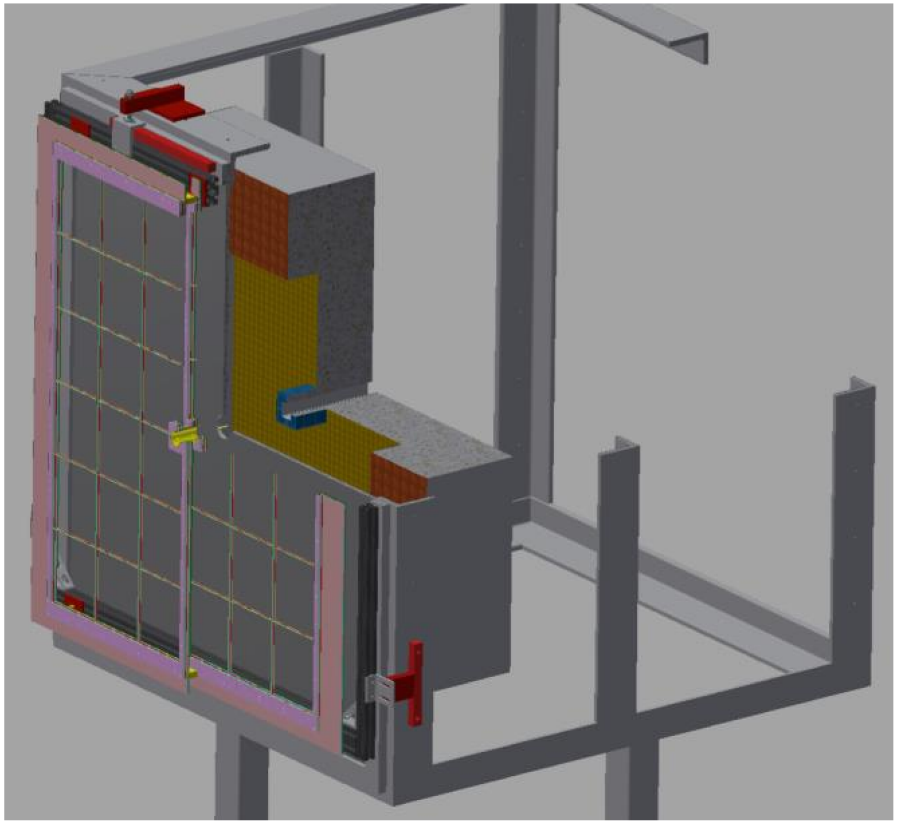
MIP energy loss distribution (ADC counts)





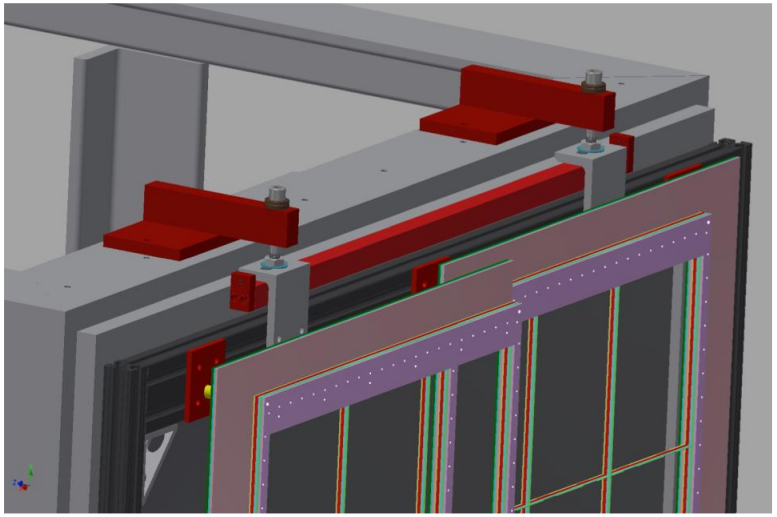
GEM chambers Mount on HyCal

- **Conceptual design by Duke/JLab**
- **Remaining work:**
  - engineering design in progress
  - construction (in local shop), ready by Jan. 2016

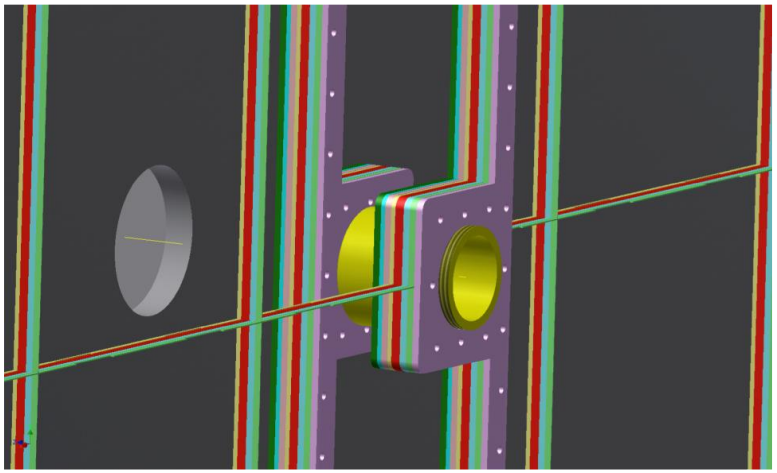


(Fig. courtesy of A. Gasparian)

Detail of the mounting structure



Beam pipe hole structure



Plans for the next two months

PRad GEM chamber I completed

- ✔ Successfully tested on cosmic showing very good response over the entire active area
  - ⇨ No loss of HV sector
- ✔ Preliminary test showed expected performances of a COMPASS like triple-GEM
- ✔ Chamber will be send to JLab (end November 2015) for further commissioning
  - ⇨ Efficiency and spatial resolution measurement

Assembly of PRad GEM chamber II just started

- ✔ Should be completed by end of November
  - ⇨ We expect about 3 weeks construction time
- ✔ 2 weeks preliminary test will be performed in the Detector Lab @ UVa
  - ⇨ Prad GEM II could be sent to JLab just before Christmas break for commissioning

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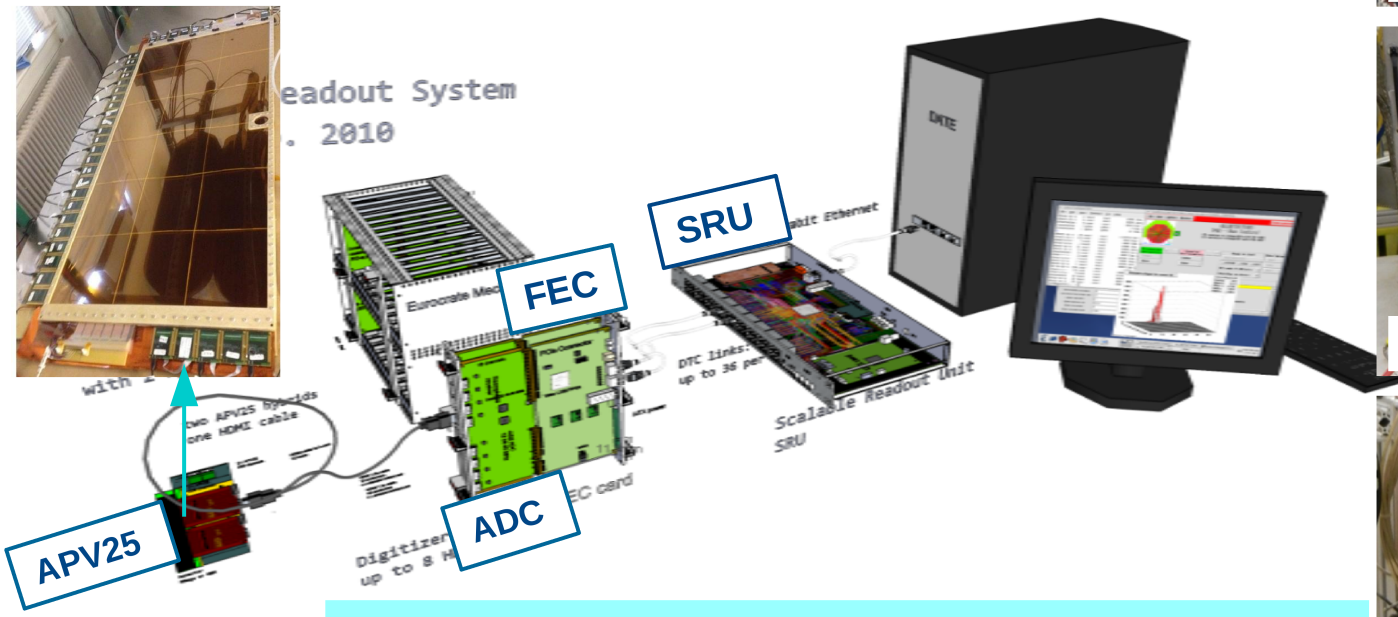
  - The Scalable Readout system (SRS)
  - Integration into Jlab DAQ CODA

Scalable Readout System Electronics for PRad GEMs

(Hans Muller, RD51 Coll. @ CERN)

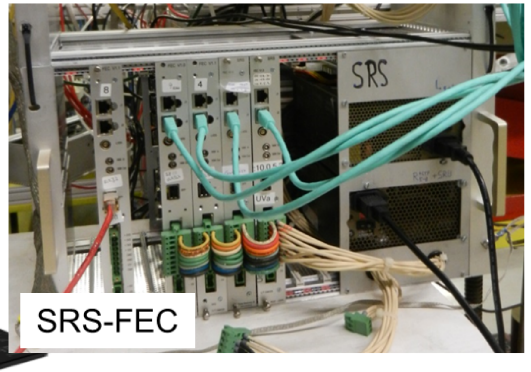
The Scalable Readout System (SRS)

- ✔ APV25-based system developed by the international RD51 Coll. based @ CERN
- ✔ Front End cards on the chamber host the APV25 chip ⇨ send data to ADC via HDMI cables
- ✔ ADC cards interfaced with the FPGA board (FEC card) ⇨ FEC data fragment to the SRU
- ✔ SRU send the data fragment from many FECs to the DAQ PC through Gb Ethernet



SRS Electronics @ UVa:

- 96 APVs ⇨12 k channels
- 5 ADC/FECs combos
- 1 + (1) SRUs

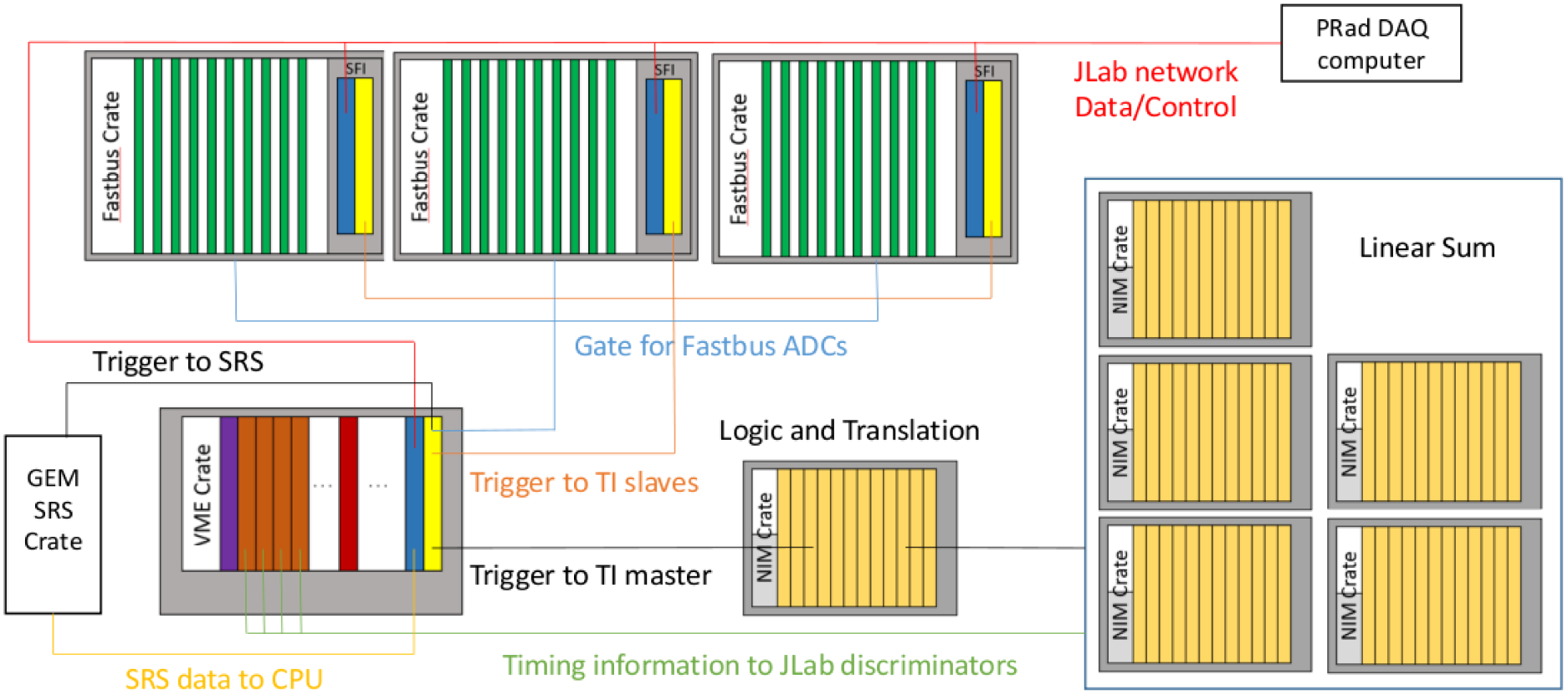


The Need for PRad GEMs readout:

- 72 APV25-FE cards (UVa) to readout 9216 channels
- 5 (6*) ADC/FECs Combo (4 (5*) UVa + 1 MSU)
- 1 (2*) SRU board (UVa) ⇨ 1 (2*) CPUs

(*) Ideally 1 CPU/SRU + 3 ADC/FEC + 36 APVs per GEM chamber

PRad DAQ System Overview



(Fig. courtesy of Chao Peng)

Integration of the SRS into JLab CODA

(K. Adhikari, L. Ye & D. Dutta, Mississippi State U.)

The integration of the SRS electronics into JLab CODA was done successfully

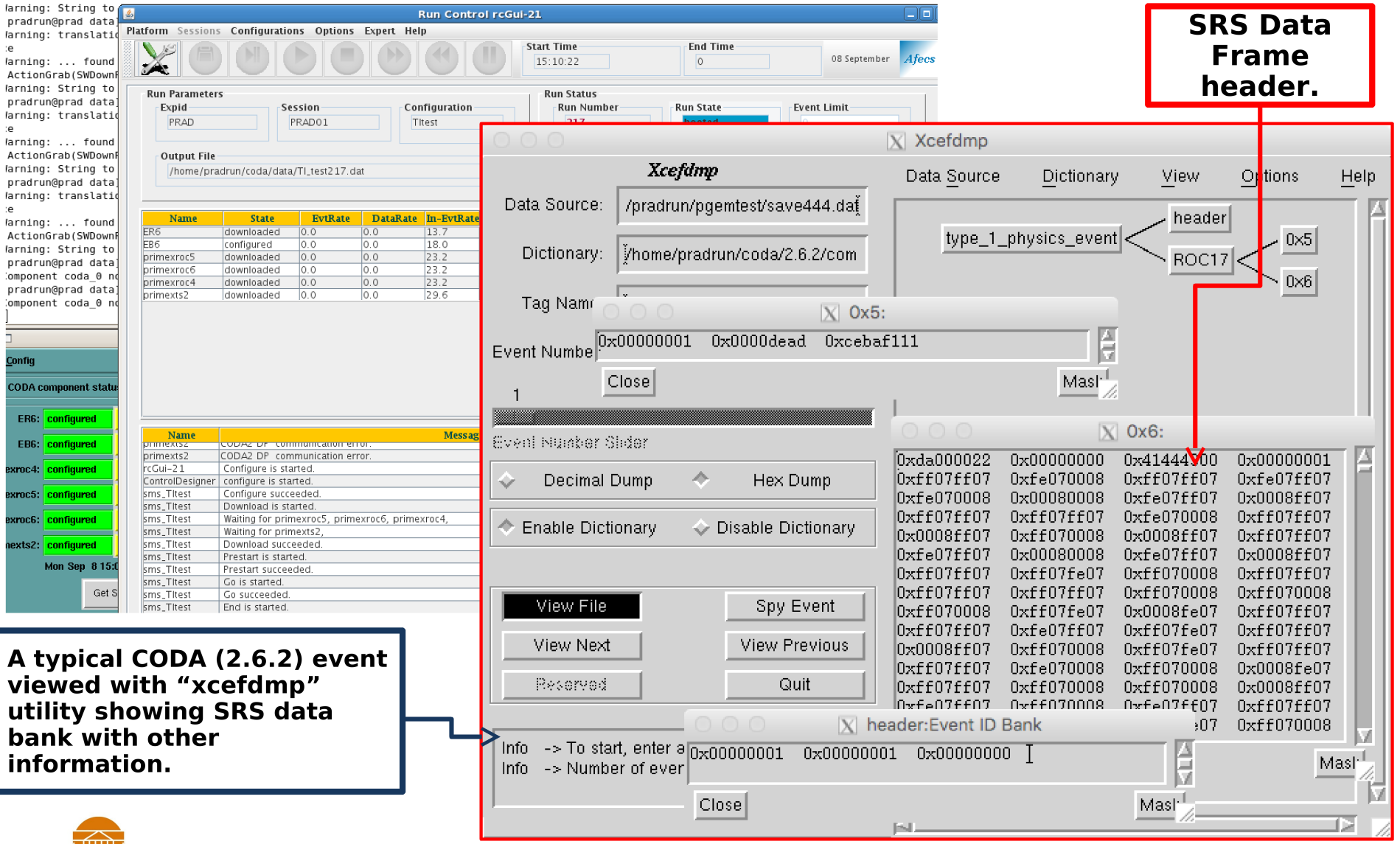
- ⇨ Development of CODA readout list to transfer SRS data via UDP protocol
- ⇨ Preliminary tests were made with the trigger through PCI-TI
- ⇨ Trigger with VME-TI & SRS data through VME-CPU is ongoing.

Current work focus on the integration into PRad DAQ system in Hall B

- ⇨ The development is under test
- ⇨ acquisition rate is still very low (work in progress)

Example of a typical CODA Event with SRS data

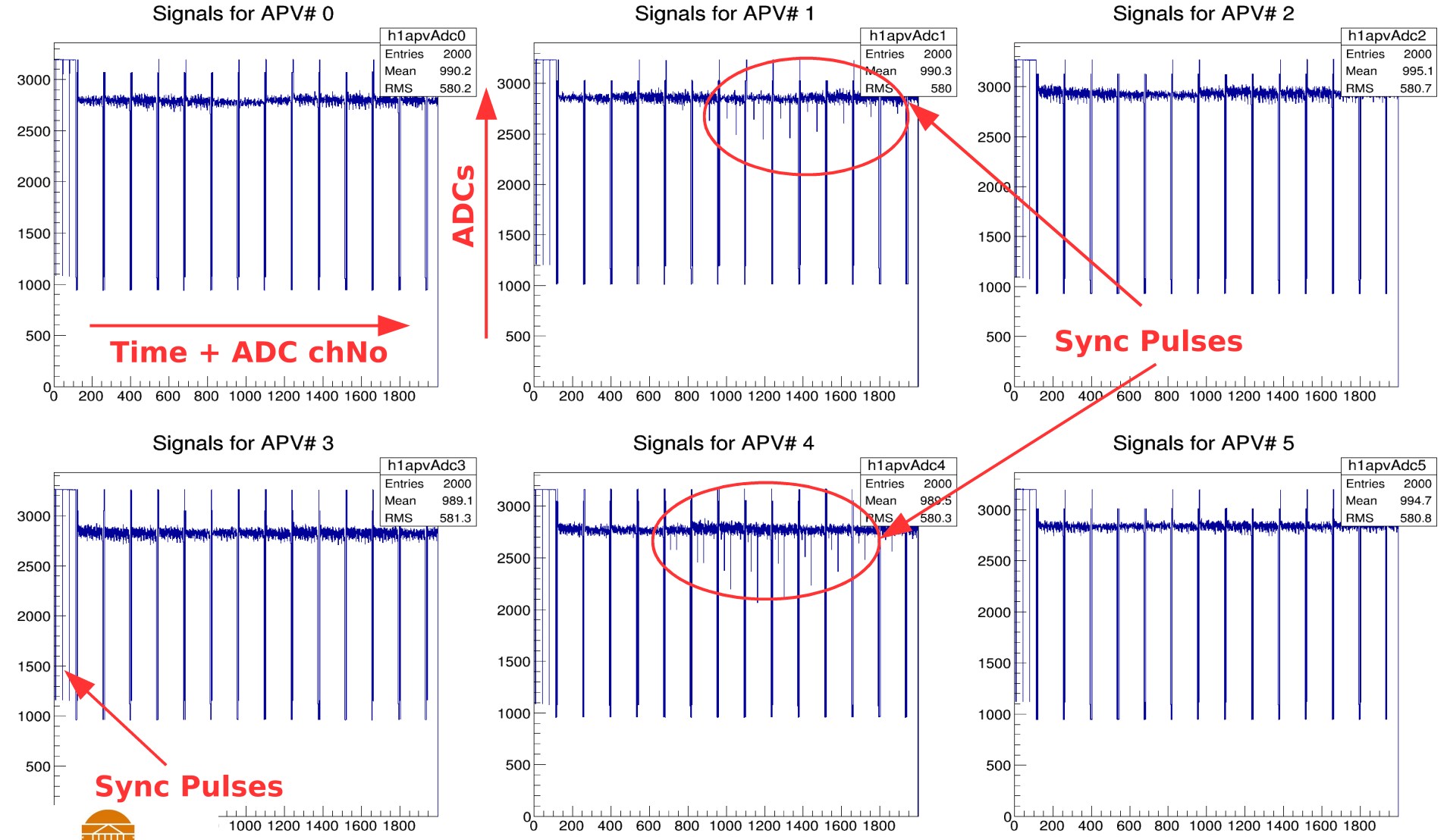
(K. Adhikari, L. Ye & D. Dutta, Mississippi State U.)



A typical CODA (2.6.2) event viewed with "xcefdmp" utility showing SRS data bank with other information.

APV25-SRS Data read out from CODA

(K. Adhikari, L. Ye & D. Dutta, Mississippi State U.)



Plans for the next two months

Test of the rate capability of the SRS with CODA

✔ Evaluate the rate capability of the SRS-CODA system

⇨ We want to the electronic to take data at a trigger rate of 2-3 kHz

✔ Outcome of the test will determine if one or two SRS / CPU combos is needed for the PRad run

⇨ the hardware is available for two SRU / CPU combos

✔ We expect to complete the test by Christmas break

✔ We should be able to commission the two GEM chambers fully equipped with the SRS electronics at high rate sometime in January 2015

Summary

GEM chamber I completed and Chamber II under construction

- Chamber I under test on the cosmic tst setup for several weeks.

  ⇨ Good response overall, No sector loss
- Construction of chamber II just started ⇨ expected to be completed in about about 3 weeks
- Chamber I & II will be at JLab before Christmas break for further commissioning

  ⇨ Efficiency and spatial resolution measurement

  ⇨ PRad GEM chambers on the mount frames by end January, ready for the experiment

Readout electronics of PRad GEM chambers

- The GEMs would be read out with APV25-based SRS electronics available at UVa
- Integration of the SRS electronics into JLab DAQ CODA was performed
- Preliminary tests are successful, development is ongoing

  ⇨ Further tests will be performed in December 2015 to evaluate the rate performances

  ⇨ Development of the decoder and analysis software development to start in January 2016

GEM & Readout Electronics Team @ UVa

Nilanga Liyanage, Vladimir Nelyubin

Kondo Gnanvo, Huong Nguyen,

Xinzhan Bai, Danning Di, Rong Wang

and

Yan Huan (Tsinghua University, China)

Yang Zhang (Duke University)

Thank you

GEM DAQ Team @ MSU

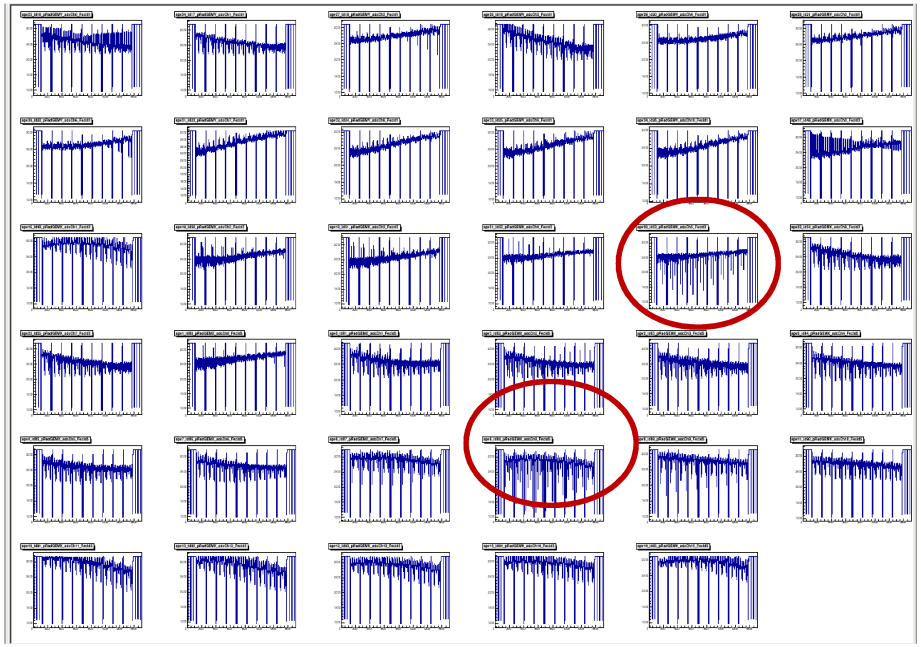
Dipangkar Dutta,

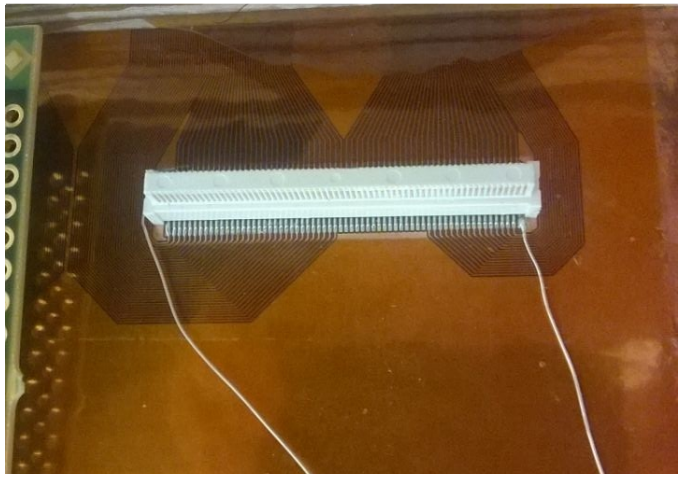
Krishna Adhikari, Li Ye

Back Up

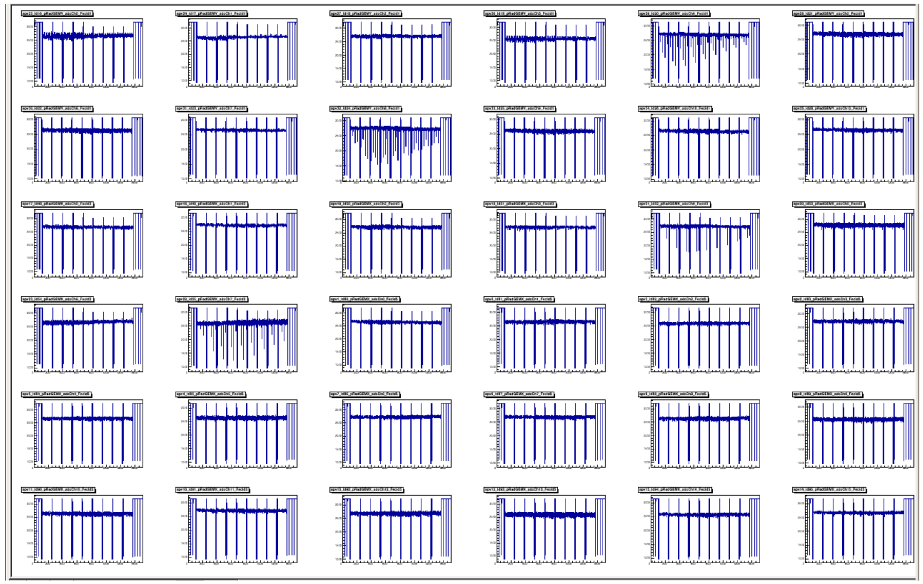
Readout Electronics for PRad GEM

before Noise Cancellation





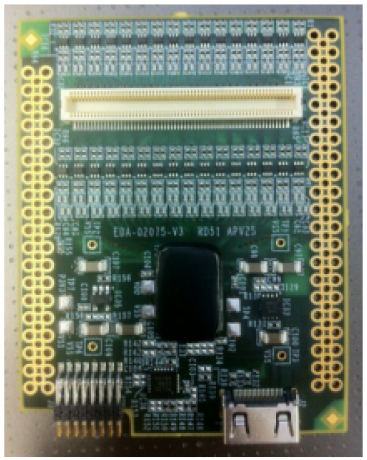
after Noise Cancellation



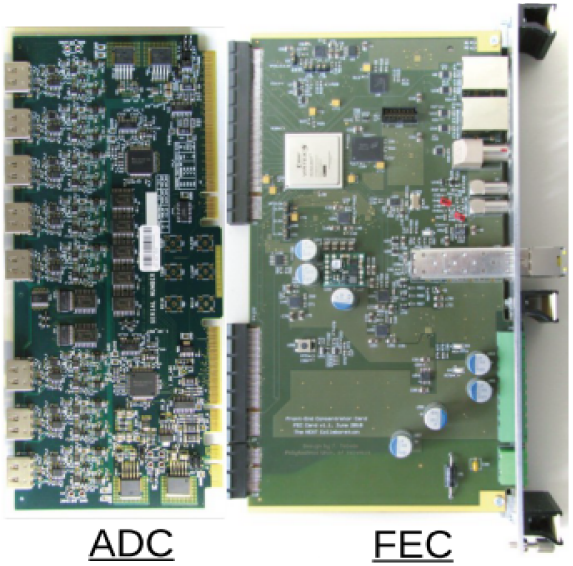
- 130 pins on Panasonic connector.
- 128 pins serve as signal lines.
- 2 extra pins provide ground level for APV front end cards.

The Scalable Readout System (SRS)

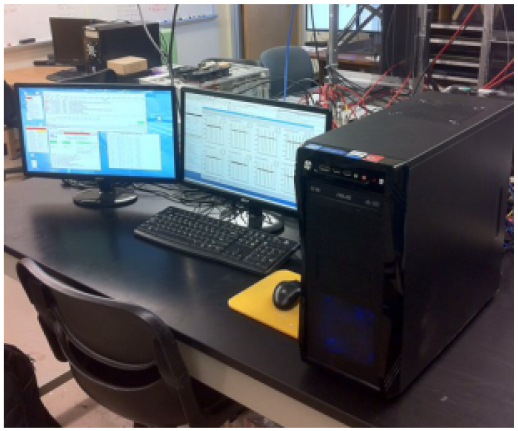
- Developed by RD51 collaboration at CERN
- Flexibility in choosing the chip frontend (ASIC, hybrid) for a detector readout
- Possibility of a common readout backend with standard DAQ Software
- Uses links instead of buses: more reliable, longer distance and more bandwidth
- Scalibility - from minimal systems (few links) -> to large systems (more links and SRUs)
- Combines 3 streams: single DTC (Data, Trigger, Control) link (copper or fiber)
- Cheap & standard: FE card chassis (Eurocrate), cables (CAT6), fibers (850 nm MM), 1 Gb Ethernet
- Radiation protected on FEC and SRU FPGA chips



HDMI



Gb Ethernet



APV25 Hybrid

- 128 channel APV25 chip
- 192-deep analog sampling memory
- Master/slave configuration
- Diode protection against discharge
- 130-pin Panasonic connector
- Mini HDMI (type C) connector

ADC

- 2 × 12-Bit Octal ADC
- 8 × HDMI input (16 APV hybrids)

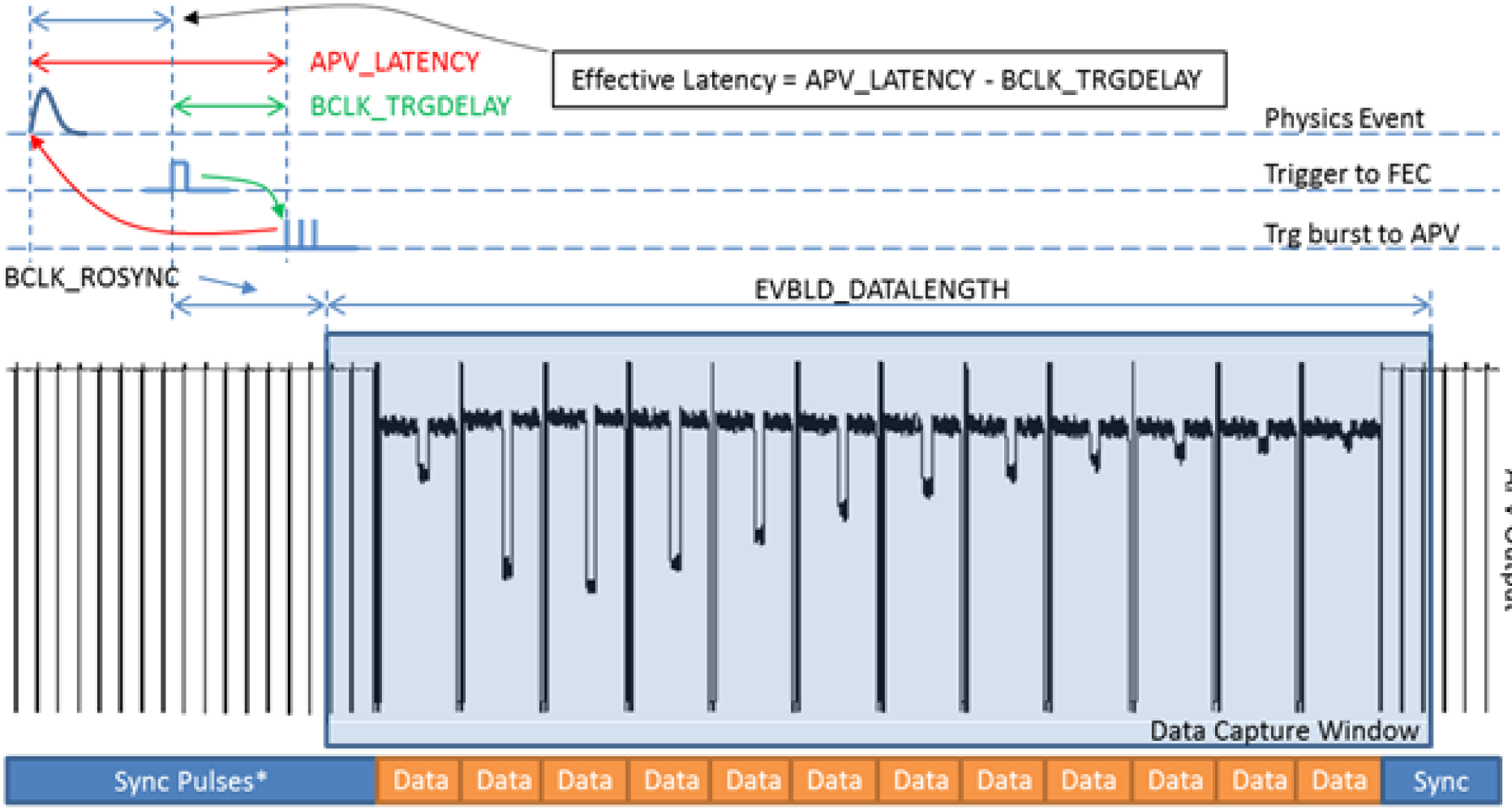
FEC

- Virtex LX50T FPGA
- SFP/Gb Ethernet/DTC interface
- NIM/LVDS GPIO
- (trigger, clock synch, etc.)

DAQ Computer

- Data Acquisition using CODA (JLab)
- Data transfer via UDP
- Slow control via ethernet

APV25-SRS trigger latency structure



Picture source:
http://test-rd51-wg5-v2.web.cern.ch/test-rd51-wg5-v2/srsdoc/SRS_Short_User_Guide.htm