Update on PRad GEMs, Readout Electronics & DAQ

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Outline

- ✓ PRad GEMs update
- ✓ Upgrade of SRS electronics
- ✓ Integration into JLab DAQ system
- ✓ Cosmic tests in EEL

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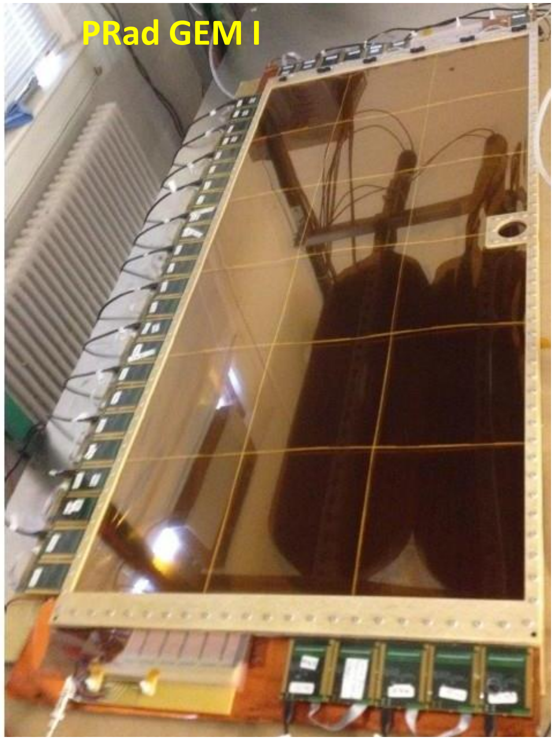
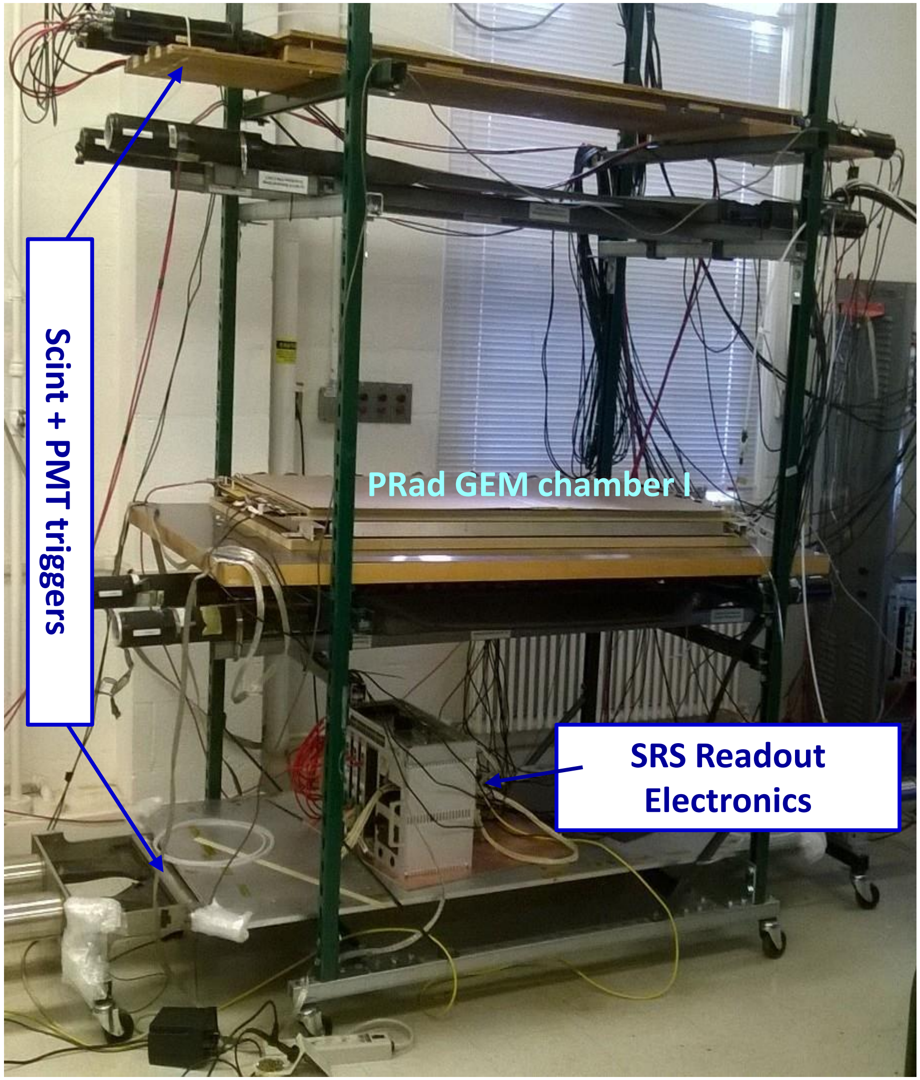
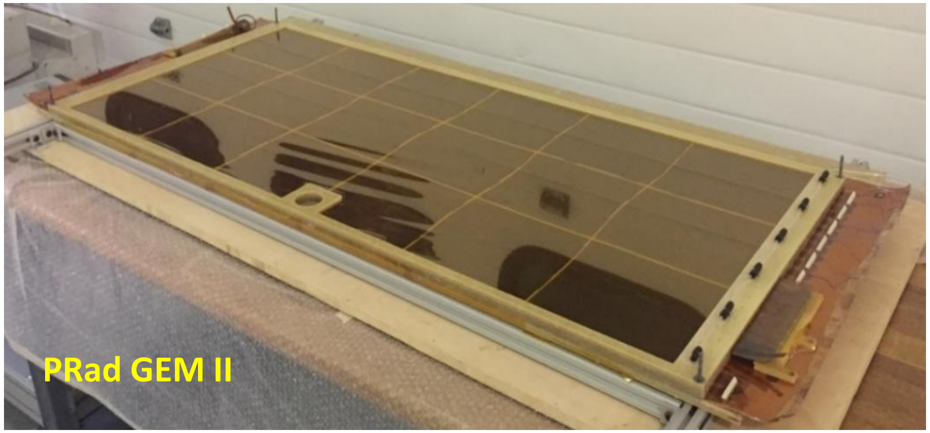
PRad GEMs Update: Assembly @ UVa



- Both chambers were completed in February
- Cosmic test performed on check all sectors active
- Basic characterization of the performances are evaluated

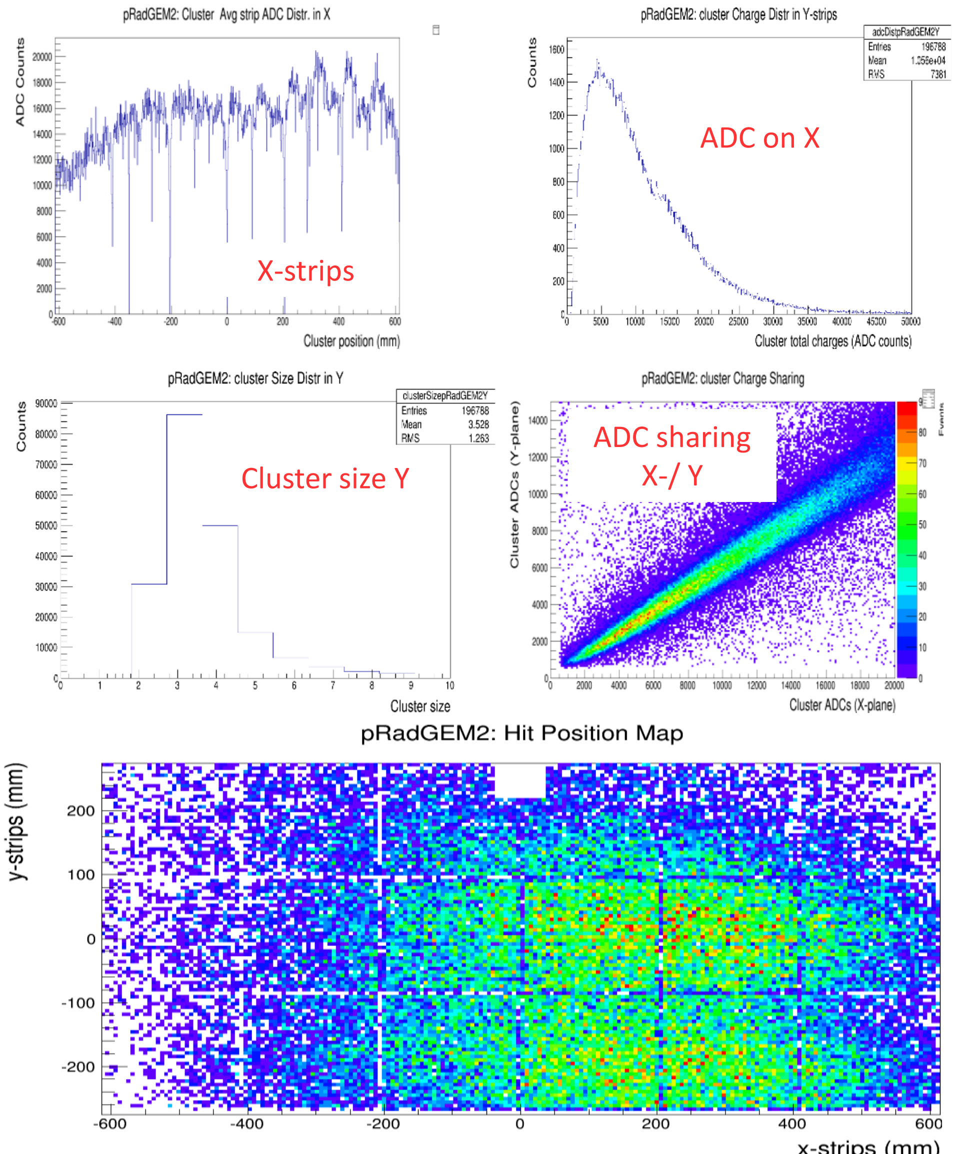
Cosmic bench setup for PRad GEM setup





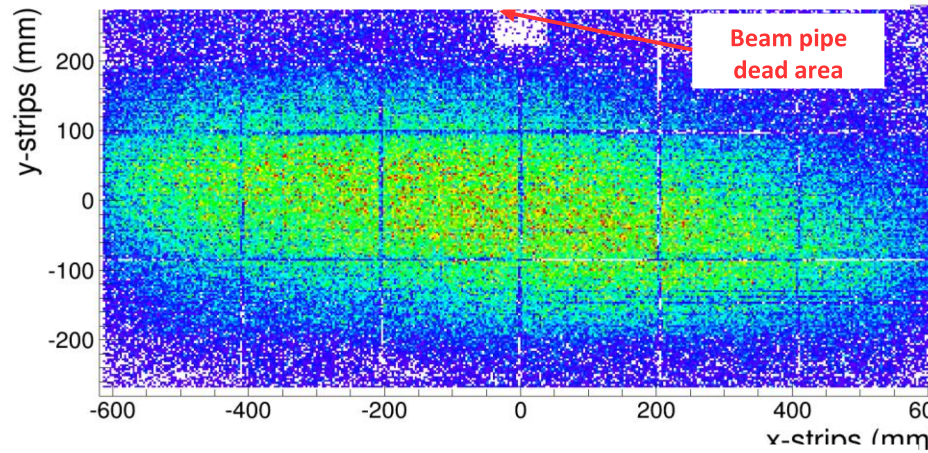
PRad GEMs Update: Results from Cosmic tests @ UVa

PRad GEM II

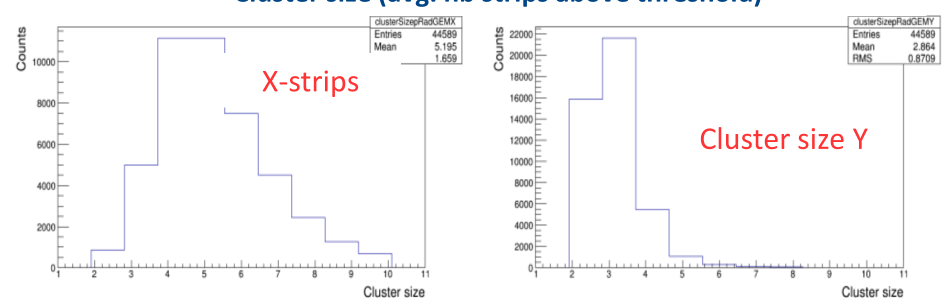


PRad GEM I

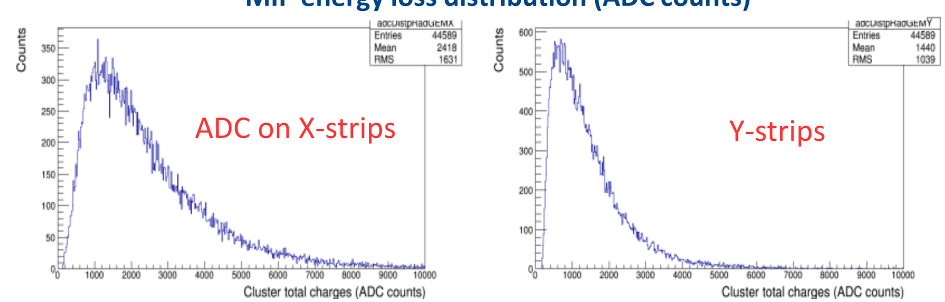
Cosmic hits cluster position map



Cluster size (avg. nb strips above threshold)



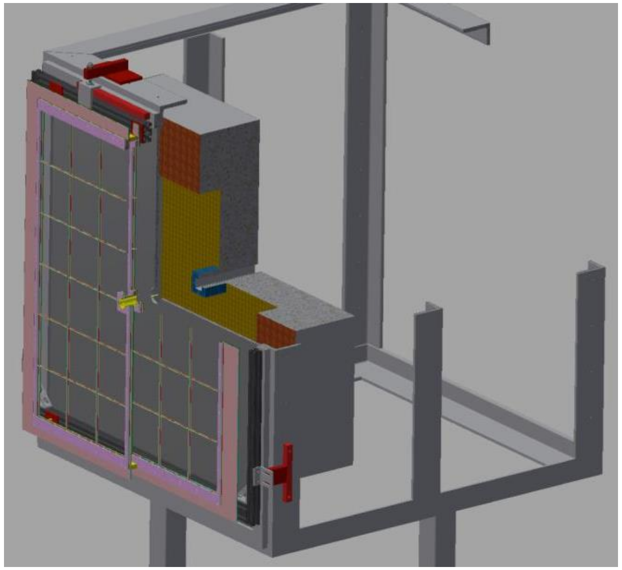
MIP energy loss distribution (ADC counts)



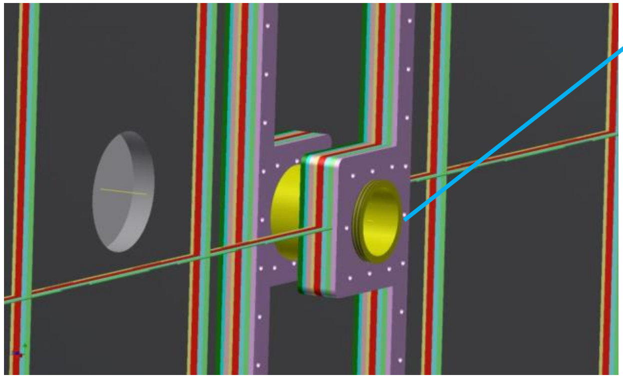
PRad GEMs Update: Both chambers @ in EEL JLab

- Moved to JLab in Feb. 2016
- Mounted on the Aluminum support and additional HV test of to check all sectors are OK once again
- Currently on cosmic stand

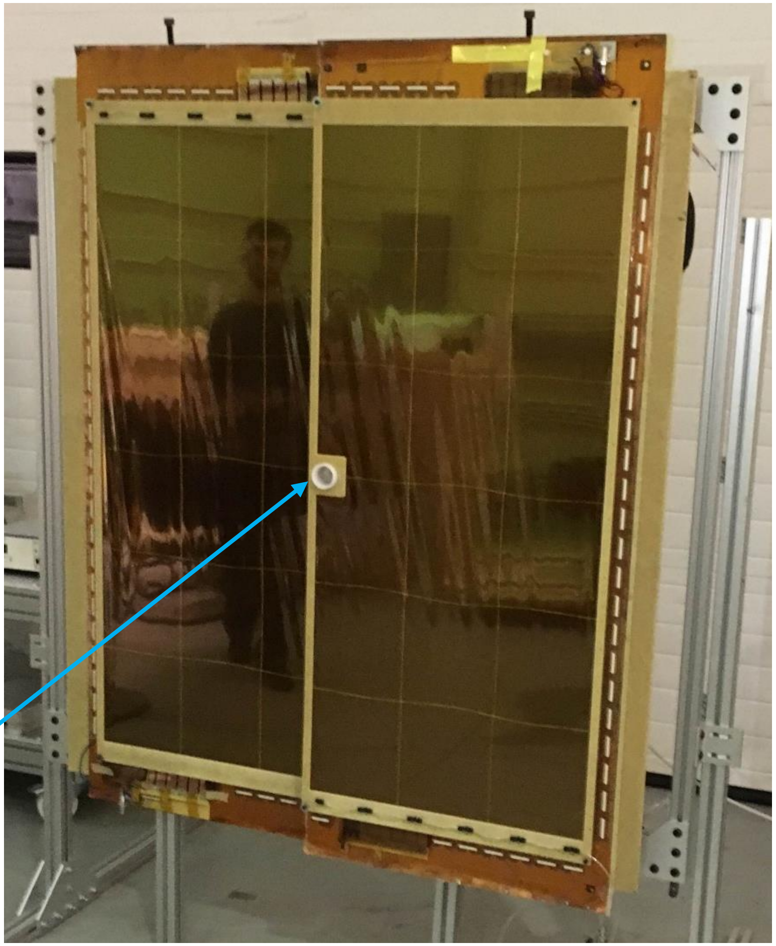
GEMs on HyCal support structure



Beam pipe structure



Mounted on their Aluminum support frames



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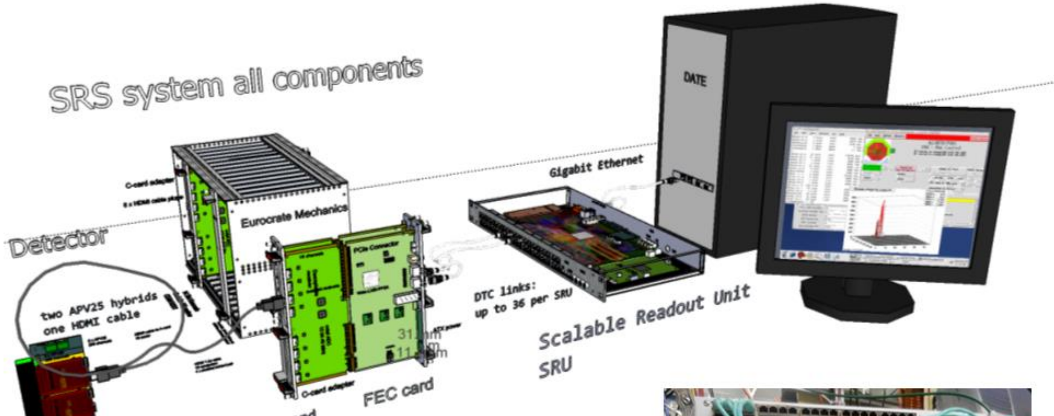
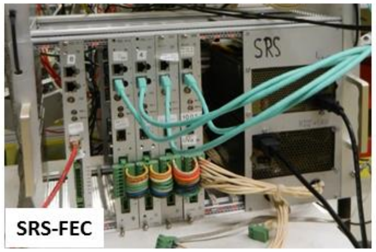
Upgrade of SRS Electronics: The Scalable Readout System

Multichannel electronics developed by the RD51 Collaboration for Micro Pattern Gaseous Detectors such as GEMs. It is based on:

- SRS-APV25: Front End cards (hybrids hosting the APV25 chip) mounted on the detector ⇨ send multiplexed data from128 channels to SRS-ADC cards via standard commercial HDMI cables.
- SRS-ADC: card that host the ADC chips, de-multiplex and convert data from up to 16 SRS-APV25 cards into digital format then send them to the SRS-FEC cards
- SRS-FEC: is the FPGA board, handles the clock and trigger synchronization of the SRS-APV hybrid cards, send digitized data from ADC to the SRS-SRU via 1 Gb Ethernet Copper link.
- SRS-SRU: handles communication between multiple (up to 40) SRS-FEC cards and the DAQ computer. It also distributes the clock and trigger synchronization to the SRS-FEC cards and send the data fragment to the DAQ PC through Gb Ethernet.





Need for the PRad GEMs:

- Hardware:
  - 72 SRS-APV FE cards (36 per GEMs)
  - 8 SRS-ADC / SRS-FECs with 9 APVs cards, 3 time samples
  - 2 SRS-SRU (4 ADC/FEC per SRU) collected the data to the DAQ PC through 10 Gb link
  - TIpcie: Interface the SRS electronics into JLab DAQ (CODA)
- Upgrade of the FEC and SRU firmware

Upgrade of SRS Electronics: Challenges @ 5kHz trigger rate

- Data from APV25 data to FEC cards:
  - 3 time samples: readout mode is about 100 kHz (10 μs), no problem for PRad GEMs readout
- Data from FEC to SRU:
  - 1Gb Ethernet cable (125 MB/s), data transfered through UDP
  - Rate capability 80 MB/s: 800 Mbps line speed × 80% (for 8b10b line encoding overhead).
  - 3 time samples mode: the APV25 data size per event is ~ 1 kB ⇨ transfer rate @ 5 kHz = 5 MB/s
  - Fixed trigger rate: the data transfer is ~ 60 MB/s with 12 APV25/ FECs (45 MB/s for with 9 APV25)
  - ✓ Firmware upgrade(done) for random trigger rate: Implementation of trigger buffering
- Data from SRU – DAQ PC:
  - Default SRU implementation: 1 G Ethernet cable (125 MB/s), data transfered through UDP
  - First bottleneck to address: SRU data from 36 APV25 ⇨ minimal transfer rate @ 5 kHz = 180 MB/s
  - ✓ Firmware upgrade (done): Implementation of 10 Gb optical link to the DAQ PC
- Data from DAQ PC to the disk: Writing APV25 data into disk @ 5kHz is a challenge (~ 360 MB/s)
  - Writing APV25 data into disk @ 5kHz is a challenge (~ 360 MB/s)
  - Online zero suppression in Event Builder on the DAQ PC ⇨ Event size to be reduced by ~ more tham100
  - Currently under development

Upgrade of SRS Electronics: 10 GbE link implementation (SRU firmware)

(B. Moffit, JLab DAQ group - B. Raydo, JLab Fast Electronics Group)

Existing SRU firmware from RD51 CERN

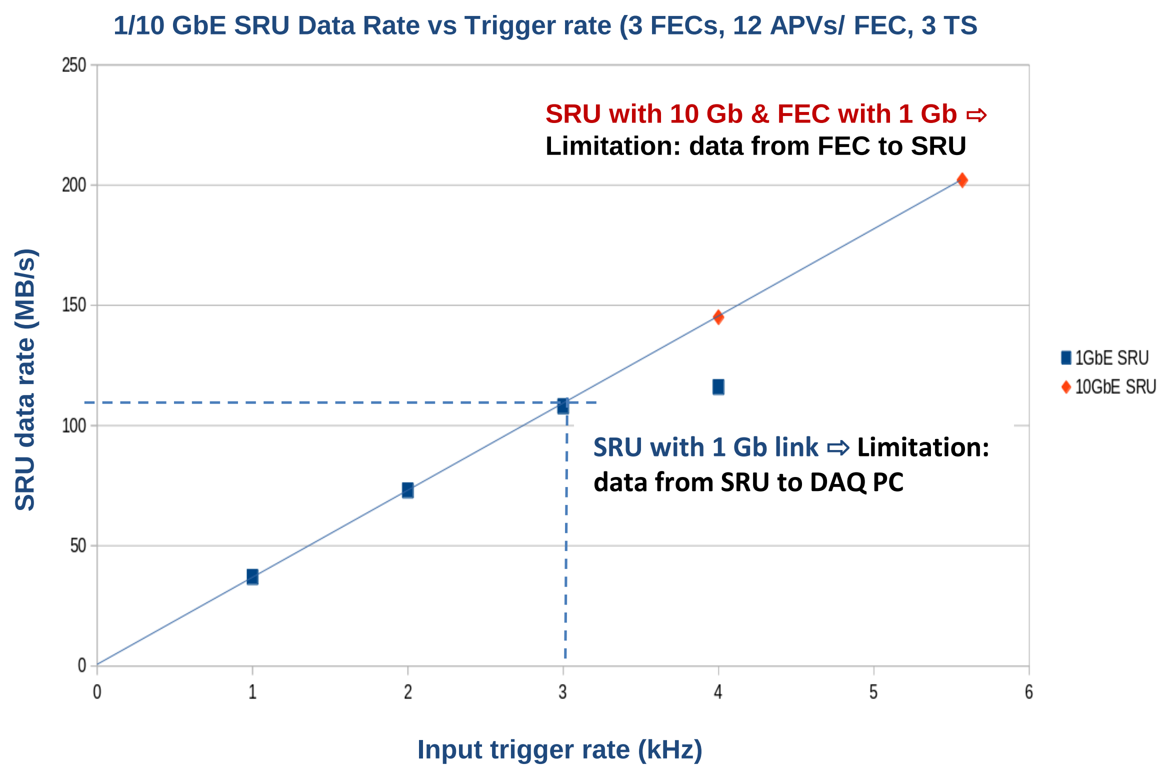
- Standard SRU firmware developped for the APV25 electronics with 1 Gb Ethernet link
- 10 Gb Optical link firmware previously developped at CERN for a different electronic was available but was not compatible with standard SRU firmware with APV25 readout

Upgrade of APV25-compatible 10 Gb SRU firmware (Ben Raydo)

- Merging the two firmware and testing with the APV25 electronics

Test Setup

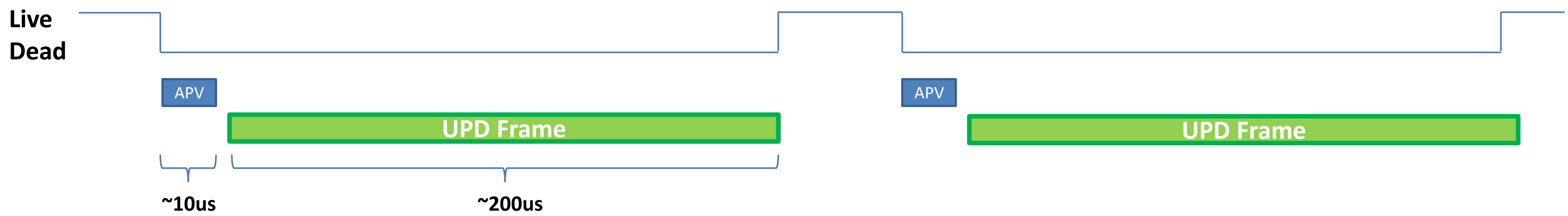
- 32 SRS-APV25 hybrids, connected to 3 FECs (event size 38.5 kB), calibration pulse with internal trigger @ 3 time samples (3TS)
- Rate tests with 1 Gb Copper link and upgraded 10 Gb Optical fiber link
- 1 Gb SRU: Saturation at ~3.2 kHz (max expected rate before saturation ~ 3.3 kHz)
- 10 Gb SRU: linear data transfet speed up to 5.5 kHz ⇨ saturation expected beyond 6 kHz (FEC data to SRU @ 80 MB/s)



Upgrade of SRS Electronics: Trigger Buffering (FEC firmware)

(B. Moffit, JLab DAQ group - B. Raydo, JLab Fast Electronics Group)

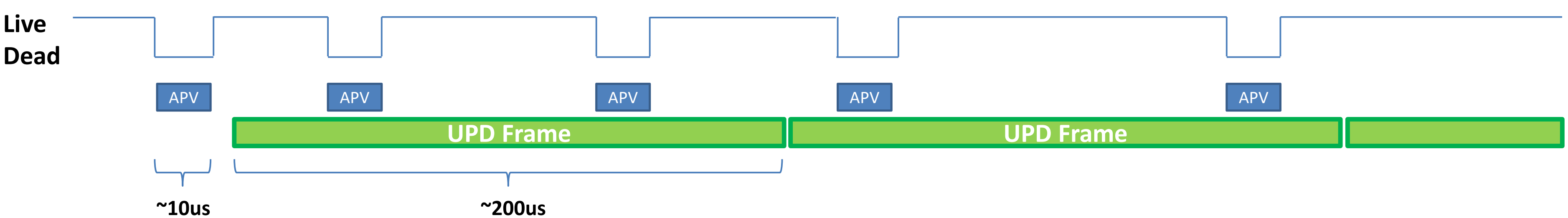
Non-buffered trigger FEC firmware (original):



- Dead/busy while APV sends triggered data **and dead/busy while UDP packets are sent**
- For fixed trigger rate, the dead time is basically determined by the UDP data processing (~200 μs)
- For random trigger: the mechanism is inefficient

  ⇨ no use of live time with low trigger burst but high trigger burst mean data loss because of dead time

Buffered trigger FEC firmware (new):



- **UDP processing of APV data is “de-coupled” from APV sending data**
- Dead/busy while APV sends triggered data, **no longer dead/busy while UDP packets are sent**
- When buffers, holding captured APV for UDP processing in FPGA become full, the FEC create necessary dead/busy time.
- For random trigger, @ high trigger burst, APV data are stocked in buffer and UDP packet is formed during the low trigger burst
- Dead/busy time while APV sends data can be eliminated to improve live time, but requires significant changes to FEC firmware.

Upgrade of SRS Electronics: Source code changes

(B. Moffit, JLab DAQ group - B. Raydo, JLab Fast Electronics Group)

APV25 chip has a 4096 deep sample buffer. When capturing a few time samples (e.g. 3), only a small fraction of the buffer is used. The new firmware makes use of the available buffer to optimize the rate capability of the system

Old firmware (standard from CERN)

- The firmware performs the following steps sequentially:
  1. receive a trigger and capture the APV25 data
  2. wait for the data to be fully processed by the UDP processor
  3. Then is ready to accept another trigger.

New firmware (upgrade @ JLab)

- circularly writes multiple events along with trigger header information in the existing buffer.
- A new FIFO is added to provide a pointer into the circular buffer to the UPD packet processor.
- The new firmware performs the following steps in parallel:
  1. Receive a trigger, capture APV25 data and is ready to accept another trigger [~ 25 μs]
  2. Check trigger FIFO and build UPD packets independently from step #1 [~ 200 μs]
  3. Check circular buffer and assert BUSY if no more events can be accepted.
- Trigger processing dead time ~ 25 microseconds with up to 10 triggers can be buffered
- BUSY output (NIM Out): Busy Feedback to Trigger Supervisor ⇨ allows for more efficient trigger acceptance without assumptions of FEC processing dead time.
- As a test example, without buffering, we needed up to 70kHz input rate to readout near 5kHz ⇨ dead-time close to 100%. With buffering enabled the input rate could be slightly over 5kHz to readout near 5kHz ⇨ dead-time just a few percent.

Upgrade of SRS Electronics: Tests of trigger buffering

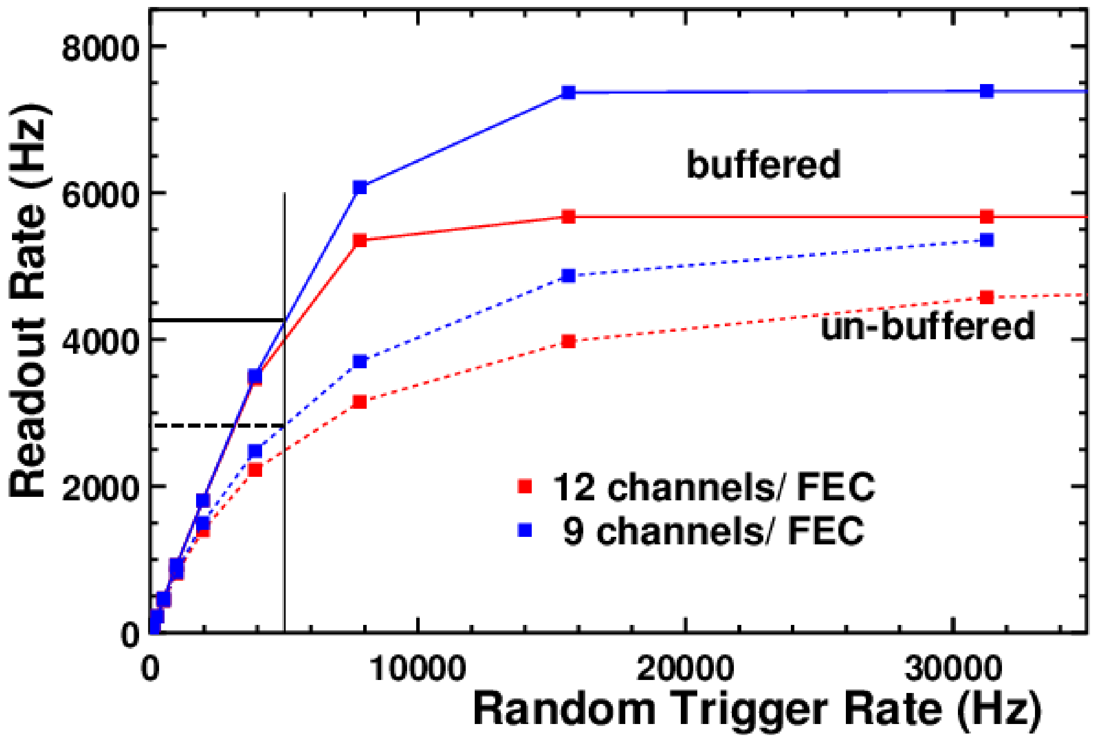
(B. Moffit, JLab DAQ group - B. Raydo, JLab Fast Electronics Group)

Preliminary tests

- 9 / 12 APV25 (ADC channels), on 1 FEC with 3 time samples to the SRU (Expected configuration for PRad)
- Random pulse generator board with both buffered and un-buffered Trigger tested simultaneously
- Additional tests was done with multiple FECs ⇨ for debbugging and troubleshooting
- Cosmic data test setup with the GEM chambers is underway to test the full DAQ with all the changes

Validation @ 5 kHz random trigger rate

- Un-buffered triggers firmware: readout rate of ~2.8 kHz (9 APVs on FEC) ⇨ 44% dead time
- Buffered trigger firmware: readout rate of ~4.25 kHz (9 APVs on FEC) ⇨ 15% dead time, OK for Prad



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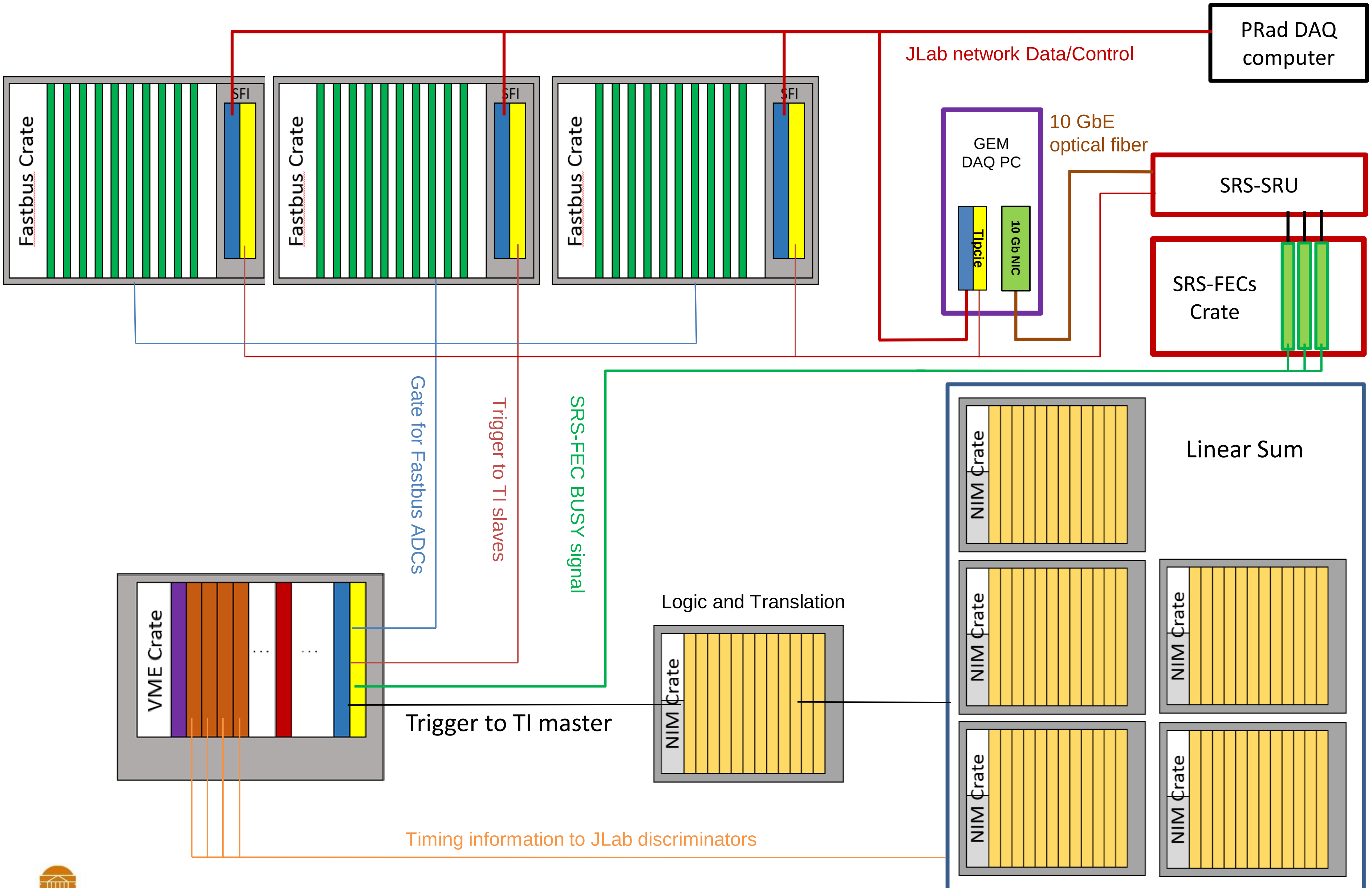
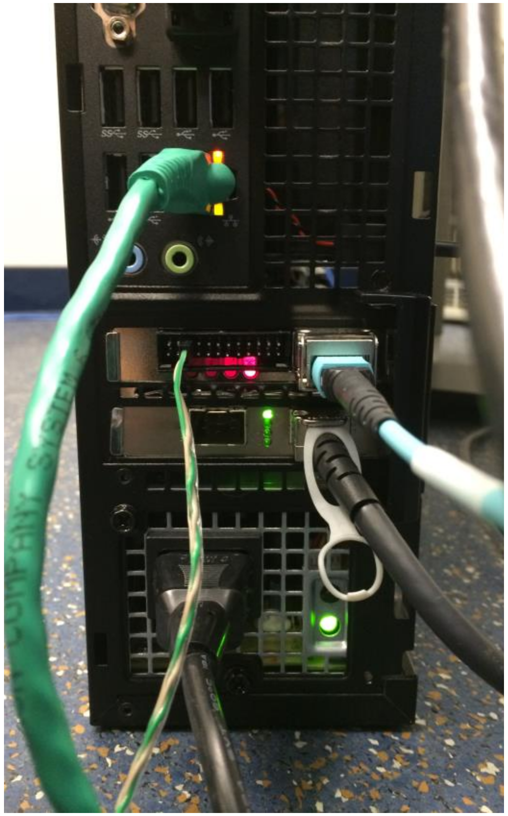
Integration of SRS into JLab DAQ: PRad DAQ Overview



Integration of SRS into JLab DAQ: Hardware

(B. Moffit, JLab DAQ group - B. Raydo, JLab Fast Electronics Group)

- PCIexpress Trigger Interface (TIpcie)
  - Integrate standard desktop or Server PC with PCIe bus into JLab Pipeline DAQ (CODA)
  - Optimal for the use of multiple cores / threads for data processing and data reduction required for PRad GEMs data
  - Standard PC Hardware allows for multiple network cards (1G, 10G, Infiniband)
  - Runs in Standalone (Master) or Larger-Scale DAQ (Slave).
  - Kernel and userspace driver compatible with EL5, EL6 (i386, x86_64)
- Interface to the SRS
  - SRU receive the trigger from the Trigger Supervisor and send BUSY.
  - TIpcie collects data from the SRU send to PRad DAQ PC via JLab Network



- Setup of the high rate (5kHz) test with the TIpcie
- The back side of the DAQ PC shows:
  - PCIe TI with the blue fiber connection to the TS
  - The twisted pair connections for triggers.
  - The 10 Gb card for data transfer with the links connected (black) to the SRU.

Integration of SRS into JLab DAQ: Software development

(B. Moffit, JLab DAQ group - B. Raydo, JLab Fast Electronics Group)

Software librairies for the slow control (B. Moffit)

- C Library written to be used with CODA, **but also works standalone**
- Compatibility: REDHAT EL5, EL6 (i386, x86_64)
- Uses calls to routines for the configuration and readout
  - instead of using system calls to external programs/scripts
  - Still has the capability of reading in the original configuration text files.
  - More ‘human’ readable, Parameters can be input in any base (hexadecimal, decimal)
- Allows for iterating over several FEC with similar configuration

✓ Done and under test with the cosmic test run

Online monitoring (Xinzhan and Weizhi)

- Before zero suppression (not implemented at the firmware level)
  - Raw APV25 data frames are available for online monitoring during the life time of PRad run and during initalisation of all APV25 after DAQ reboot

  ✓ Done and under test with the cosmic test run
- Zero suppression at software level by CODA Event Builder in the DAQ PC
  - Monitoring of hits and clusterization algorithm for real time characterisation of the GEMs, Hits and cluster data will be passed to the CODA Event Recorder to be written into disk

  ✓ Under development

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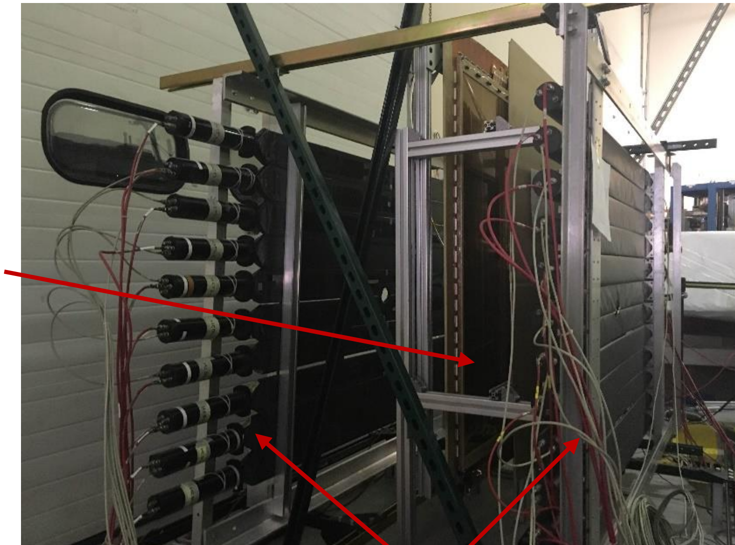
Cosmic Tests: setup in EEL building

(Xinzhan and Weizhi)

- 2 PrimEx Scintillators layers used for cosmic trigger
- 1 SRU / SRS crate, 4 FECs, 36 APVs (half of the PRad GEM requirement)
- ✓ full PRad GEM DAQ with real data and decoder/monitoring software
- Lots of troubleshooting these past few weeks

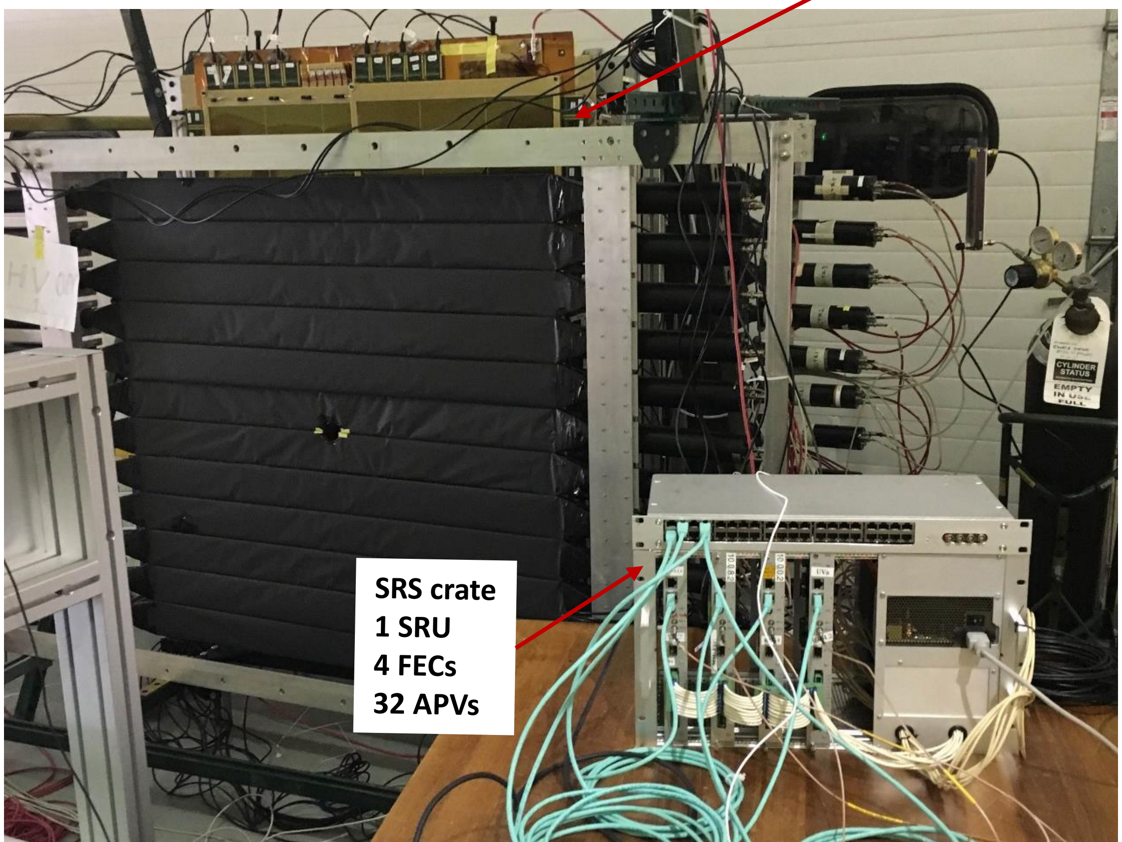
Side view



PRad GEMs

Scintillators planes for cosmic trigger

Front view

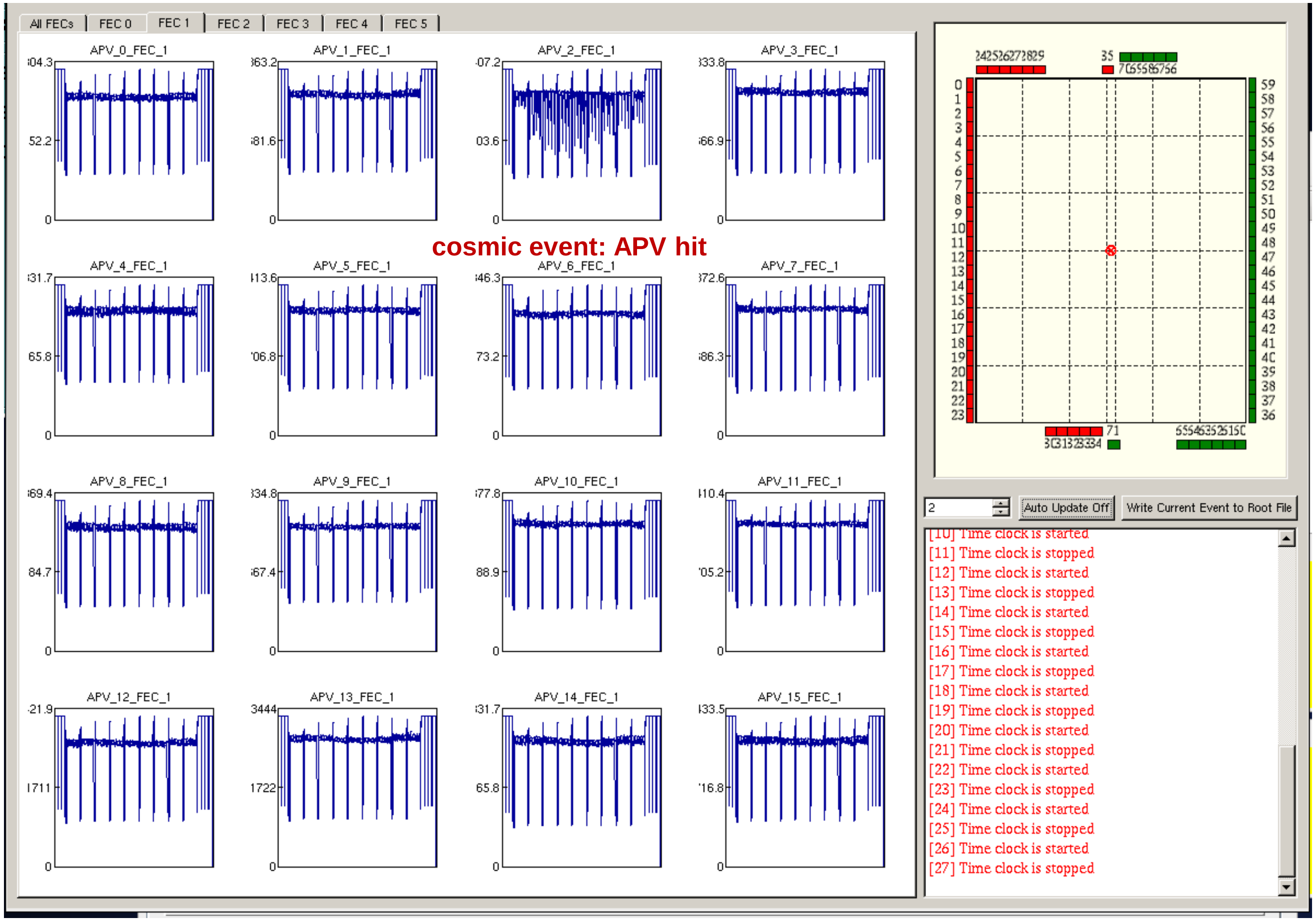


Cosmic Tests: Preliminary data

(Xinzhan and Weizhi)

- ✓ At last we are seeing cosmic data signal with the chambers
- Ongoing tuning of trigger signal and APV25 data latency for optimization of the setting
- Plan to monitor the stability of the DAQ in the cosmic setup for a few days
- Will after move to the full DAQ system to read out all two chambers and take data for several days for efficiency study

PRad GEMs Online Raw Data Event Display



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Summary

- Two large PRad GEM chambers built at Uva
  - Preliminary cosmic data test conducted at UVa to test basic performances
  - Delivered to JLab in Februrary and mounted on the support frames in the cosmic setup
- APV25-based SRS is the readout electronics for the Prad GEMs
  - Readout System is based on the SRS electronics developped by the RD51 coll. @ CERN
  - Challenge is to read out 9216 electronic channels (detector strips) @ 5 khz trigger rate
- Firmware upgrade to allow high rate capability
  - SRU firmware: implementation of 10 Gb optical link for the data transfer from the SRU to the DAQ PC
  - FEC firmware: Implementation of the buffering trigger ⇨ allow 5 kHz trigger rate with limited dead time
- Integration of the SRS into JLab DAQ system
  - JLab custom board TIpcie for the trigger interface between SRS and Prad DAQ system
  - Development of the TIpcie libraries and slow control routines, online monitoring software
- Cosmics setup of the GEM chambers with SRS readout / DAQ
  - First real data from the GEM with the full DAQ chain
  - Test of the DAQ / readout and preliminary study of the chamber detection efficiency
- Goals and plans or the coming weeks before the installation in Hall B
  - Implementation the zero suppression algorithm for online data reduction
  - More tests and checks of the performances of the DAQ and GEM chambers with cosmic setting

Back Up