

# DAQ Update

## Test of all ADC boards

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# Test crate setup

- A test crate is successfully built
  - It can load up to 10 1881M ADC boards
  - Trigger system is built based on the SFI and SFI AUX card at the back panel
  - A pulse generator is used as the trigger source
- Replay code is developed
  - It decodes the data file and store them channel by channel for each ADC board

# Test results

- 29 ADC boards in total
  - #1 ~ #30 except #21, which is 1877 TDC board
- Pedestal of all the boards are recorded
- Board #18 and #20 are found problematic

The screenshot displays the Run Control rcGui-48 interface. The top section shows control buttons and time fields (Start Time: 13:43:41, End Time: 07 August). The middle section contains Run Parameters (Expid: PRAD, Session: PRAD01, Configuration: ROC5) and Run Status (Run Number: 110, Run State: active, Total Events: 8952). Below this is a table of board data:

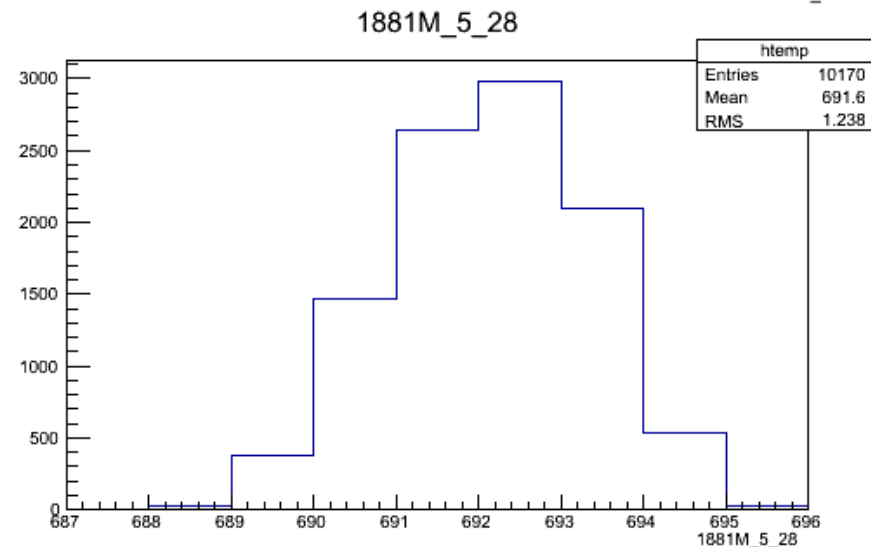
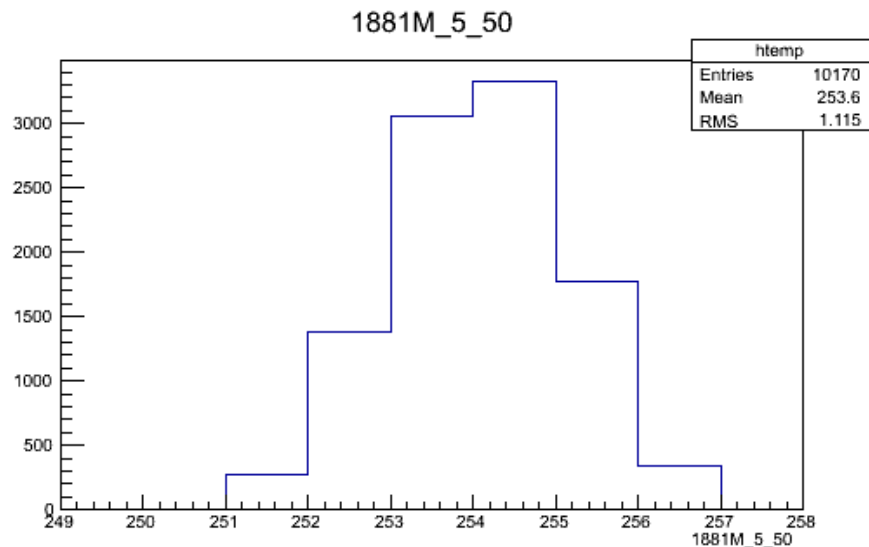
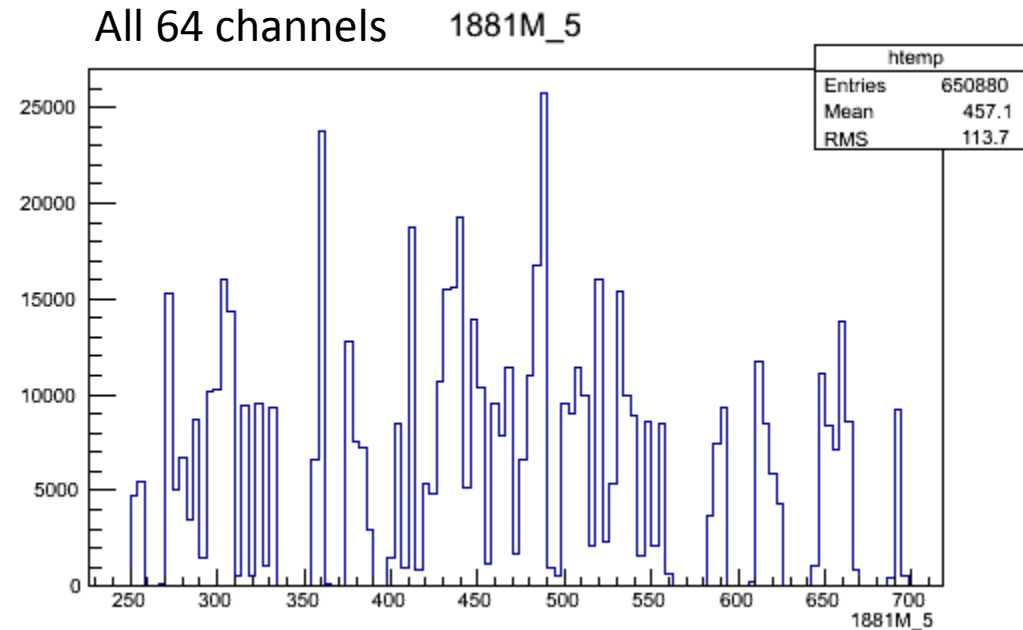
Name	State	EvtRate	DataRate	In-EvtRate	In-DataRate
ER3	active	25.0	66.6	29.3	77.9
EB3	active	32.5	85.7	29.4	77.6
primexroc5	active	29.5	85.7	29.6	77.9

To the right of the table is a graph showing the Event Rate for ER3 over time, with a y-axis from 0 to 60 and an x-axis from 13:48:20 to 13:48:40. The graph shows a sawtooth pattern. At the bottom, a log window displays a list of messages with columns for Name, Message, Time, and Severity.

Name	Message	Time	Severity
sms_ROC5	End is started.	13:41:30 08/07	Info
sms_ROC5	End succeeded.	13:41:56 08/07	Info
rcGui-48	Reset issued.	13:42:12 08/07	Info
sms_ROC5	reseted is started.	13:42:12 08/07	Info
rcGui-48	Configure is started.	13:42:58 08/07	Info
ControlDesigner	configure is started.	13:42:58 08/07	Info
sms_ROC5	Configure succeeded.	13:42:59 08/07	Info
sms_ROC5	Download is started.	13:43:03 08/07	Info
sms_ROC5	Waiting for primexroc5,	13:43:11 08/07	Warning
sms_ROC5	Waiting for primexroc5,	13:43:16 08/07	Warning
sms_ROC5	Waiting for primexroc5,	13:43:21 08/07	Warning
sms_ROC5	Download succeeded.	13:43:22 08/07	Info
sms_ROC5	Prestart is started.	13:43:28 08/07	Info
sms_ROC5	Prestart succeeded.	13:43:34 08/07	Info
sms_ROC5	Go is started.	13:43:37 08/07	Info
sms_ROC5	Go succeeded.	13:43:40 08/07	Info

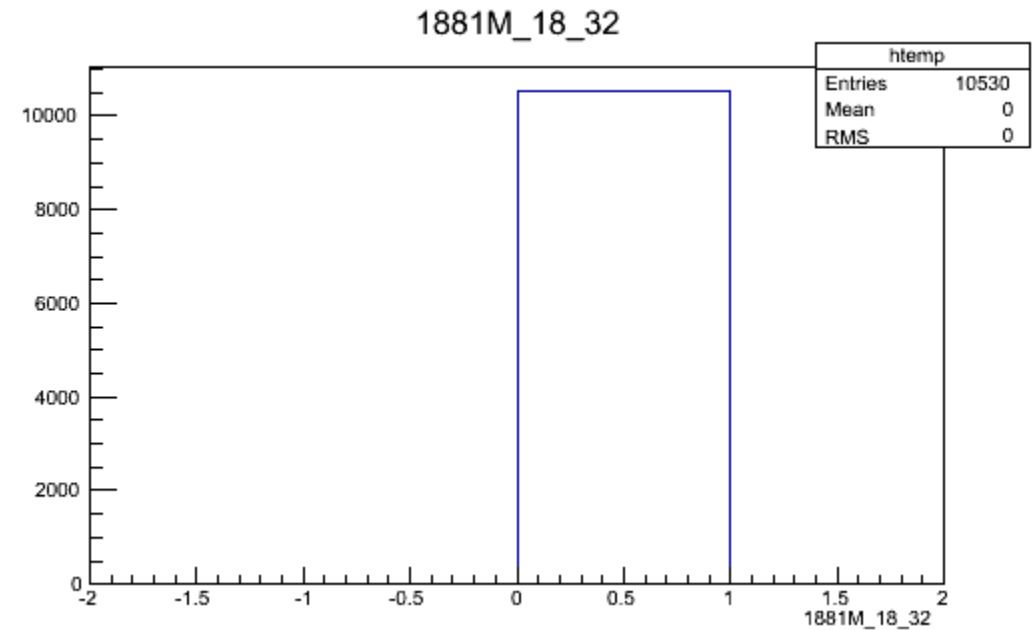
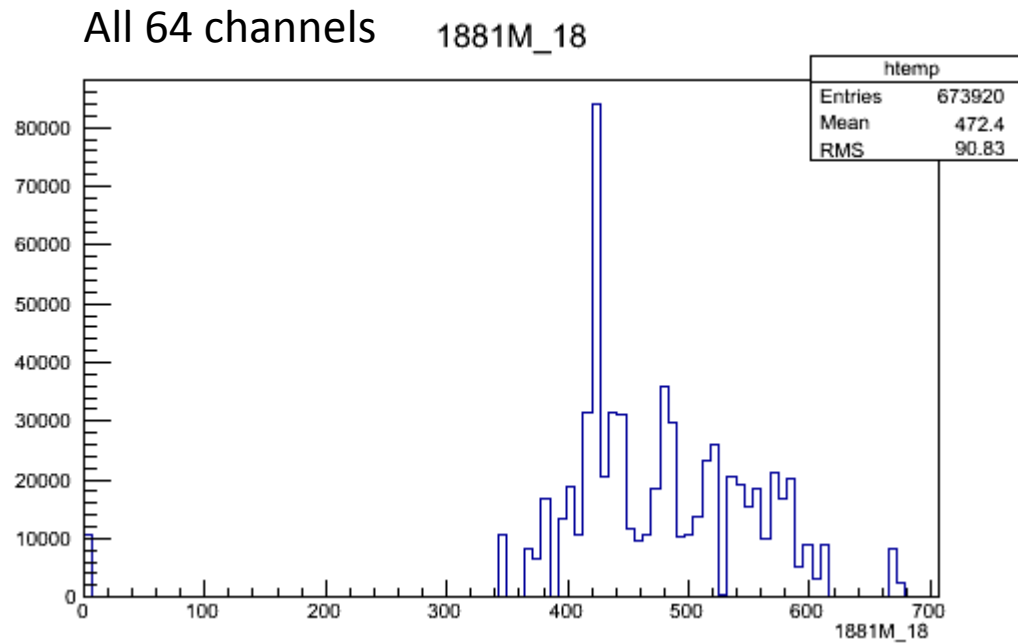
# Test Results

- Typical result, from #5
  - Horizontal axis: values in each channel (13 bit data, integer from 0 to 8191)
  - Vertical axis: Counts



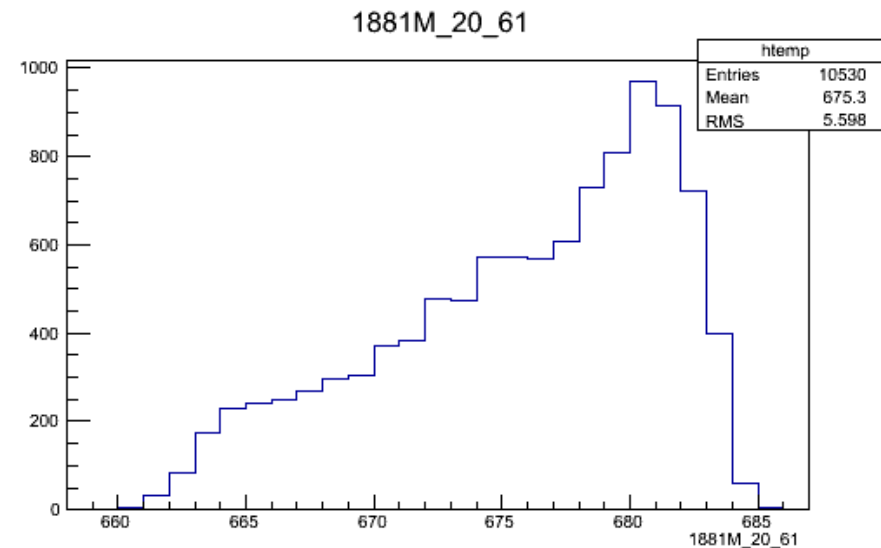
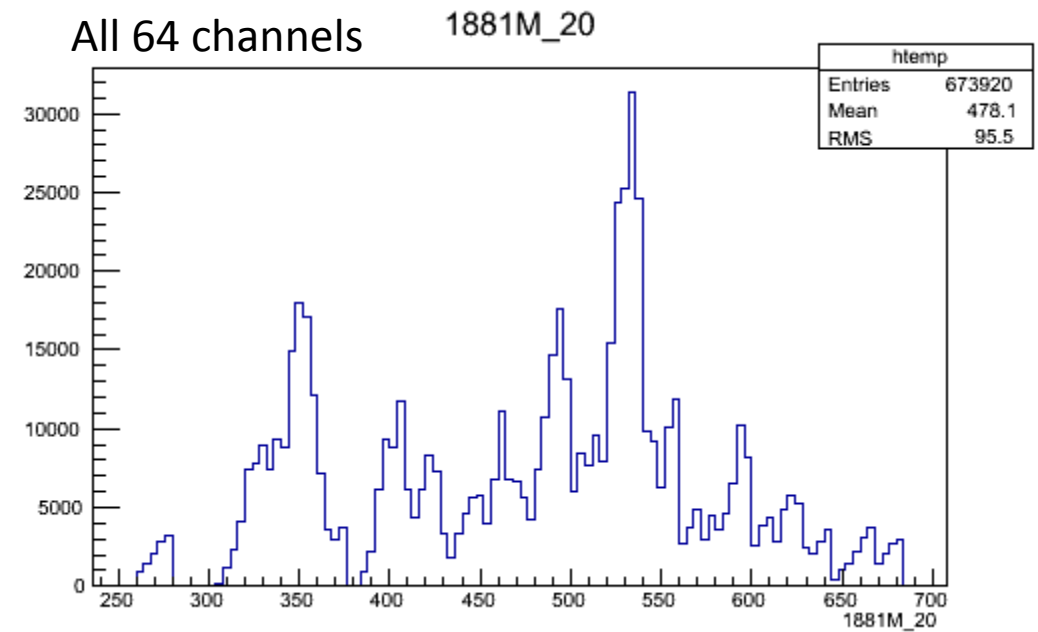
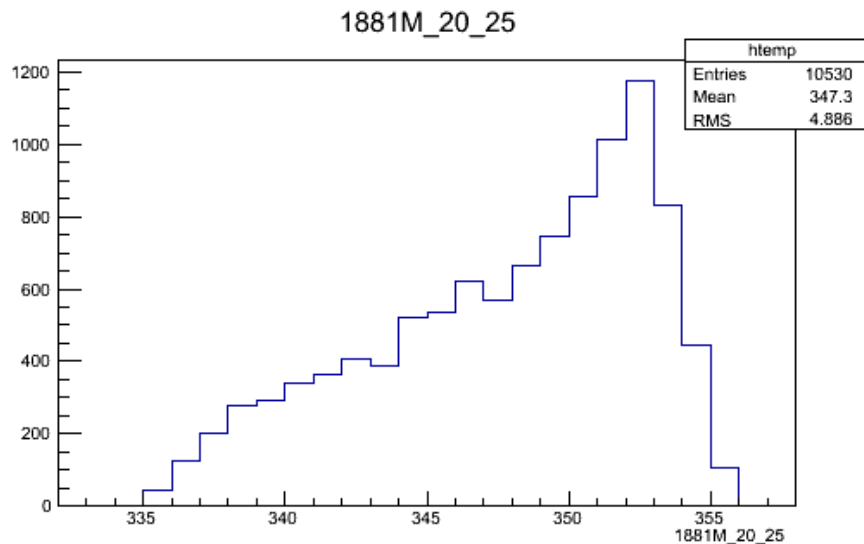
# Bad ADC board 18

- #18, channel 32 has no readout in 3 test runs in a row, others are normal



# Bad ADC board 20

- #20, channel 32 has no readout in first 2 test runs. It gets data in the 3<sup>rd</sup> test run.
- All channels have a very wide (>20) pedestal



# Summary and plan

- Summary

- Most of the boards work, the width of pedestal for each channel is about 10, the center varies from 200 to 800
- Board 18 has a bad channel, board 20 has a problematic channel and has a very wide pedestal
- It will be good to replace these two boards
- Detailed log for the test work is at <https://wiki.jlab.org/pcrewiki/index.php/Test>, the pedestal plots for all the boards and channels will be uploaded

- Plan

- Test the other two crates, test other SFIs and CPUs, this will be done in this weekend
- Get new Trigger Interface from Sergey, to use and test this new trigger electronics (it supports higher rates)