

Update on PRad GEMs, Readout Electronics & DAQ

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Outline

- ✓ PRad GEMs update
- ✓ Upgrade of SRS electronics
- ✓ Integration into JLab DAQ system
- ✓ Cosmic tests in EEL

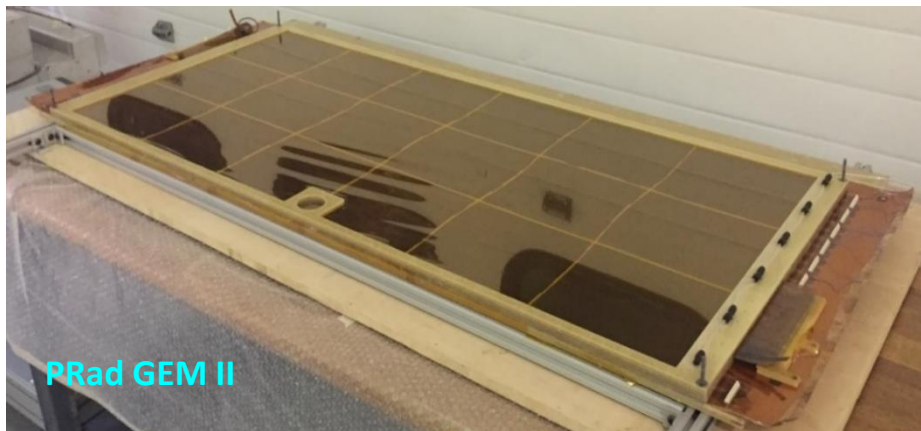
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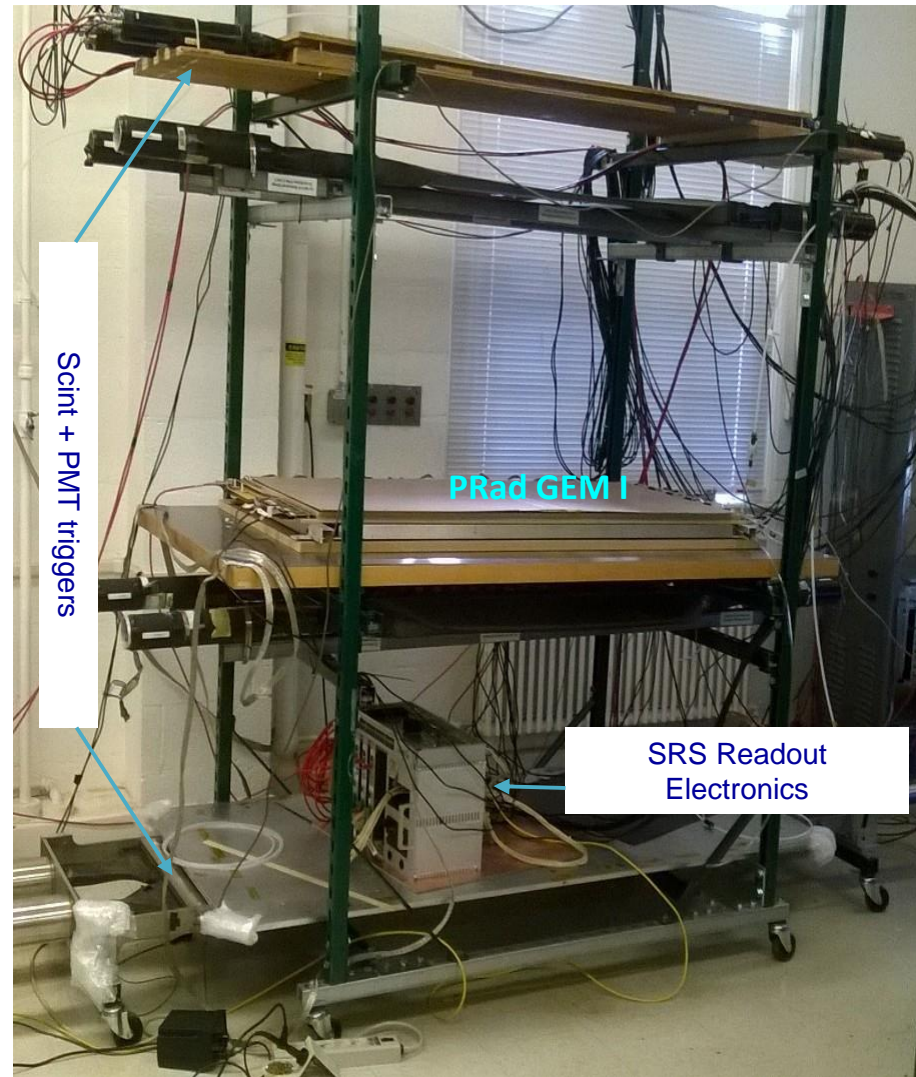
PRad GEMs Update: Assembly @ UVa



- Both chambers were completed in February
- Cosmic test performed on check all sectors active
- Basic characterization of the performances are evaluated

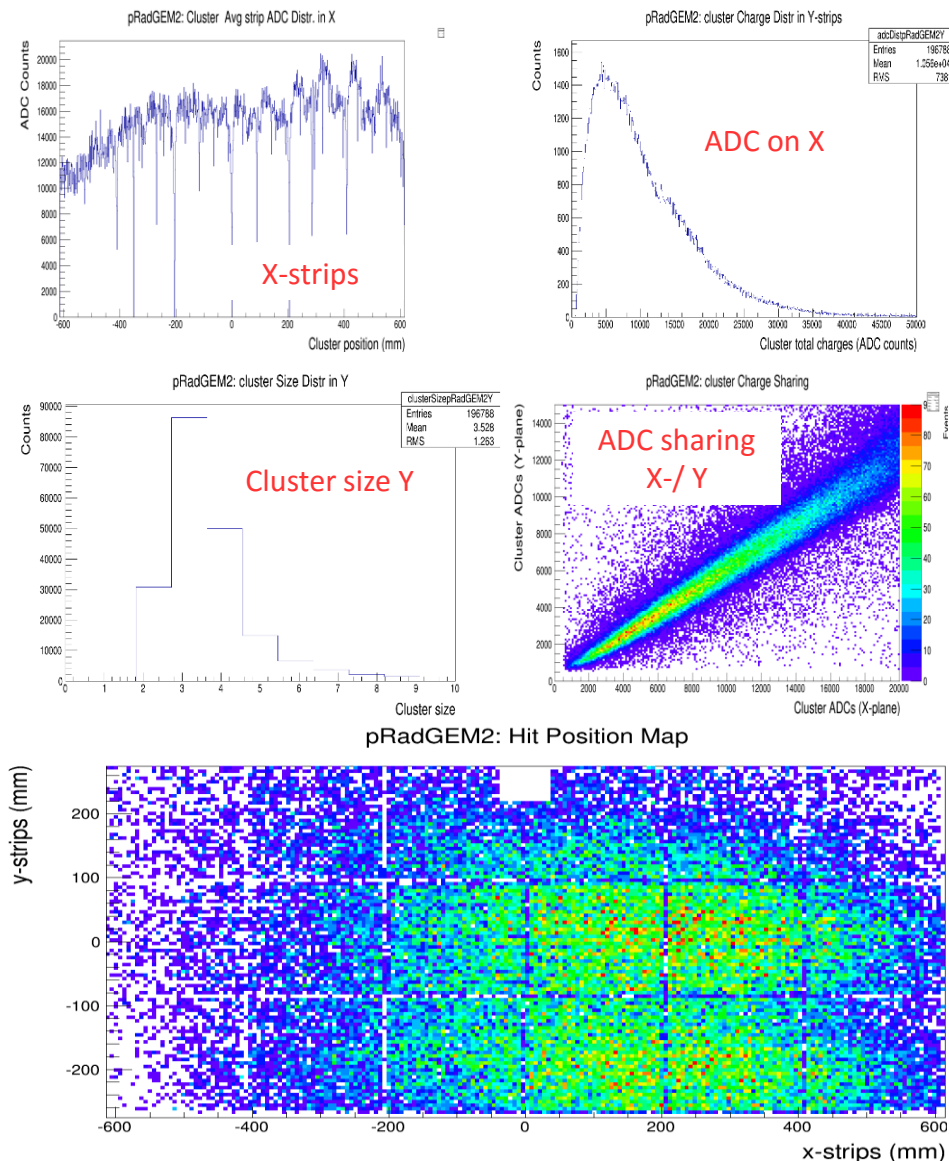


Cosmic stand in detector lab @ UVa



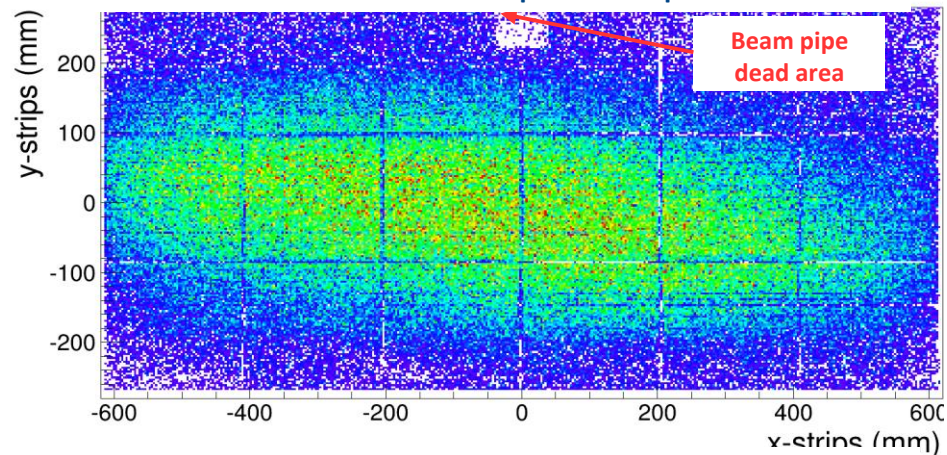
PRad GEMs Update: Results from Cosmic tests @ UVa

PRad GEM II

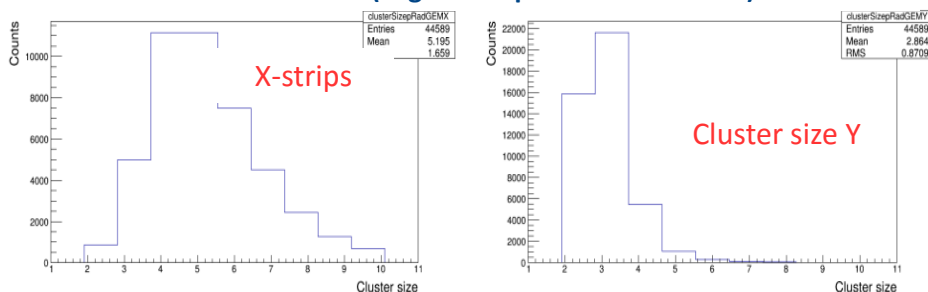


PRad GEM I

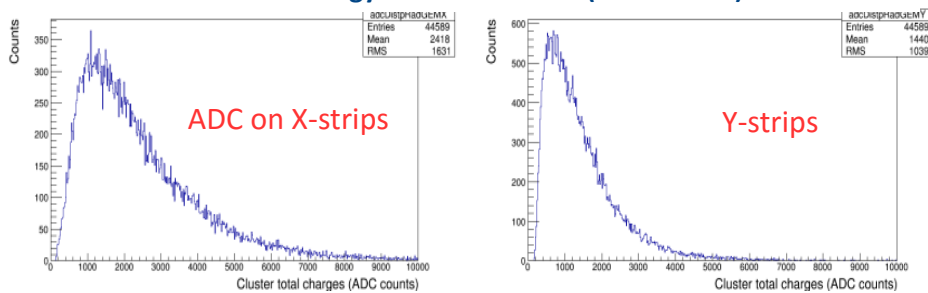
Cosmic hits cluster position map



Cluster size (avg. nb strips above threshold)

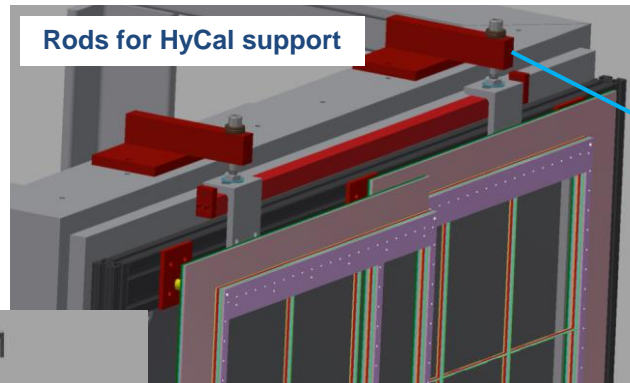


MIP energy loss distribution (ADC counts)

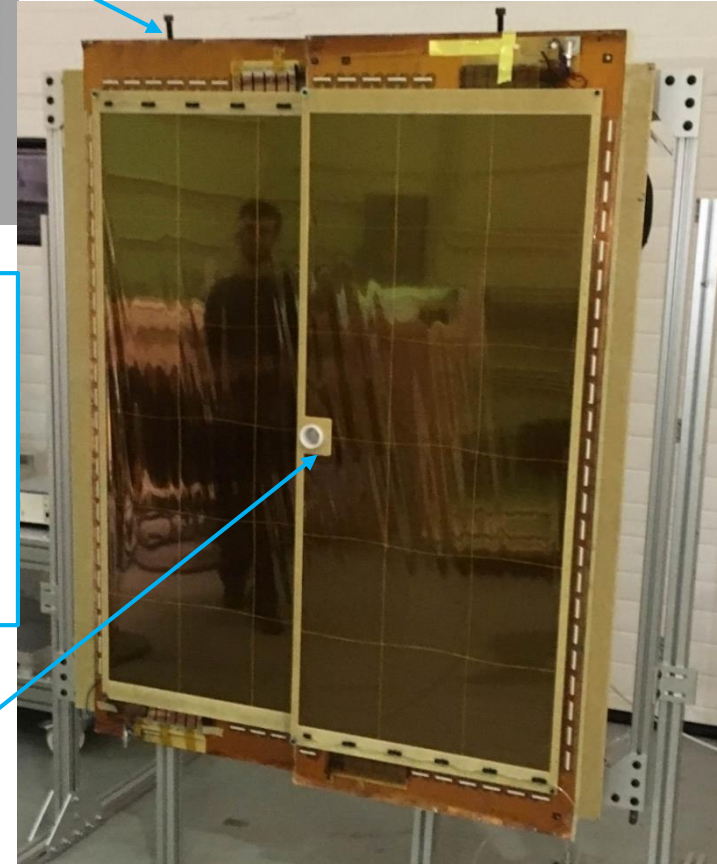


PRad GEMs Update: Both chambers @ JLab

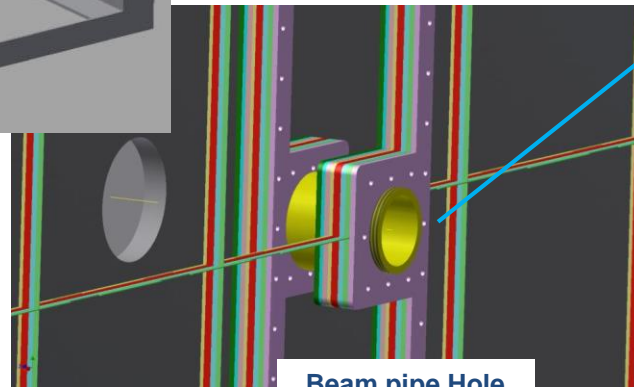
PRad GEM chambers will be mounted on HyCal support structure



Mounted on aluminum support frames



- Chambers are in room 125 in EEL building at JLab since Feb.
- Already mounted on the aluminum support frames
- All HV sectors checked once again after assembly
- Currently taking data on cosmic setup



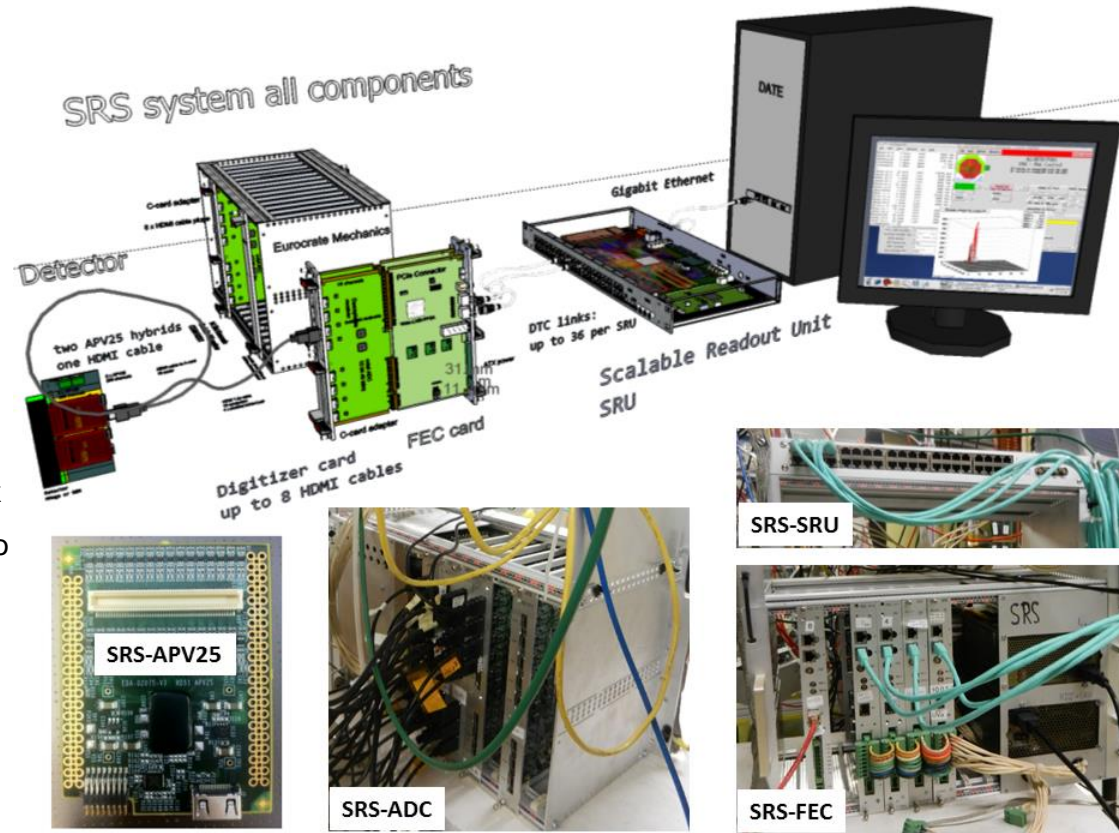
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Upgrade of SRS Electronics: The Scalable Readout System (SRS)

Multichannel electronics developed by the RD51 Collaboration for Micro Pattern Gaseous Detectors such as GEMs. It is based on:

- **SRS-APV25:** Front End cards (hybrids hosting the APV25 chip) mounted on the detector \Rightarrow send multiplexed data from 128 channels to SRS-ADC cards via standard commercial HDMI cables.
- **SRS-ADC:** card that host the ADC chips, de-multiplex and convert data from up to 16 SRS-APV25 cards into digital format then send them to the SRS-FEC cards
- **SRS-FEC:** is the FPGA board, handles the clock and trigger synchronization of the SRS-APV hybrid cards, send digitized data from ADC to the SRS-SRU via 1 Gb Ethernet Copper link.
- **SRS-SRU:** handles communication between multiple (up to 40) SRS-FEC cards and the DAQ computer. It also distributes the clock and trigger synchronization to the SRS-FEC cards and send the data fragment to the DAQ PC through Gb Ethernet.



Need for the PRad GEMs:

- **Hardware:**
 - 72 SRS-APV FE cards (36 per GEMs) \Rightarrow total of 9184 channels to read out
 - 8 SRS-ADC / SRS-FECs with 9 APVs cards, 3 time samples
 - 2 SRS-SRUs to collect the data from the FECs transfer to the DAQ PC
 - Tlpcie: Interface the SRS electronics into JLab DAQ (CODA)
- **Firmware upgrade**

Upgrade of SRS Electronics: Challenges @ 5kHz trigger rate

- Data from APV25 data to FEC cards:
 - 3 time samples: readout mode is about 100 kHz (10 μ s), no problem for PRad GEMs readout
- Data from FEC to SRU:
 - 1Gb Ethernet (125 MB/s), data transferred through UDP
 - Rate capability 80 MB/s: 800 Mbps line speed \times 80% (for 8b10b line encoding overhead).
 - 3 time samples mode: the APV25 data size per event is \sim 1 kB \Rightarrow transfer rate @ 5 kHz = 5 MB/s
 - Fixed trigger rate: the data transfer is \sim 60 MB/s with 12 APV25/ FECs (45 MB/s for with 9 APV25)
 - ✓ Firmware upgrade (done) for random trigger rate: Implementation of trigger buffering
- Data from SRU to GEM DAQ PC:
 - Default SRU implementation: 1Gb Ethernet (125 MB/s), data transferred through UDP
 - First bottleneck to address: SRU data from 36 APV25 \Rightarrow minimal transfer rate @ 5 kHz = 180 MB/s
 - ✓ Firmware upgrade (done): Implementation of 10 Gb optical link to the GEM DAQ PC
- Data from GEM DAQ PC to PRad DAQ PC:
 - Data are sent from GEM DAQ PC to the PRad DAQ computer via JLab network \Rightarrow GEM DAQ PC has the Tlpcie interface
 - Limited bandwidth to send the data to PRad DAQ PC and write them into disk (APV25 data size @ 5kHz = \sim 400 MB/s)
 - Zero suppression is done in GEM DAQ PC before the transfer of the data to PRad DAQ PC
 - APV25 data size is expected to be reduced by \sim more than a factor 100 to just a couple MB/s

Upgrade of SRS Electronics: 10 GbE link implementation (SRU firmware)

(B. Moffit, JLab DAQ group - B. Raydo, JLab Fast Electronics Group)

Existing SRU firmware from RD51 CERN

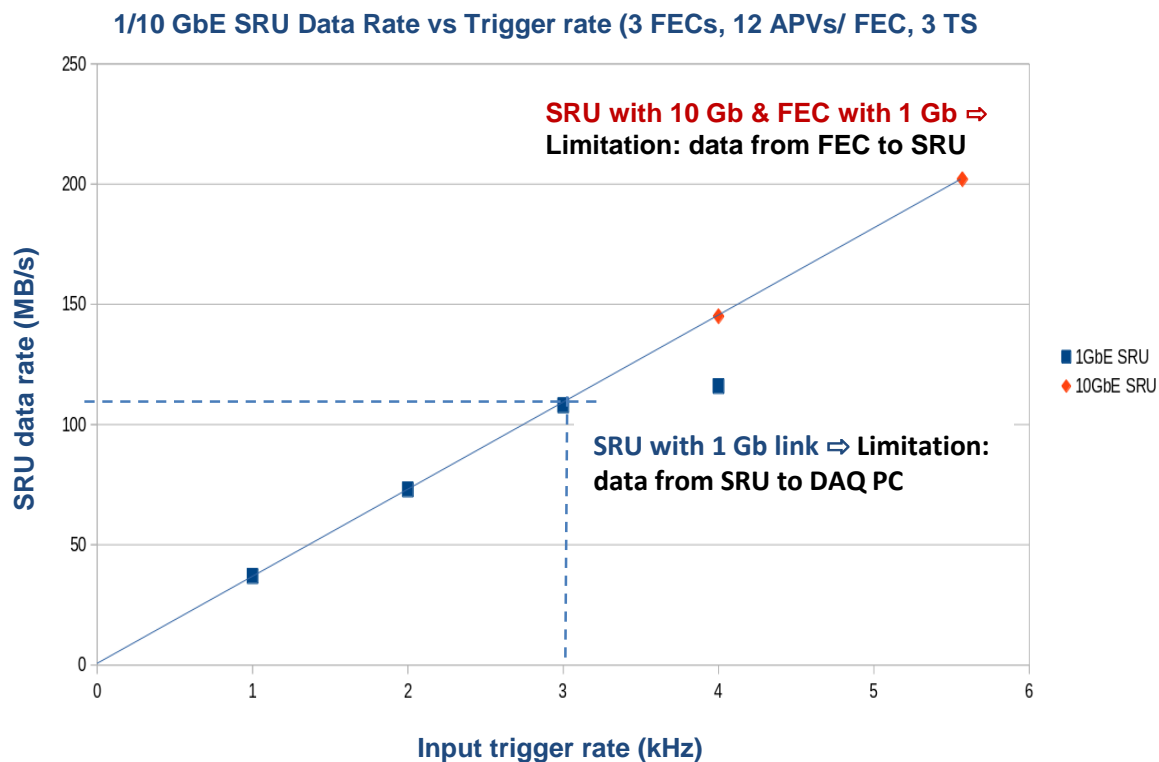
- Standard SRU firmware developed for the APV25 electronics with 1Gb Ethernet link
- 10 Gb Optical link firmware previously developed at CERN was available but not compatible with standard firmware

Upgrade of APV25-compatible 10 Gb SRU firmware (Ben Raydo)

- Merging the two firmware and testing with the APV25 electronics

Test Setup

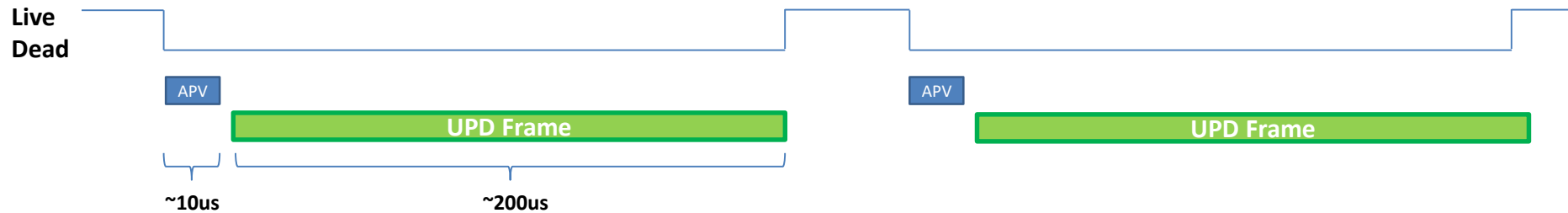
- 36 SRS-APV25 hybrids, connected to 3 FECs (event size 38.5 kB), calibration pulse with internal trigger @ 3 time samples (3TS)
- Rate tests with 1Gb Copper link and upgraded 10 Gb Optical fiber link
- 1Gb SRU: Saturation at ~3.2 kHz (max expected rate before saturation ~ 3.3 kHz)
- 10Gb SRU: linear data transfer speed up to 5.5 kHz \Rightarrow saturation expected beyond 6 kHz (FEC data to SRU @ 80 MB/s)



Upgrade of SRS Electronics: Trigger Buffering (FEC firmware)

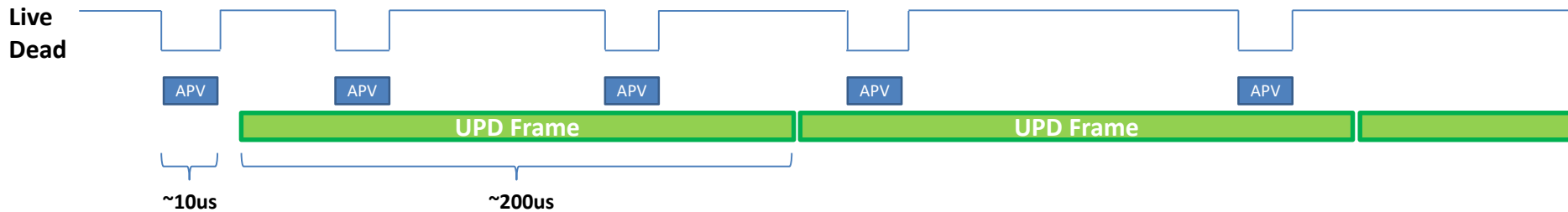
(B. Moffit, JLab DAQ group - B. Raydo, JLab Fast Electronics Group)

Non-buffered trigger FEC firmware (original):



- Dead/busy while APV sends triggered data **and dead/busy while UDP packets are sent**
- For fixed trigger rate, the dead time is basically determined by the UDP data processing ($\sim 200 \mu\text{s}$)
- For random trigger: the mechanism is inefficient
 - ⇒ no use of live time with low trigger burst but high trigger burst mean data loss because of dead time

Buffered trigger FEC firmware (new):



- **UDP processing of APV data is “de-coupled” from APV sending data**
- Dead/busy while APV sends triggered data, **no longer dead/busy while UDP packets are sent**
- When buffers, holding captured APV for UDP processing in FPGA become full, the FEC create necessary dead/busy time.
- For random trigger, @ high trigger burst, APV data are stocked in buffer and UDP packet is formed during the low trigger burst
- Dead/busy time while APV sends data can be eliminated to improve live time, but requires significant changes to FEC firmware.

Upgrade of SRS Electronics: Source code changes

(B. Moffit, JLab DAQ group - B. Raydo, JLab Fast Electronics Group)

APV25 chip has a 4096 deep sample buffer. When capturing a few time samples (e.g. 3), only a small fraction of the buffer is used. The new firmware makes use of the available buffer to optimize the rate capability of the system

Old firmware (standard from CERN)

- The firmware performs the following steps **sequentially**:
 1. receive a trigger and capture the APV25 data
 2. **wait** for the data to be fully processed by the UDP processor
 3. Then is ready to accept another trigger.

New firmware (upgrade @ JLab)

- circularly writes multiple events along with trigger header information in the existing buffer.
- A new FIFO is added to provide a pointer into the circular buffer to the UPD packet processor.
- The new firmware performs the following steps **in parallel**:
 1. Receive a trigger, capture APV25 data and is **ready to accept** another trigger [**~ 25 μ s**]
 2. Check trigger FIFO and build UPD packets independently from step #1 [**~ 200 μ s**]
 3. Check circular buffer and **assert BUSY** if no more events can be accepted.
- Trigger processing dead time ~ 25 microseconds with up to 10 triggers can be buffered
- **BUSY output (NIM Out)**: Busy Feedback to Trigger Supervisor \Rightarrow allows for more efficient trigger acceptance without assumptions of FEC processing dead time.
- As a test example, without buffering, we needed up to 70kHz input rate to readout near 5kHz \Rightarrow dead-time close to 100%. With buffering enabled the input rate could be slightly over 5kHz to readout near 5kHz \Rightarrow dead-time just a few percent.

Upgrade of SRS Electronics: Tests of trigger buffering

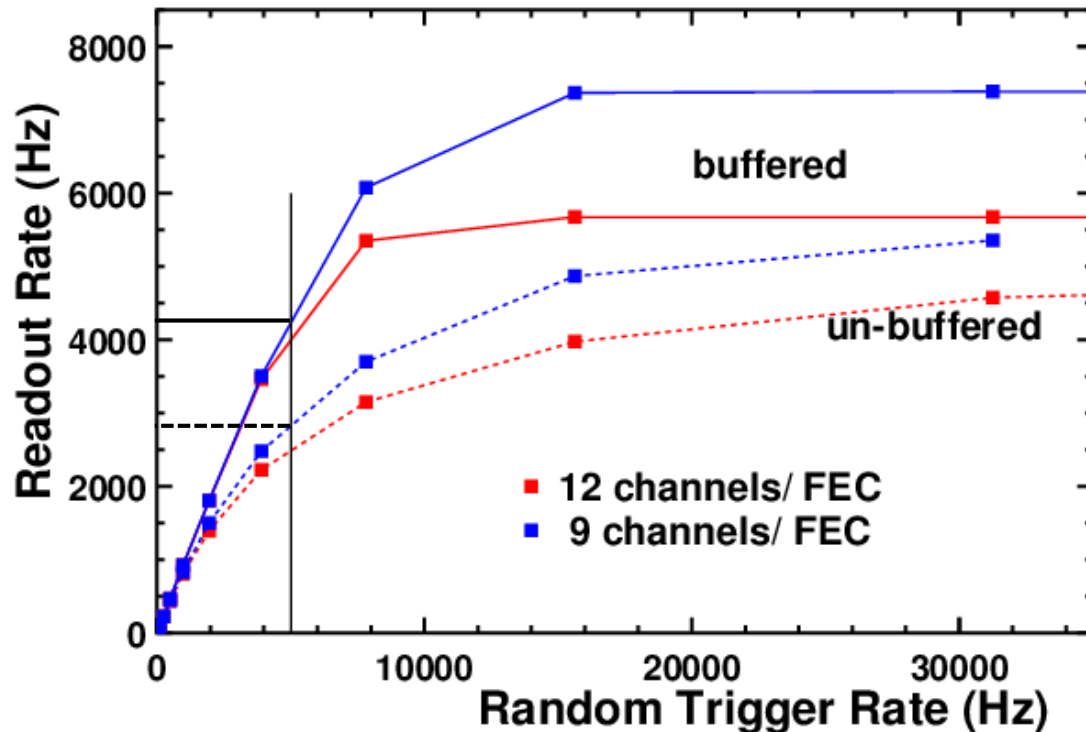
(B. Moffit, JLab DAQ group - B. Raydo, JLab Fast Electronics Group)

Preliminary tests

- 9 / 12 APV25 (ADC channels), on 1 FEC with 3 time samples to the SRU (Expected configuration for PRad)
- Random pulse generator board with both buffered and un-buffered Trigger tested simultaneously
- Additional tests was done with multiple FECs \Rightarrow for debbuging and troubleshooting
- Cosmic data test setup with the GEM chambers is underway to test the full DAQ with all the changes

Validation @ 5 kHz random trigger rate

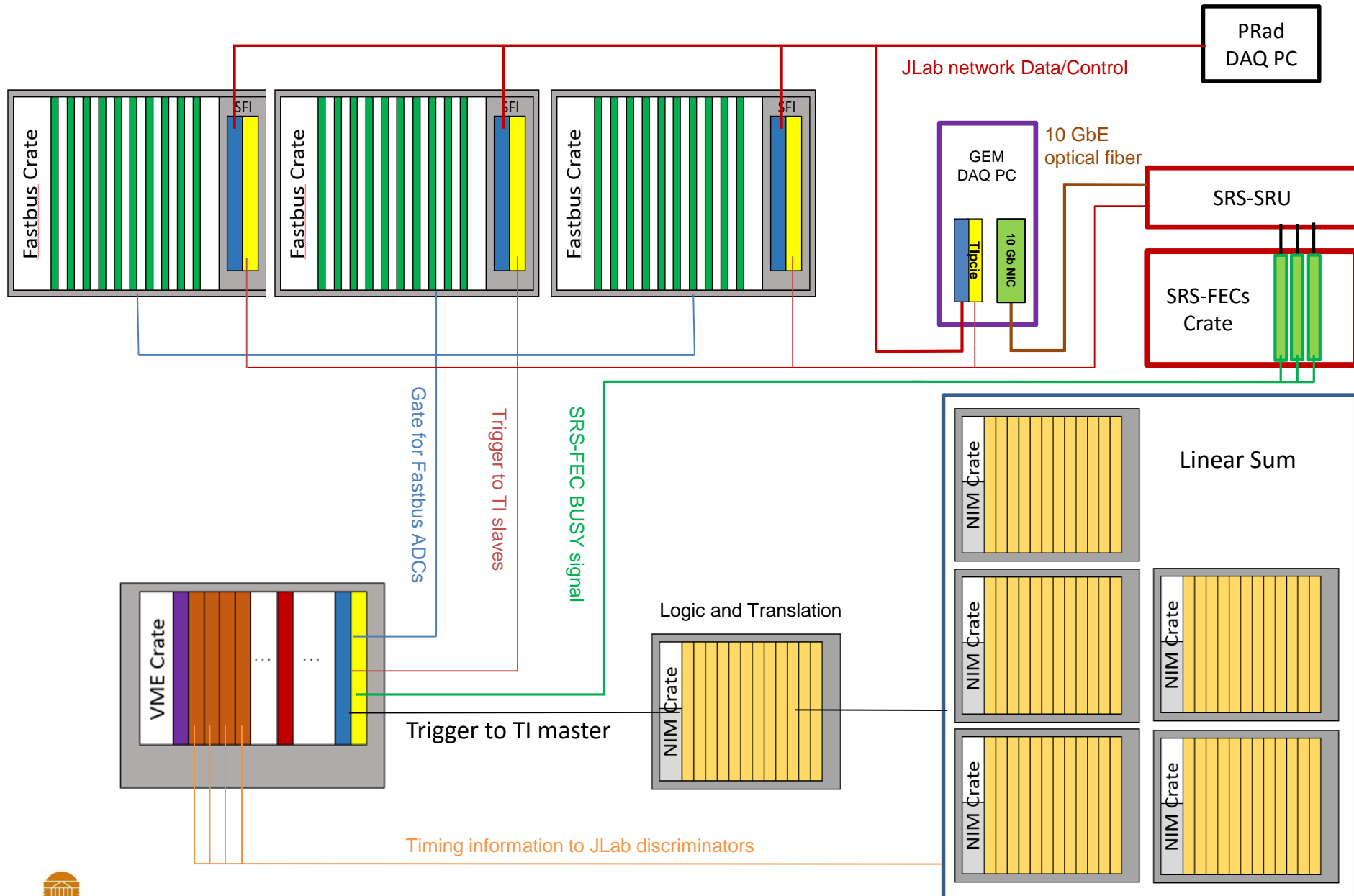
- Un-buffered triggers firmware: readout rate of ~ 2.8 kHz (9 APVs on FEC) \Rightarrow 44% dead time
- Buffered trigger firmware: readout rate of ~ 4.25 kHz (9 APVs on FEC) \Rightarrow 15% dead time, OK for Prad



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Integration of SRS into JLab DAQ: PRad DAQ Overview



Integration of SRS into JLab DAQ: Hardware

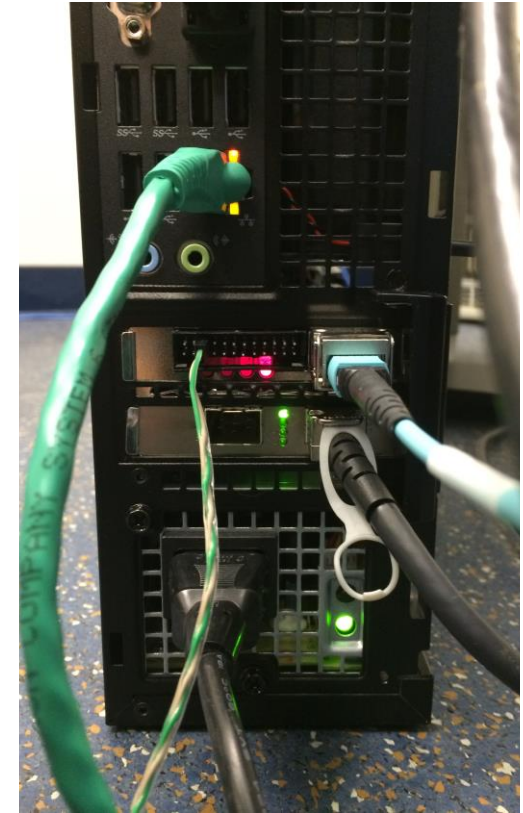
(B. Moffit, JLab DAQ group - B. Raydo, JLab Fast Electronics Group)

▪ PCIe Express Trigger Interface (Tlpcie)

- Integrate standard desktop or Server PC with PCIe bus into JLab Pipeline DAQ (CODA)
- Optimal for the use of multiple cores / threads for data processing and data reduction required for PRad GEMs data
- PC Hardware allows for multiple network cards (1G, 10G, Infiniband)
- Runs in Standalone (Master) or Larger-Scale DAQ (Slave).
- Kernel and userspace driver compatible with EL5, EL6 (i386, x86_64)

▪ Interface to the SRS

- SRU receive the trigger from the Trigger Supervisor and send BUSY.
- Tlpcie collects data from SRU send to PRad DAQ PC via JLab Network



- Setup of the high rate (5kHz) test with the Tlpcie
- The back side of the DAQ PC shows:
 - PCIe TI with the blue fiber connection to the TS
 - The twisted pair connections for triggers.
 - The 10 Gb card for data transfer with the links connected (black) to the SRU.

Integration of SRS into JLab DAQ: Software development

(B. Moffit, JLab DAQ group - B. Raydo, JLab Fast Electronics Group)

Software libraries for the slow control (B. Moffit)

- C Library written to be used with CODA, **but also works standalone**
 - Compatibility: REDHAT EL5, EL6 (i386, x86_64)
 - Uses calls to routines for the configuration and readout
 - instead of using system calls to external programs/scripts
 - Still has the capability of reading in the original configuration text files.
 - More 'human' readable, Parameters can be input in any base (hexadecimal, decimal)
 - Allows for iterating over several FEC with similar configuration
- ✓ Done and under test with the cosmic test run

Online monitoring (Xinzhan and Weizhi)

- Before zero suppression (not implemented at the firmware level)
 - Raw APV25 data frames are available for online monitoring during the life time of PRad run
 - During initialisation of all APV25 after DAQ reboot
- ✓ Done and under test with the cosmic test run
- Zero suppression at software level by CODA Event Builder in the DAQ PC
 - Monitoring of hits and clusterization algorithm for real time characterisation of the GEMs
 - Hits and cluster data will be passed to the CODA Event Recorder to be written into disk
- ✓ Under development

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Cosmic Tests: setup in EEL building

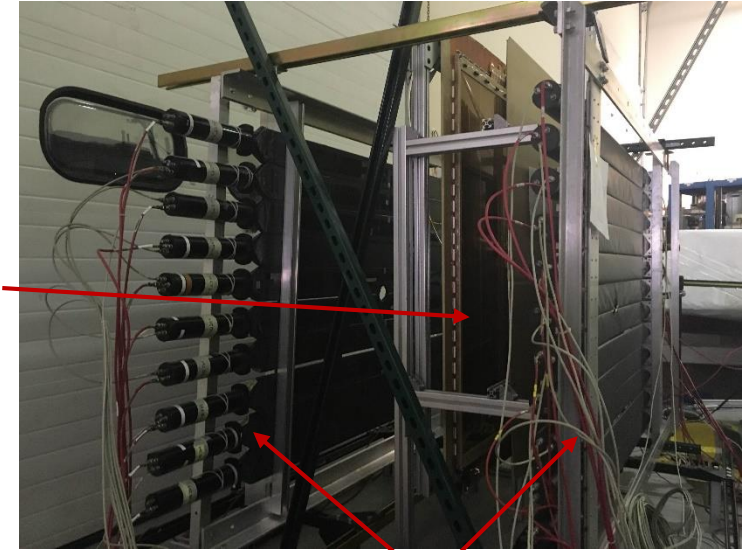
(Xinzhan and Weizhi)

- 2 PrimEx Scintillators layers used for cosmic trigger
- 1 SRU / SRS crate, 4 FECs, 36 APVs (half of the PRad GEM requirement)
- ✓ full PRad GEM DAQ with real data and decoder/monitoring software
- Lots of troubleshooting these past few weeks

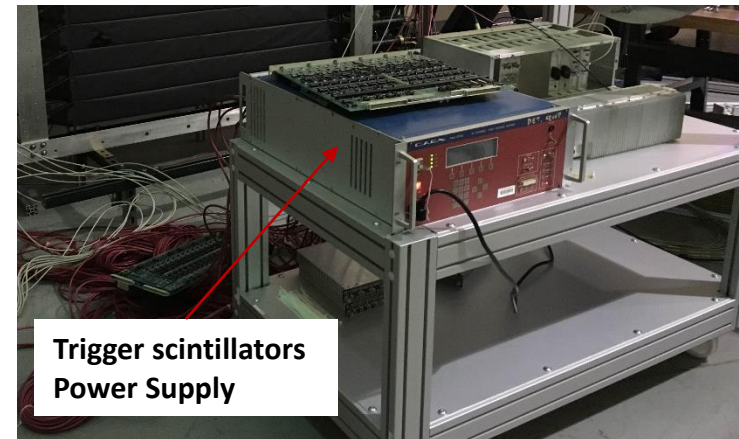
Front view

PRad GEMs

Side view



Scintillators planes for cosmic trigger



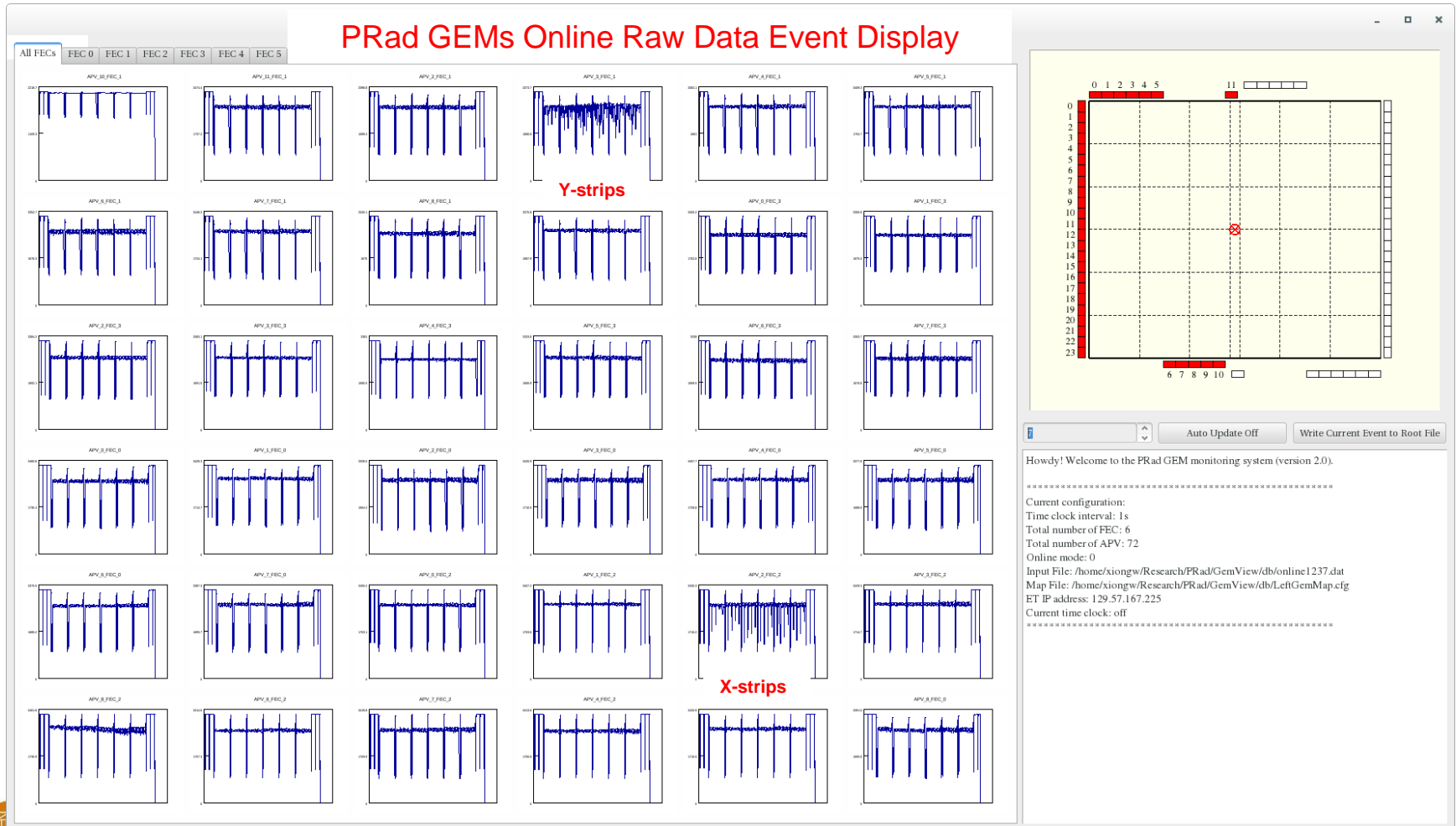
Trigger scintillators Power Supply

SRS crate
1 SRU
4 FECs
32 APVs

Cosmic Tests: Preliminary data

(Xinzhan and Weizhi)

- ✓ At last we are seeing cosmic data signal with the GEM chambers
- Ongoing tuning of trigger signal and APV25 data latency for optimization of the setting
- Plan to monitor the stability of the DAQ in the cosmic setup for a few days
- Will after move to the full DAQ system to read out all two chambers and take data for several days for efficiency study



Summary

- Two large PRad GEM chambers built at Uva
 - Preliminary cosmic data test conducted at UVa to test basic performances
 - Delivered to JLab in February and mounted on the support frames in the cosmic setup
- APV25-based SRS is the readout electronics for the Prad GEMs
 - Readout System is based on the SRS electronics developed by the RD51 coll. @ CERN
 - Challenge is to read out 9216 electronic channels (detector strips) @ 5 kHz trigger rate
- Firmware upgrade to allow high rate capability
 - SRU firmware: implementation of 10 Gb optical link for the data transfer from the SRU to the DAQ PC
 - FEC firmware: Implementation of the buffering trigger \Rightarrow allow 5 kHz trigger rate with limited dead time
- Integration of the SRS into JLab DAQ system
 - JLab custom board Tlpcie for the trigger interface between SRS and Prad DAQ system
 - Development of the Tlpcie libraries and slow control routines, online monitoring software
- Cosmics setup of the GEM chambers with SRS readout / DAQ
 - First real data from the GEM with the full DAQ chain
 - Test of the DAQ / readout and preliminary study of the chamber detection efficiency
- Goals and plans for the coming weeks before the installation in Hall B
 - Implementation of the zero suppression algorithm for online data reduction
 - More tests and checks of the performances of the DAQ and GEM chambers with cosmic setting

Back Up