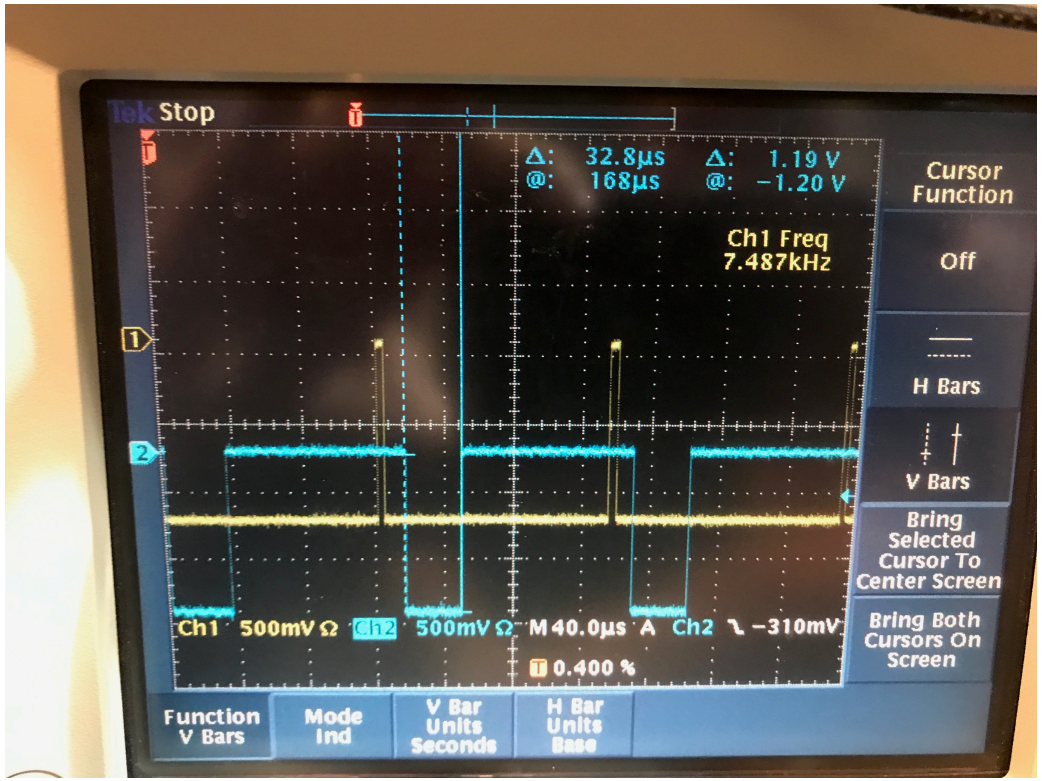
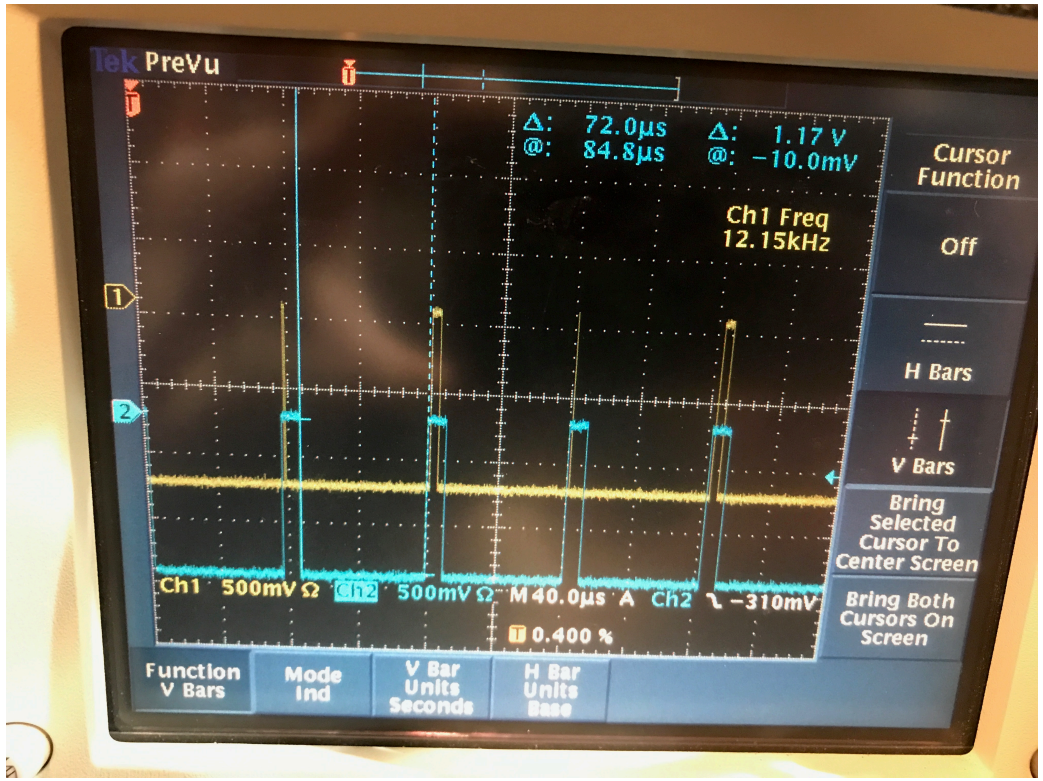
fADC TI Readout Time

TI Readout time in Mode 9 (pulse integral)



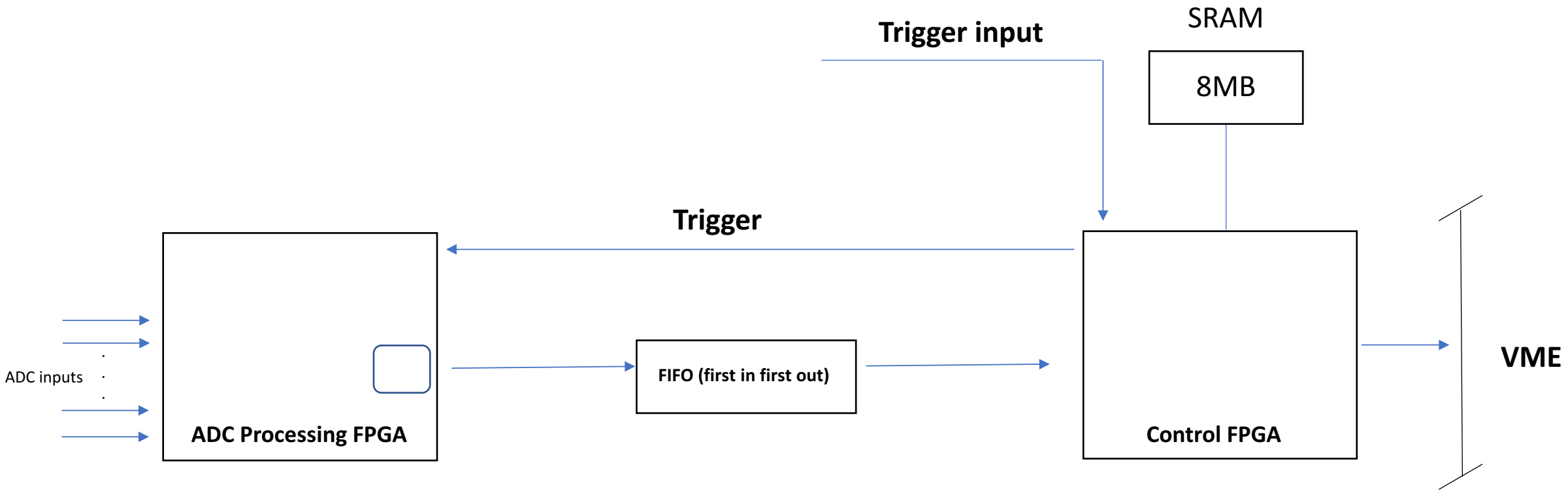
Read out time : 32.8 μs

TI Readout time in Mode 10 (Raw Sample)



Read out time : 72.0 μs

Simplified Trigger processing path



*Reproduced from Ed Jastrzembski's presentation

fADC Busy Levels

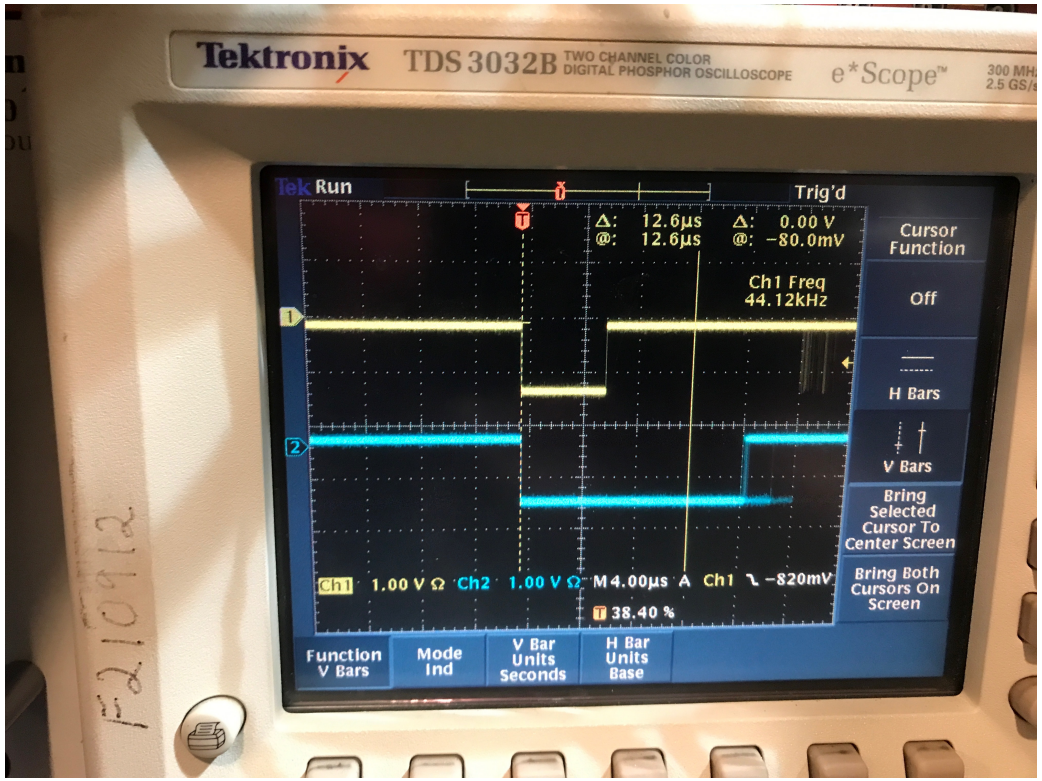
- Acknowledged trigger : Data associated with a trigger is sent to the control FPGA
- Limit on the number of unacknowledged triggers (based on the mode ,window width, & number of pulses processed for window).
- Too many unacknowledged triggers-> may overflow buffer
- Two Thresholds
    1. Number of unacknowledged triggers before module does not accept incoming triggers
    2. Number of unacknowledged triggers before module asserts a busy
- To insure buffer doesn’t become full and data becomes corrupt (loss of synchronization)
    1. Set second threshold lower threshold for unacknowledged triggers. Will assert a busy and communicate with TS to stop sending triggers. Allows triggers in pipeline to still be processed. Should limit synchronization errors

Fadc Busy

- Two scenarios when fADC will be busy
  1. 8 MB buffer is full
  2. Trigger rate – has 2 thresholds
     - Before module stops accepting incoming triggers (if asserted may cause sync. error)
     - Before asserting a busy (should be lower threshold than 1st to allow communication with TS)
- We confirmed the fADCs are producing a busy when
  1. When buffer is full
  2. When threshold for asserting busy = 1

FADC Busy
FaSetTriggerBusyCondtion = 1

Mode 9



Fadc Busy : 6.3 μ

Mode 10

Fadc Busy : 18.3 μ

fADC Summary

Measured quanity	Mode 9	Mode 10
TI Readout Time	32.8 μs	72.0 μs
fADC Busy	6.3 μs	18.3 μs

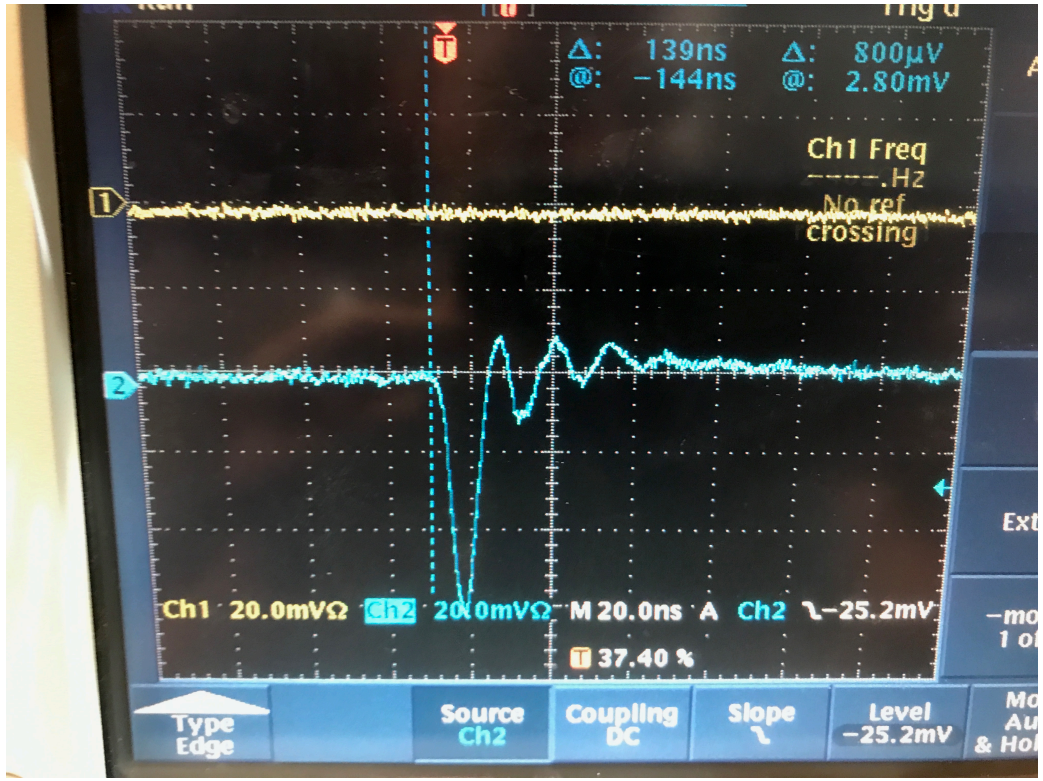
LHRS:Fastbus Busy

Crate	Busy	Readout time
Top	2 μs	51.2 μs
Middle	2 μs	35 μs
Bottom	11 μs	107 μs

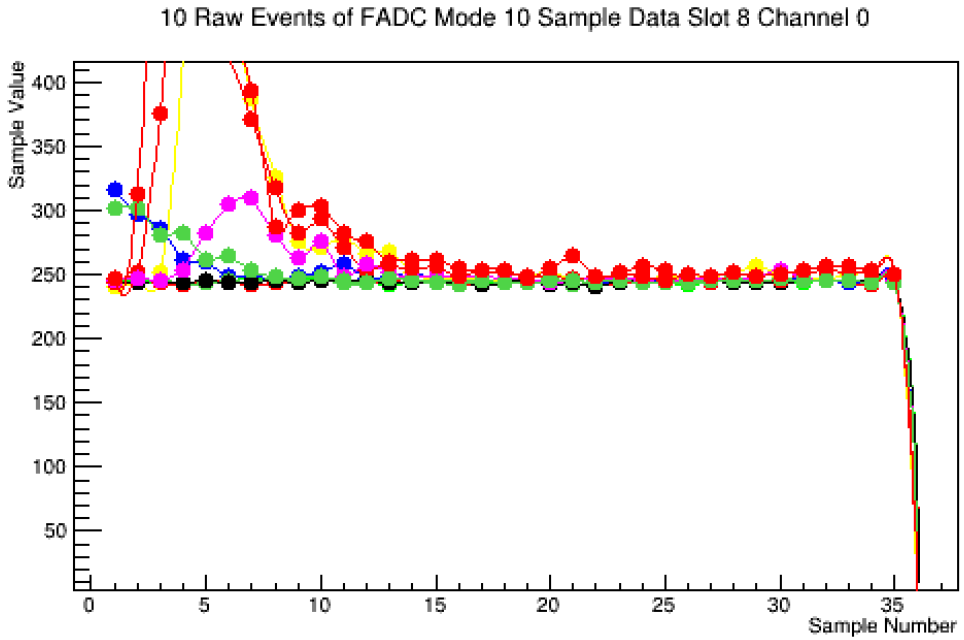
New Filter/Splitter

Signal to electronics

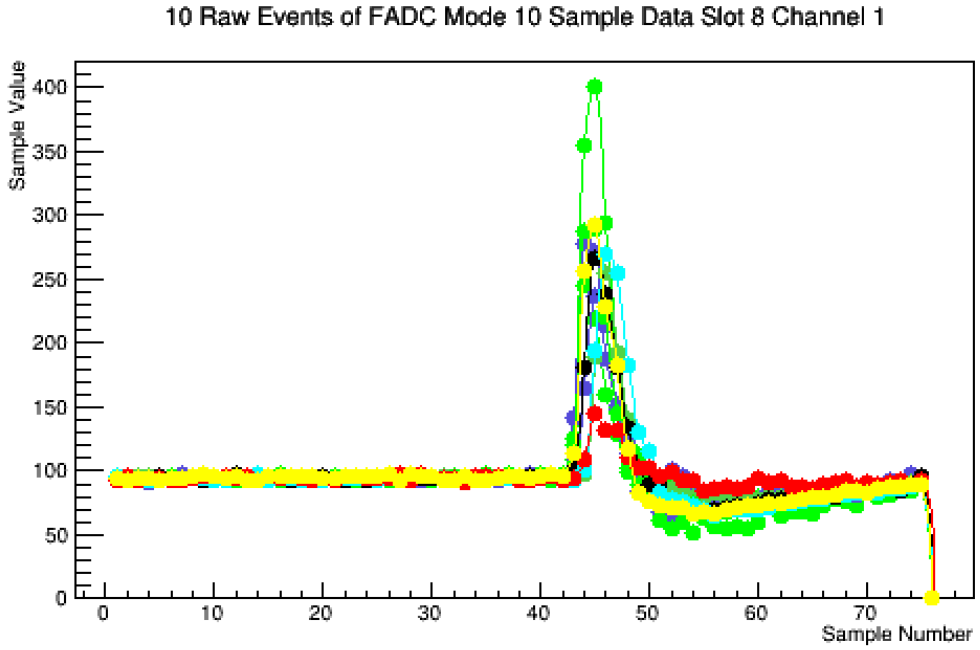
Signal to fADC



Previous splitter

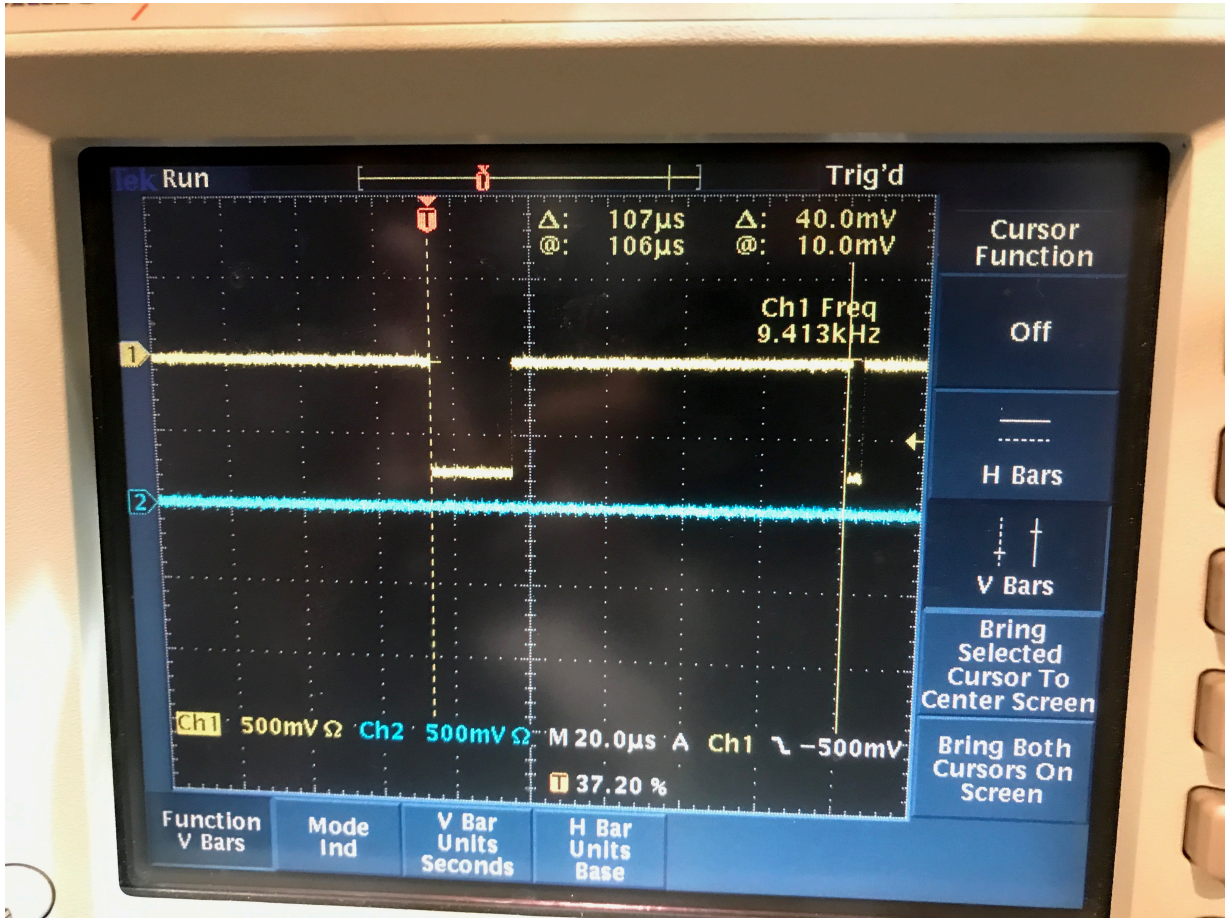


New Filter/splitter



Fastbust readout time (top crate)

Fastbus Readout time (Bottom crate :ADC)



Fastbus Readout time (Middle crate :ADC)