Introduction to FADC based detector class

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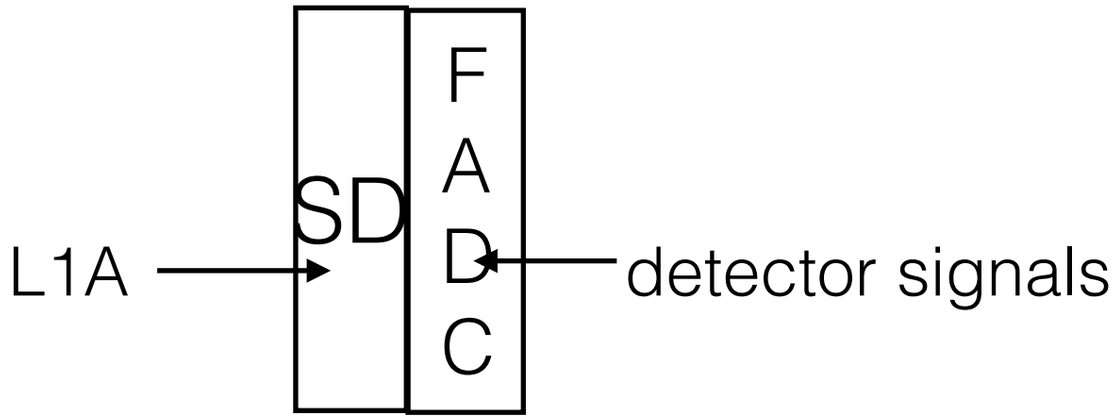
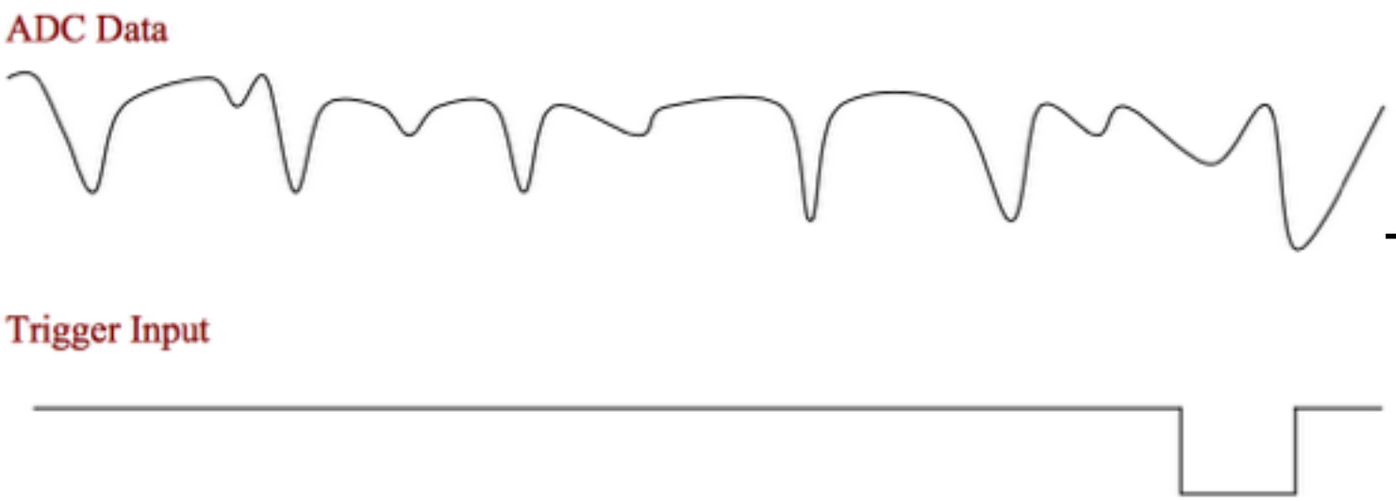
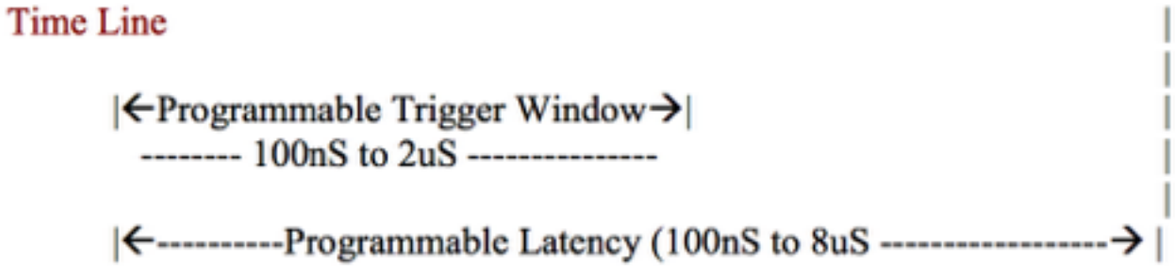
- new things added to FADC based detector class: S0, S2, Cer;
- useful FADC data when threshold is set;
- current FADC configuration for both arms;

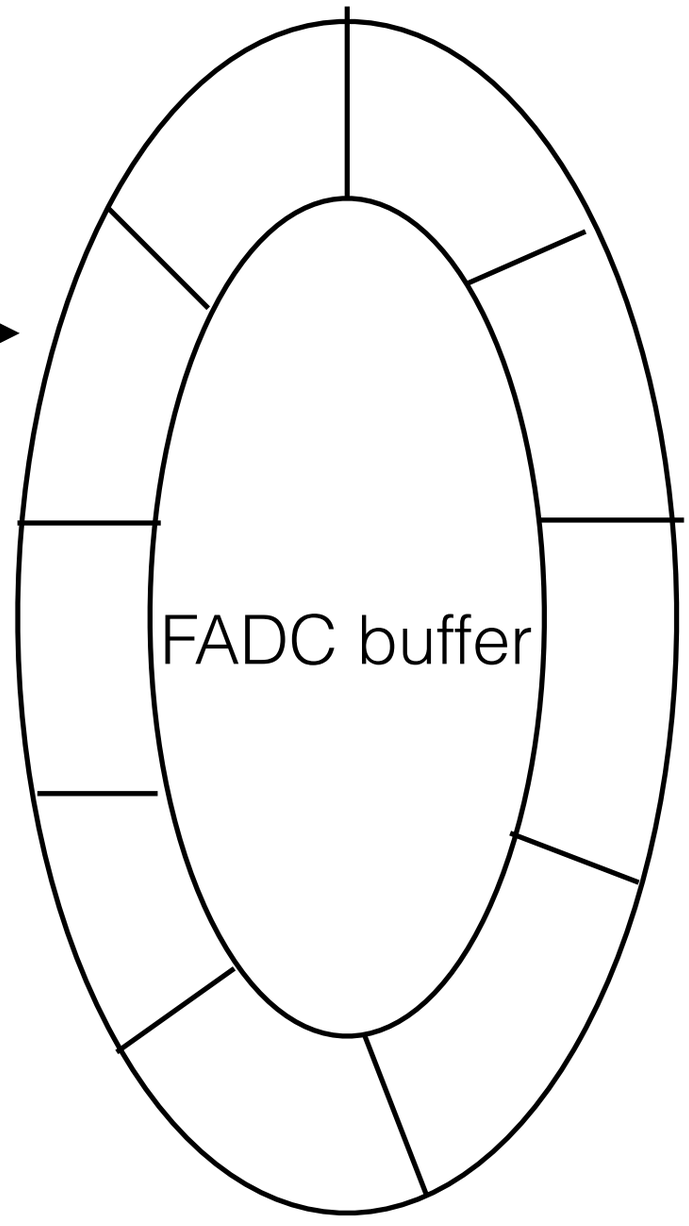






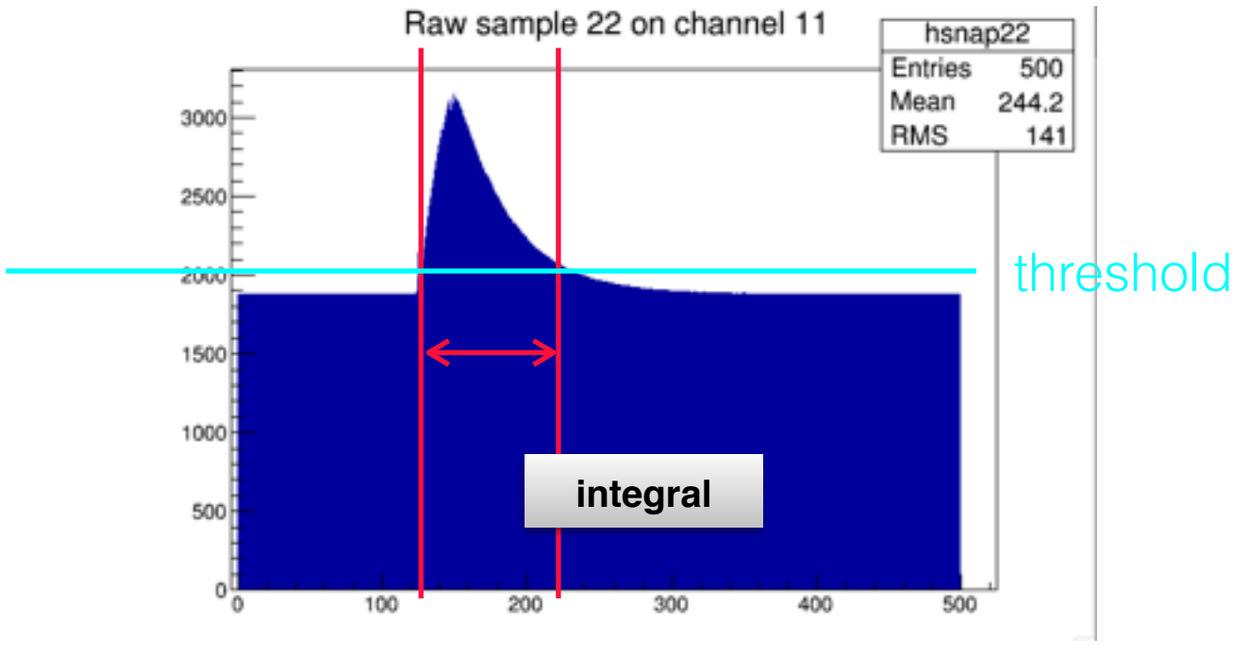
put in

readout



Pulse integral mode (mode 9)

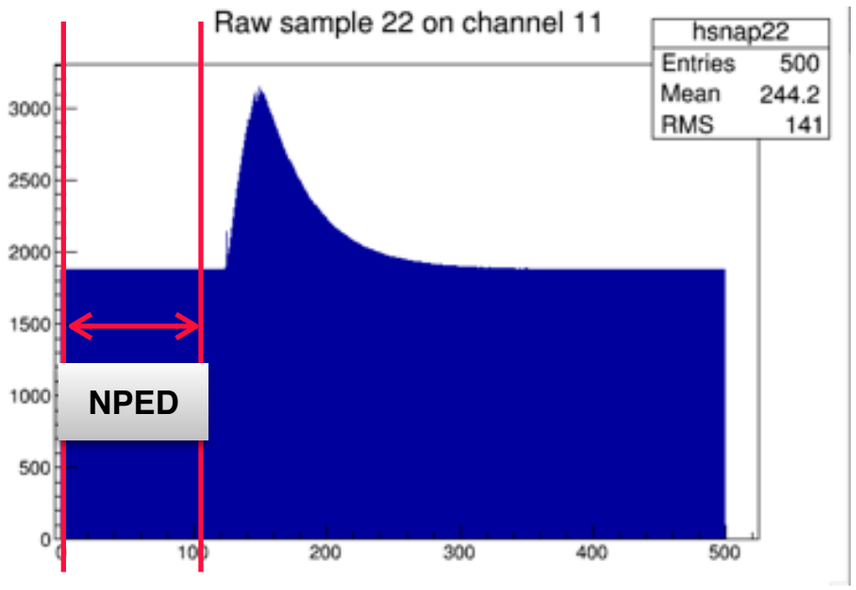
- **Integral number**



For each event:

- integral number
- time crossing the threshold
- pedestal

• pedestal subtraction



For each event:

- sum first NPED samples as pedestal sum
- ped = ped_sum/NPED * Integral_window

- **in S0, S2, Cer database: NPED, Win**

needs to be same as what are in FADC readout list

Parameters for pulse quality

- overflow bit:

when one or more samples of a pulse is overflow, the overflow bit will be set to 1, and the value of overflow samples will be 4095 (maximum pulse value)

- underflow bit:

when one or more samples of a pulse is underflow, the underflow bit will be set to 1, and the value of underflow samples will be 0;

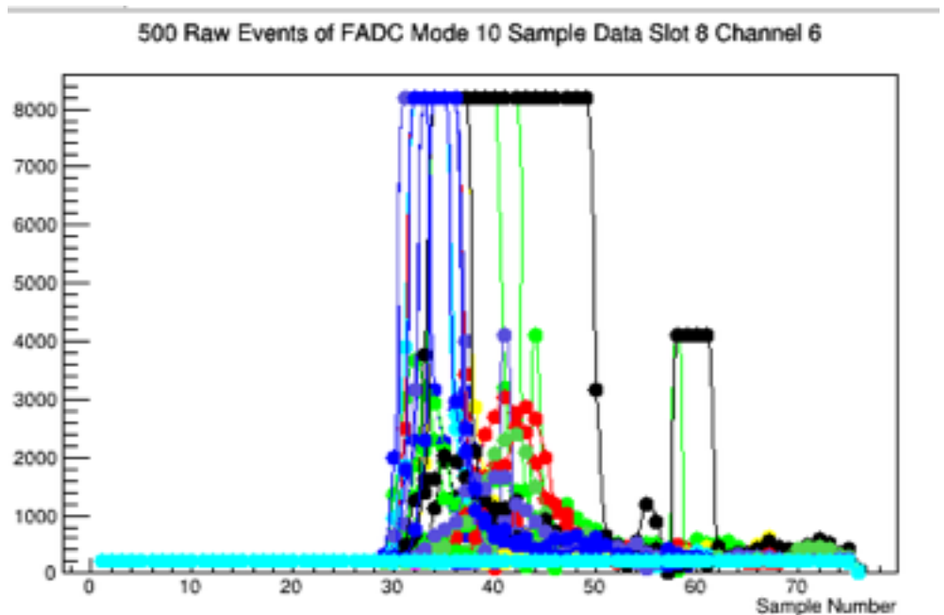
- pedestal quality bit:

when any of NPED samples is greater than MAXPED or is underflow or overflow, this bit will be set to 1. In this case, FADC based detector class will use the average pedestal in DB as the pedestal for this event.

add to S0, S2, Cer block

S0, S2: loverflow, lunderflow, lbadped (left PMT)
roverflow, runderflow, rbadped (right PMT)

Cer: noverflow, nunderflow, nbadped

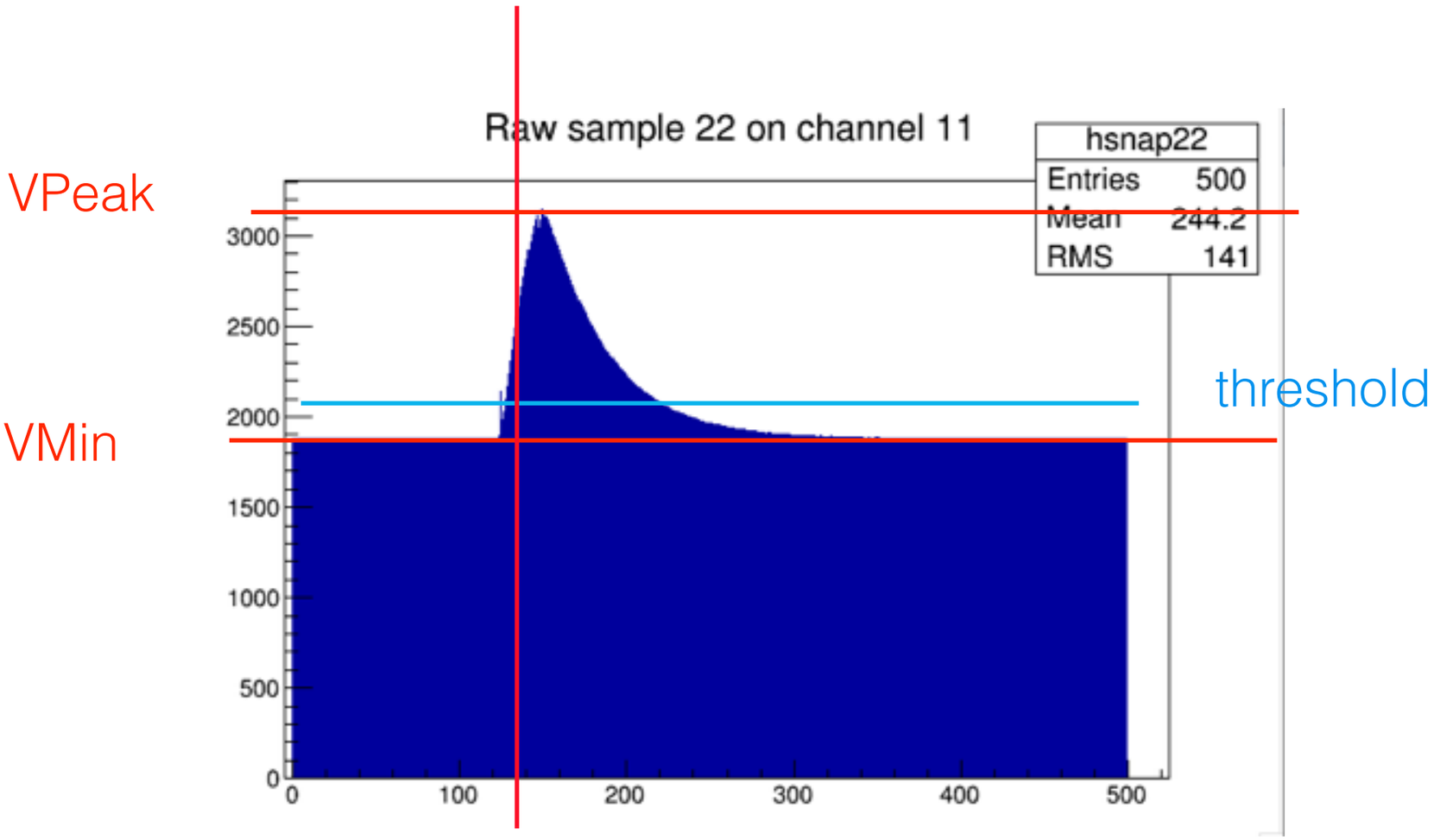


Parameters might help when use threshold

When having threshold, will have:

- VPeak: value of pulse peak;
- number of samples within integral window that it's above threshold;
- TF: fine time of half pulse;

→ no time walk effect



TF= time of (VPeak+VMin)/2 in the unit of 62.5ps

FADC configuration settings

LHRS

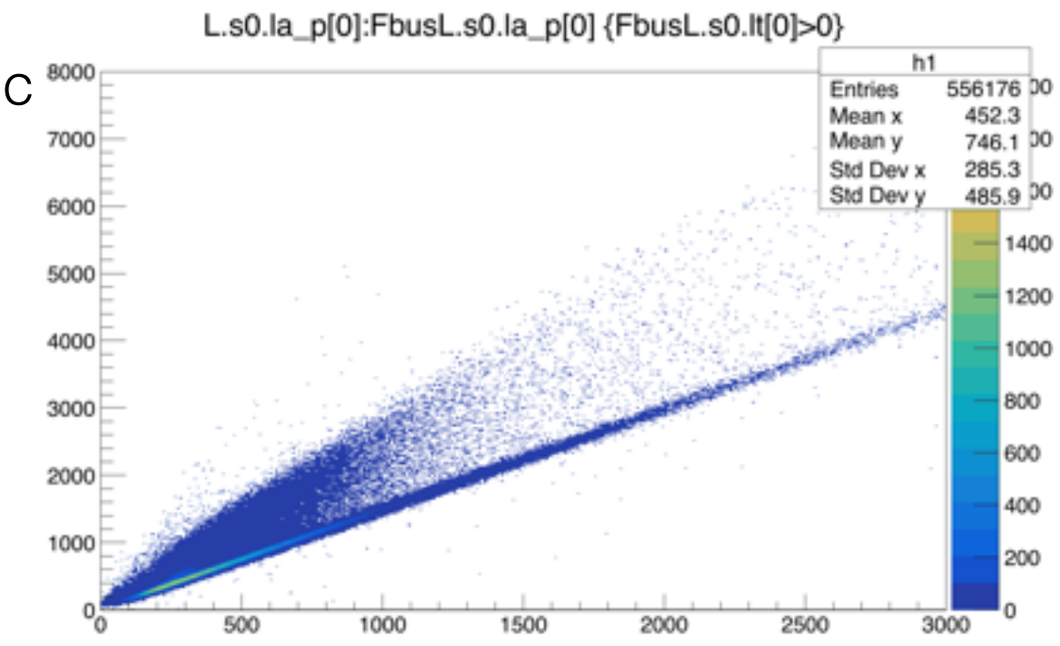
	Slot 6 (s2_la)	Slot 7 (s2_ra)	Slot 8 (s0 & cer)	Slot 9 (Raster & BPM)
PL	71	71	71	71
PTW	50	50	50	50
NSB	3	3	3	3
NSA	50	50	50	50
NPED	15	15	15	15
MAXPED	160	160	160	160
DAC	3200	3200	3220	2500
voltage range (V)	0.5	0.5	0.5	2

RHRS

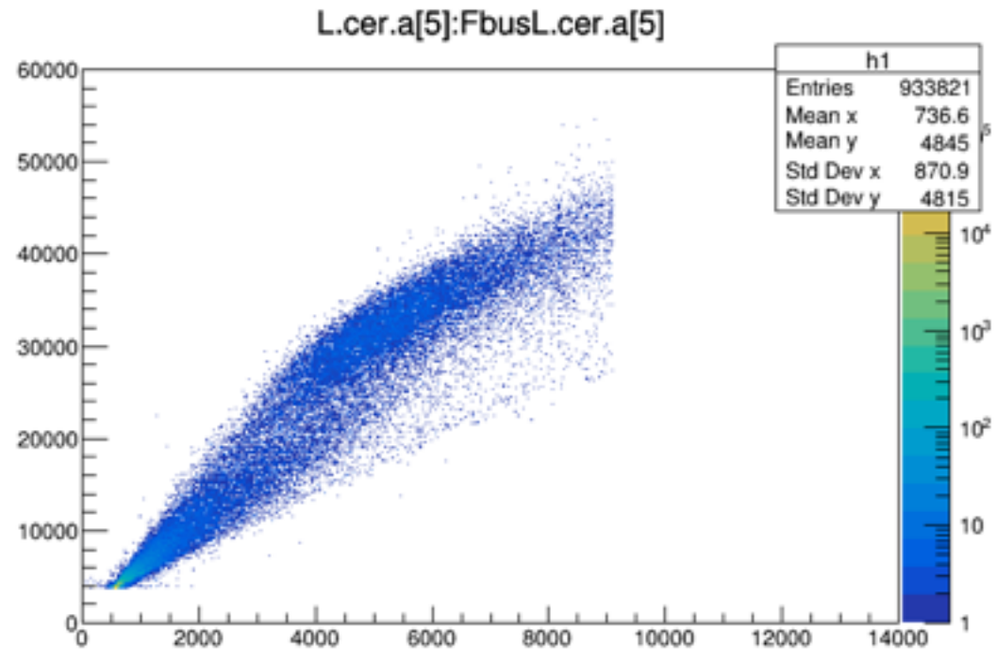
	Slot 13 (s2_la)	Slot 14 (s2_ra)	Slot 15 (s0 & cer)	Slot 16 (Raster & BPM)
PL	65	65	65	65
PTW	55	55	55	55
NSB	2	2	2	2
NSA	55	55	55	55
NPED	15	15	15	15
MAXPED	160	160	160	160
DAC	3200	3200	3220	2500
voltage range (V)	0.5	0.5	0.5	2

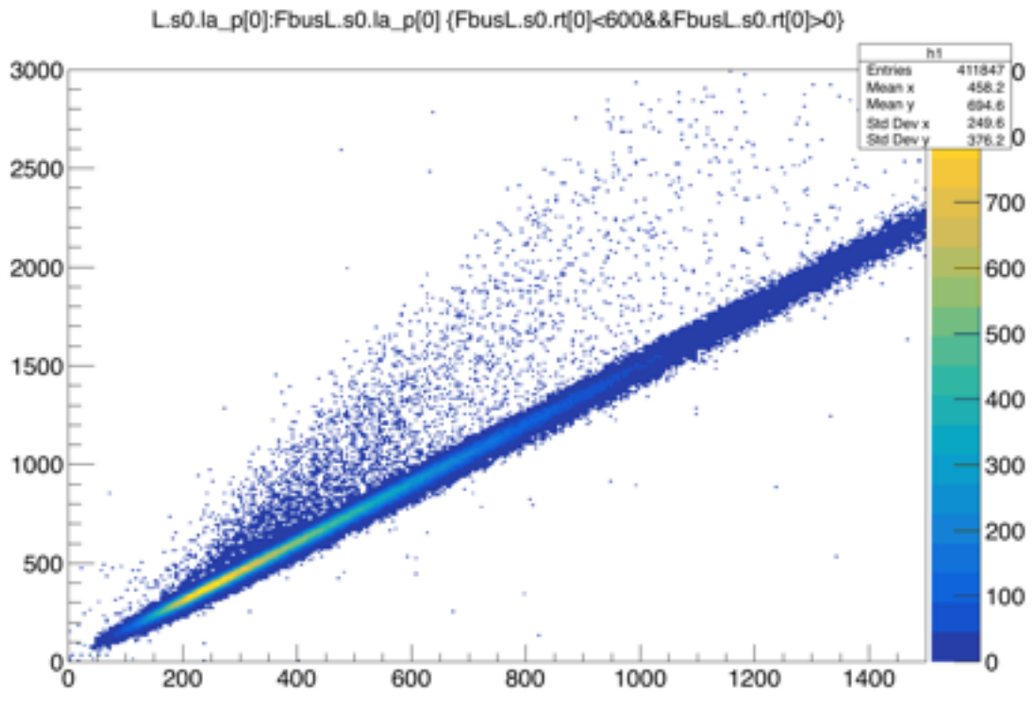
plots from Tong Su

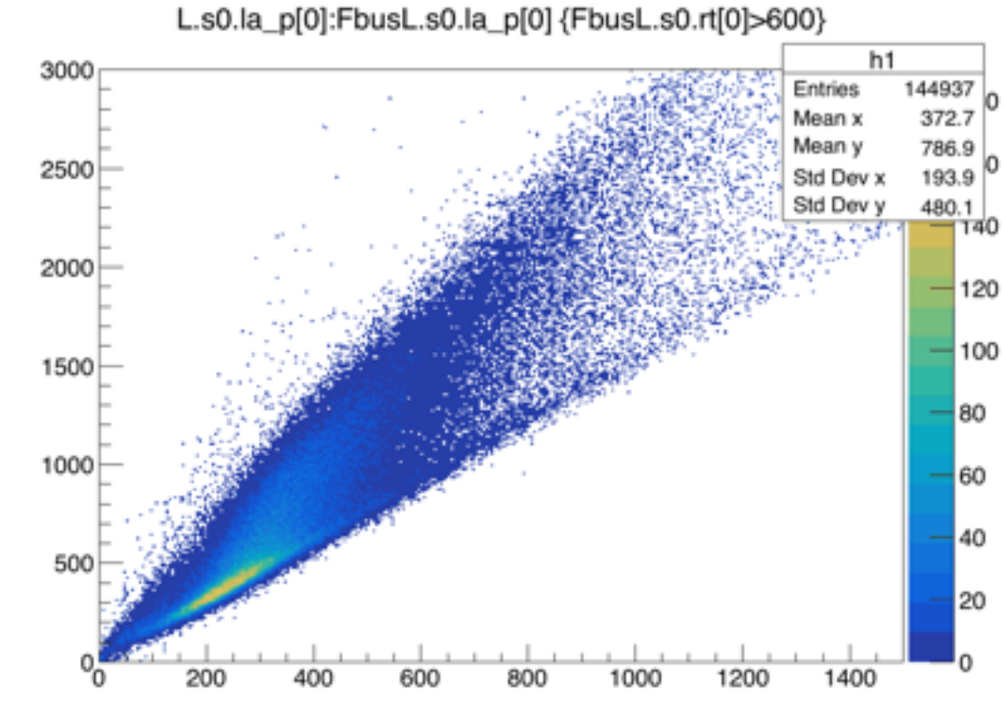
fadc

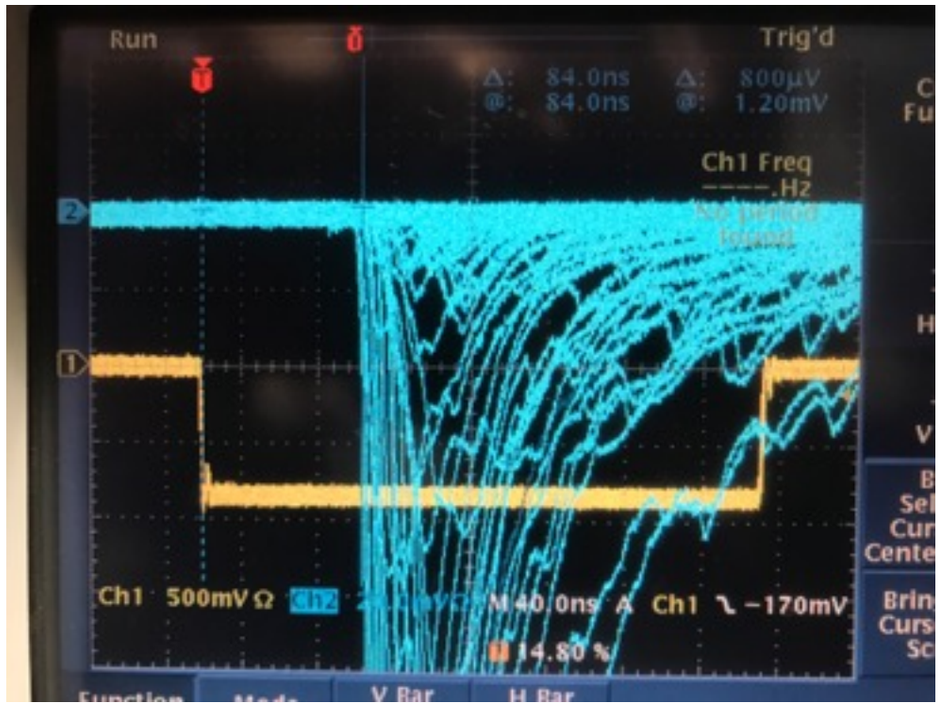


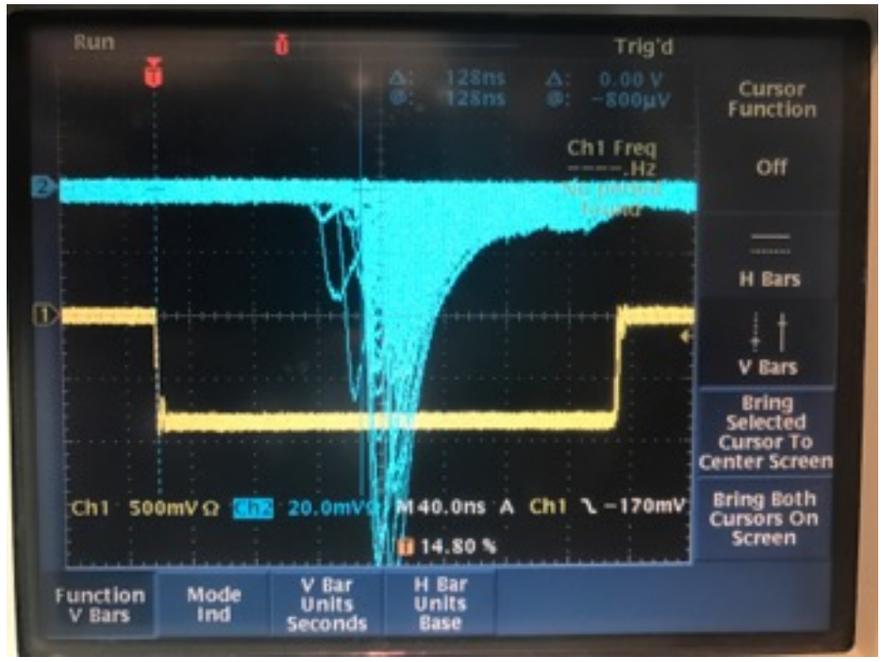
Fastbus

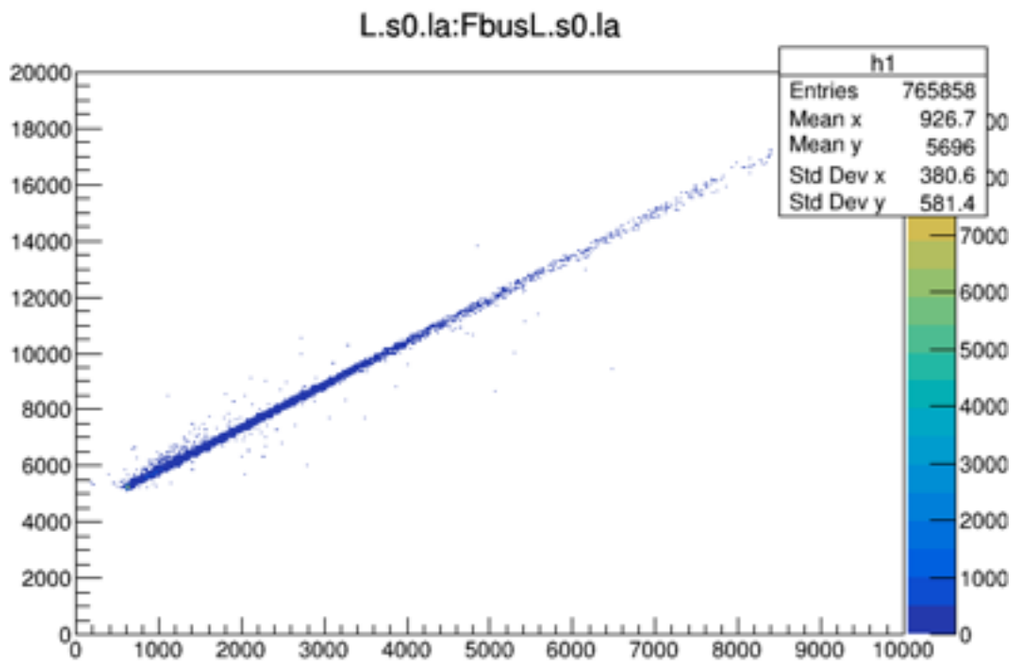


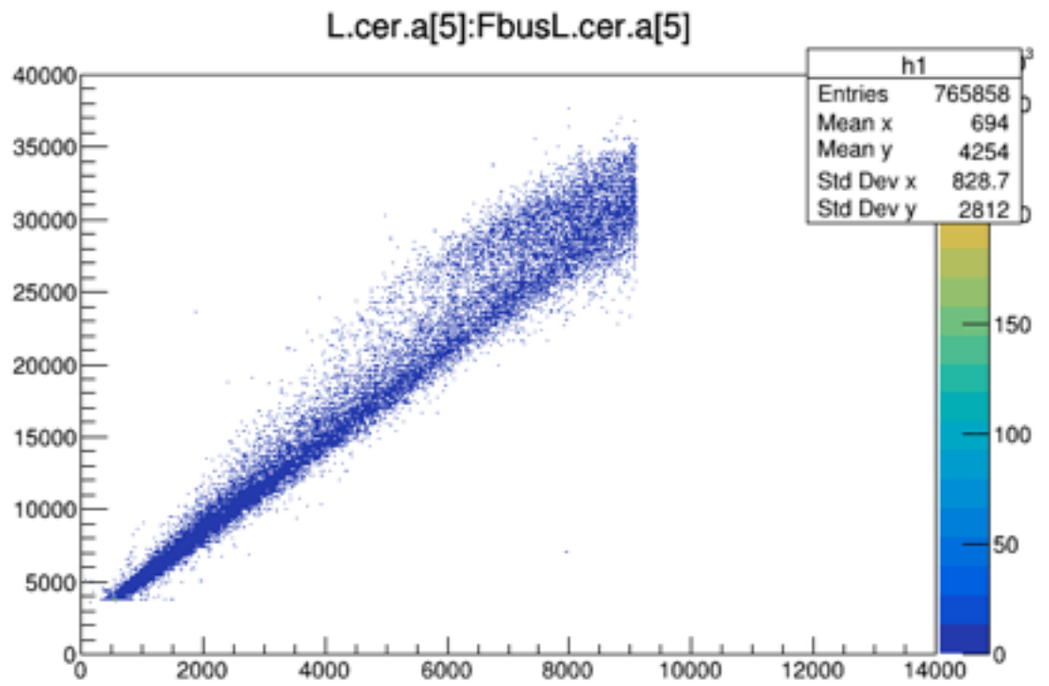





Run
Trig'd
Δ: 84.0ns Δ: 800µV
@: 84.0ns @: 1.20mV
Ch1 Freq
----.Hz
No pulses found
Ch1 500mV Ω Ch2
M40.0ns A Ch1 ∖ -170mV
14.80 %


Run
Trig'd
Δ: 128ns Δ: 0.00 V
@: 128ns @: -800µV
Ch1 Freq
----.Hz
No pulses found
Ch1 500mV Ω Ch2 20.0mV Ω
M40.0ns A Ch1 ∖ -170mV
14.80 %
Cursor Function
Off
H Bars
V Bars
Bring Selected Cursor To Center Screen
Bring Both Cursors On Screen
Function V Bars
Mode Ind
V Bar Units Seconds
H Bar Units Base


L.s0.la:FbusL.s0.la
h1
Entries 765858
Mean x 926.7
Mean y 5696
Std Dev x 380.6
Std Dev y 581.4


L.cer.a[5]:FbusL.cer.a[5]
h1
Entries 765858
Mean x 694
Mean y 4254
Std Dev x 828.7
Std Dev y 2812