Hall-A Tritium Analysis Meeting

JLab 250 MHz Flash ADC Modules

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Jefferson Lab

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On Behalf of the Hall-C DAQ Working Group

Jefferson Lab

FADC250: Technical Details

- Jefferson Lab's fast electronics group developed and maintains high speed and high density 250 MHz pipelined flash ADC modules

- Conditions, samples, digitizes, and processes fast negative-going analog signals at 250 MHz

- Data are stored in circular buffers every 4 ns

- Conforms to VME64x switched serial (VXS) standard

- Serial data is routed via the back plane to a switch slot at a rate of 6 Gb/s

- Provides information for energy deposition, timing, hits, and trigger information

- Currently utilized for production running in Hall's B, C, and D

- 72 channel FADC125's utilized for drift chamber readout in Hall-D

F.J. Barbosa, et al., GlueX Doc 1022
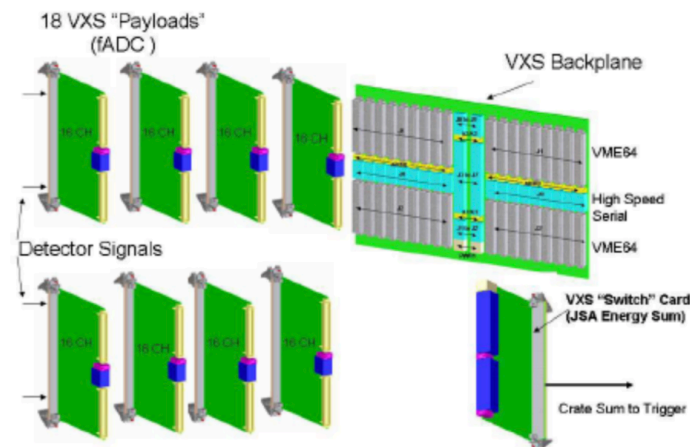
FADC250: Architecture

- 16 channel 50 Ω, coax, LEMO inputs

- There are 3 configurable ranges available *via*. jumpers: 0.5, 1.0, 2.0 V

- Differential signal conditioning scales the input signals to within the 12-bit dynamic range of the ADC's

- Individual channel offsets are effected by means of DACs under VME control

- Digitized data and clock signals are fed to a pair of FPGA's for data processing and temporary storage

- Third FPGA combines data from data processing FPGAs

- ADC data is stored in RAM for event building and is readout via VME

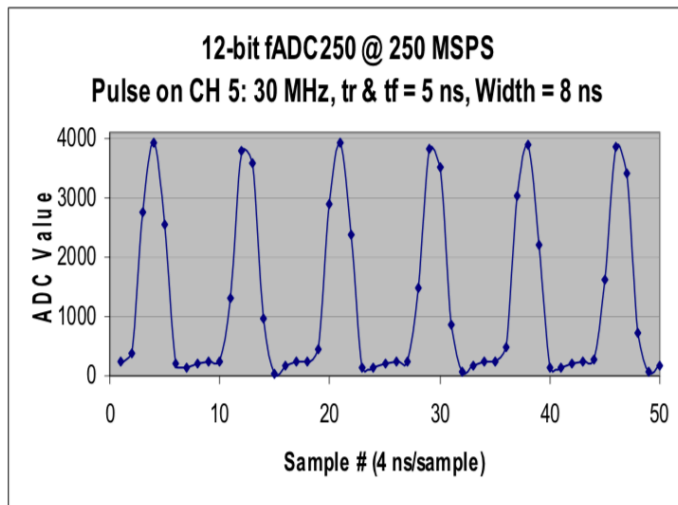- Fourth FPGA handles the control, trigger, and interface functions
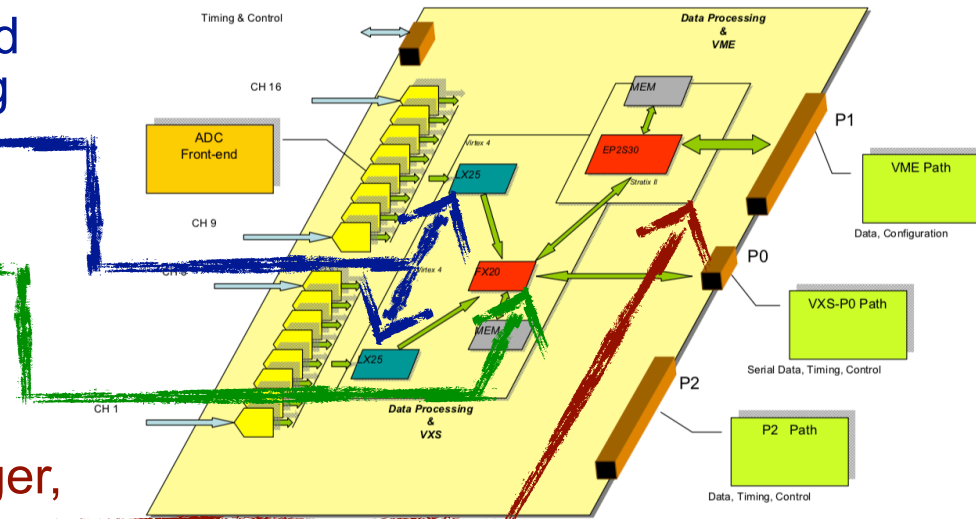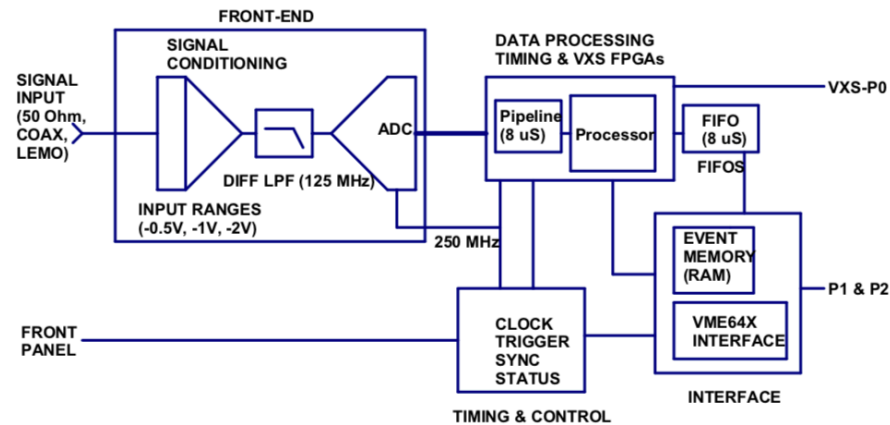
F.J. Barbosa, et al., GlueX Doc 1022

FADC250: Performance Specifications

- Two primary functional output data paths are configured for data readout and trigger information

- 8 µs pipeline with user programmable trigger latency and readout window widths

- Sparsification, charge, pedestal, timing, and peak values are obtainable

- Hit information with user defined thresholds and trigger processing also available

- Internal clock domains governed by differential PECL clock with < 2 ps jitter

12-bit fADC250 @ 250 MSPS
Pulse on CH 5: 30 MHz, tr & tf = 5 ns, Width = 8 ns

F.J. Barbosa, et al., GlueX Doc 870

fADC-250 Specifications
VME64x with VXS, Pipelined 250 MSPS Flash ADC Module

|			
Signal Inputs	Number	16	S Version (50 Ohm, LEMO)*
	Range	-0.5V, -1V & -2V. User Selectable	
	Offset	±10% FS per channel via DACs	
Clock	Sampling	250 MSPS, Differential	
	Jitter	1 pS (10-bit ADC), 350 fS (12-bit ADC)	
	Source	Internal and External	
Control Inputs/Outputs	Clock	N – Diff., LVPECL (Front Panel & Backplane)	
	Trigger	IN, OUT - Differential (Front Panel & Backplane)	
	Status 1	OUT – Differential (Front Panel & Backplane)	
	Status 2	OUT – Differential (Front Panel & Backplane)	
	Sync	OUT – Differential (Front Panel & Backplane)	
	Trigger	SW	Software Strobe (Internal)
Conversion Characteristics	Resolution	10-bit (8 and 12-bit by chip replacement)	
	INL	± 0.8 LSB	
	DNL	± 0.5 LSB	
	SNR	56.8 dB @ 100 MHz Input	
	Data Latency	32 nS	
Trigger Latency	8 µS		
Data Memory	8 µS		
Data Processing	Sparcification		
	Windowing		
	Charge, Pedestal, Peak, Energy Sum on VXS for Trigger		
	Time (Over Threshold, Relative to trigger)		
	Output (Backplane, VXS)		
Interface	VME64x – 2eVME Data Transfer Cycles (40, 80, 160 & 320 MB/sec) with VXS-P0		
Packaging	6U VME64x		
Power	+3.3V, +5V, +12V, -12V		

F.J. Barbosa, et al., GlueX Doc 1022

FADC250: Bench Performance

- FADC250's provide excellent resolution and pedestal differences of <10%

  - Pedestal variation is a measure of the intrinsic rms resolution

  - $\sigma = 1.5$ LSB for single channel

  - $\sigma = 1.43 \pm 0.06$ LSB for 8 channels

- No cross talk present even under saturating conditions, effects are within noise margins
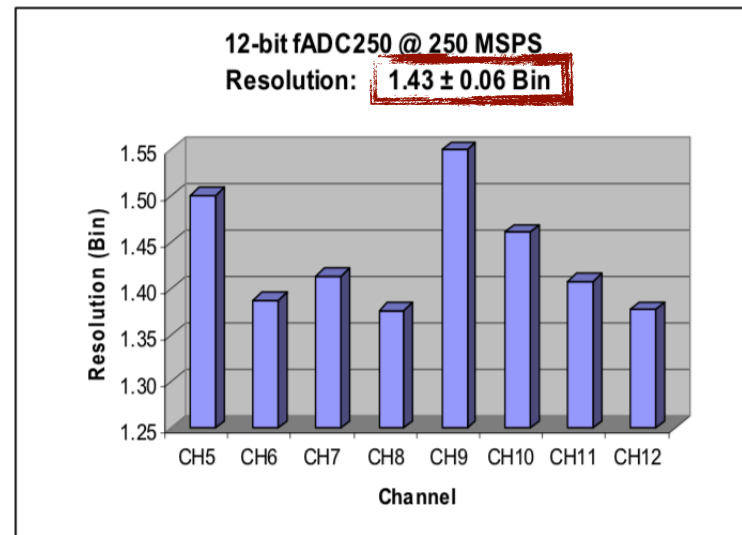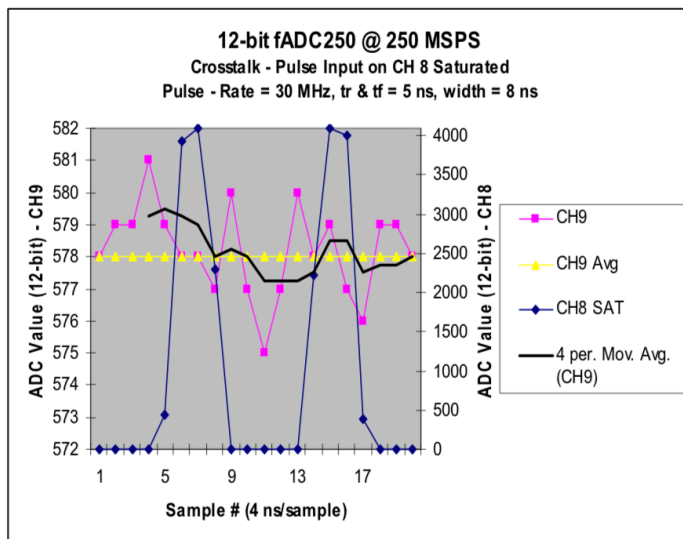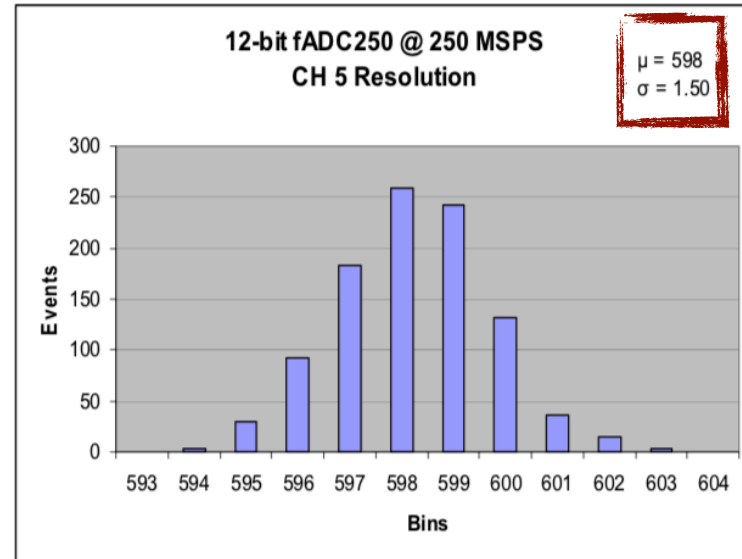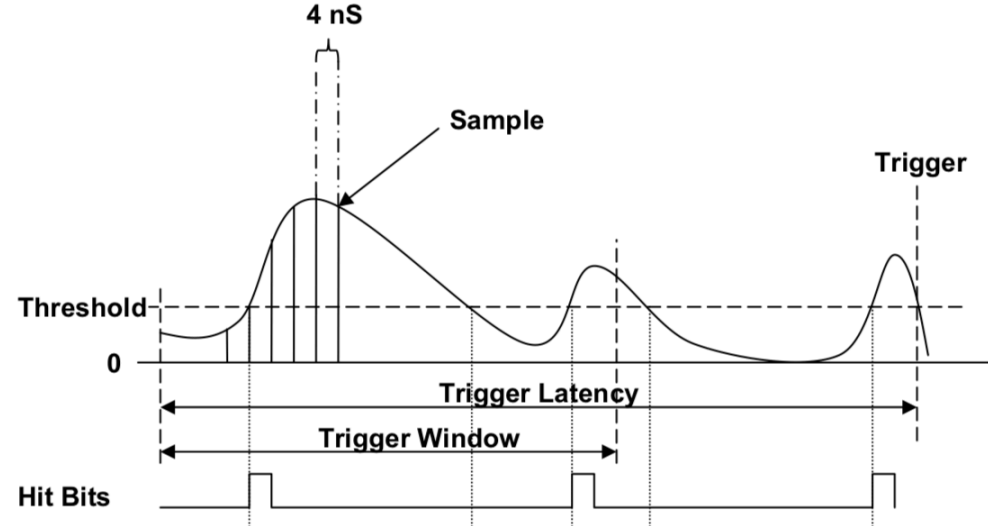

F.J. Barbosa, et al., GlueX Doc 870

F.J. Barbosa, et al., GlueX Doc 870
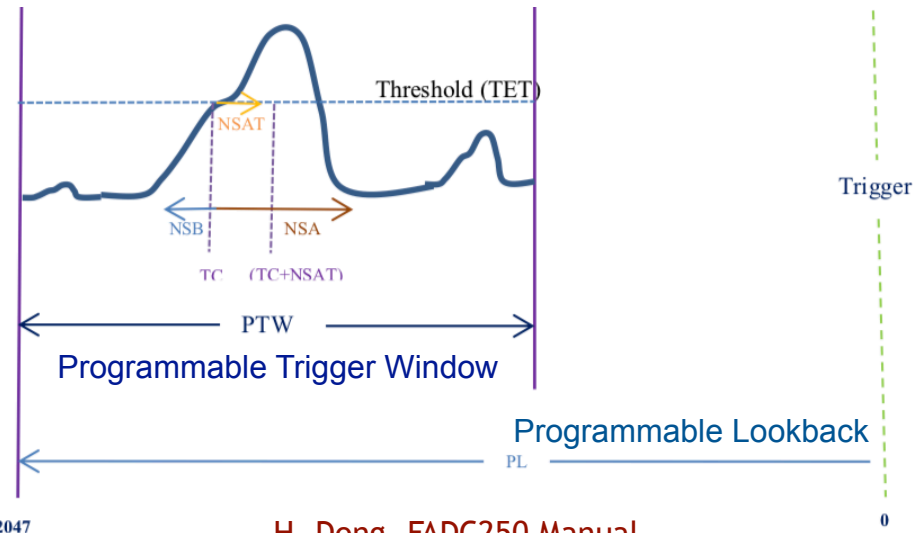
FADC250: FPGA Pulse Processing

- ADC samples are stored in 2048 sample circular raw buffers

- When a trigger is received, the 12-bit trigger number counter is incremented and a PTW number of ADC samples are stored in the unprocessed buffer

- PTW is user programmable from 5 to 511 (9-bits, ≈ 2 µs)

- PL is user programmable from 0 to 2047 (11-bits, ≈ 8 µs)

- Sample processing is comprised of two modes (> 0x0C00)

  - 9 ➤ Production Mode

  - 10 ➤ Debug Mode

F.J. Barbosa, et al., GlueX Doc 1040

Programmable Trigger Window

Programmable Lookback
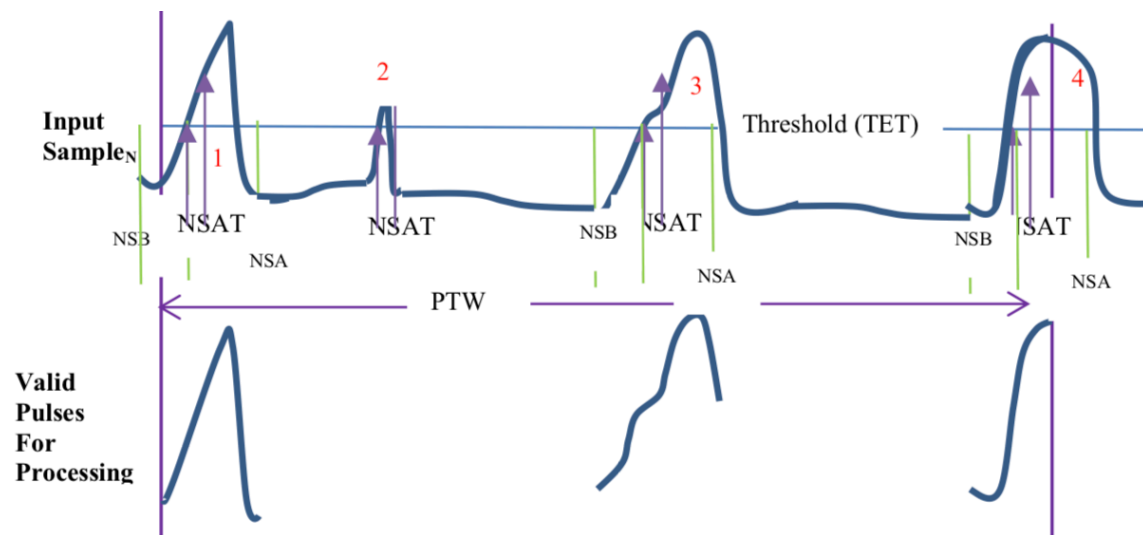
H. Dong, FADC250 Manual

- Pulse identification is initiated if number of consecutive pulses samples (NSAT) are above the programmable threshold (TET)

- The pulse duration includes the ADC number of samples before (NSB) and after (NSA) the first sample crossed the threshold (TC)

- NSA $\in$ [2, 511] (9 bits), NSB $\in$ [-8, 8] (4 bits) : + indicates number of samples before TC, - indicates number of samples after TC to be excluded from the pulse duration

- The pulse data only includes samples within PTW even if NSB and/or NSA extend beyond PTW

- Up to four pulse are detectable within PTW

- Pulse must have at least one sample < TET before pulse is identified

- If NSB > 0, TC must be within last NSAT + 1 samples of the window

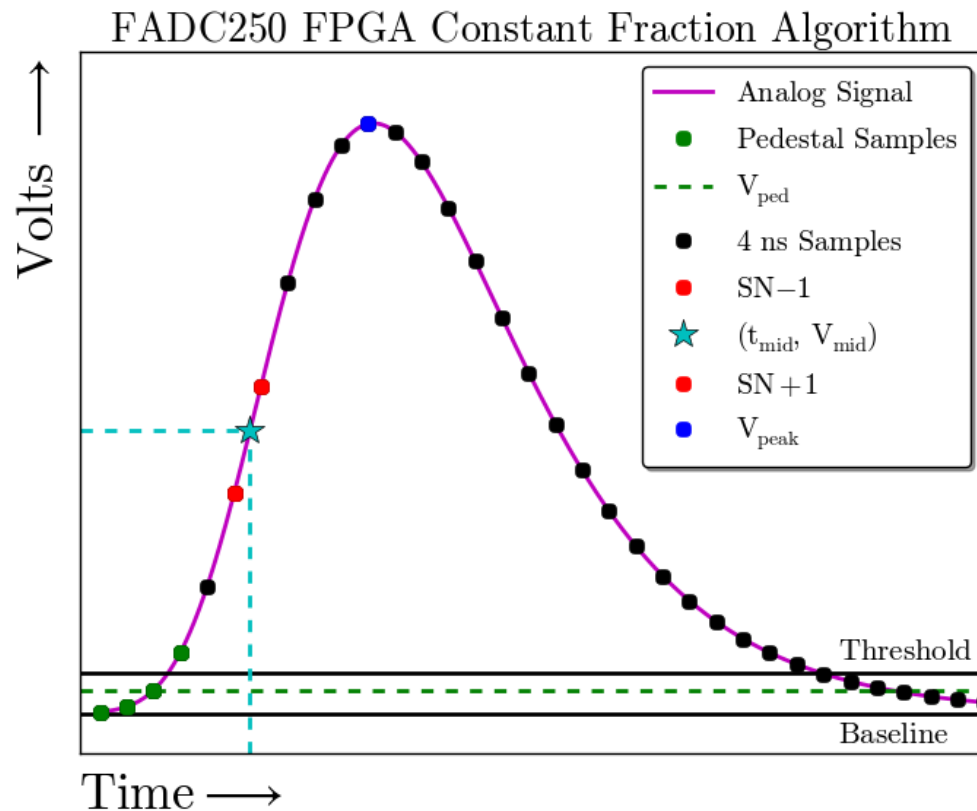- If NSB < 0, TC must be within last NSAT + NSB + 2 samples of the window

H. Dong, FADC250 Manual

- Pulse integral is the sum of samples of the defined pulse duration (18 bit word)

  - Integral quality bits (3 bits) identify instances of under & over flow, exceeding PTW

- Pulse pedestal is the sum of NPED samples after the beginning of PTW

  - NPED $\in$ [4, 15], if pedestal is above MaxPed, or identified as under or over flow, quality bit is set

- Pulse amplitude (12 bit word) identifies maximum value of identified pulse

  - Found when the current sample is less than the one that preceded it

- Pulse time is the time in which the leading edge of the identified pulse reaches half of its maximum sampled amplitude

FADC250 FPGA Constant Fraction Algorithm

Legend:
- Analog Signal
- Pedestal Samples
- V_{ped}
- 4 ns Samples
- $SN-1$
- (t_{mid}, V_{mid})
- $SN+1$
- V_{peak}

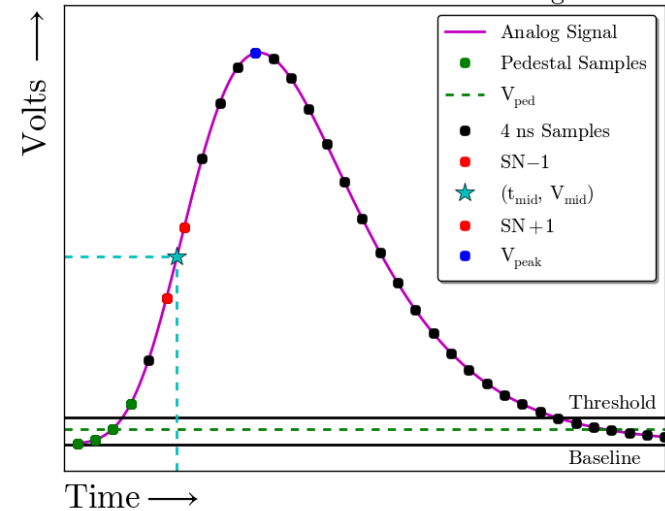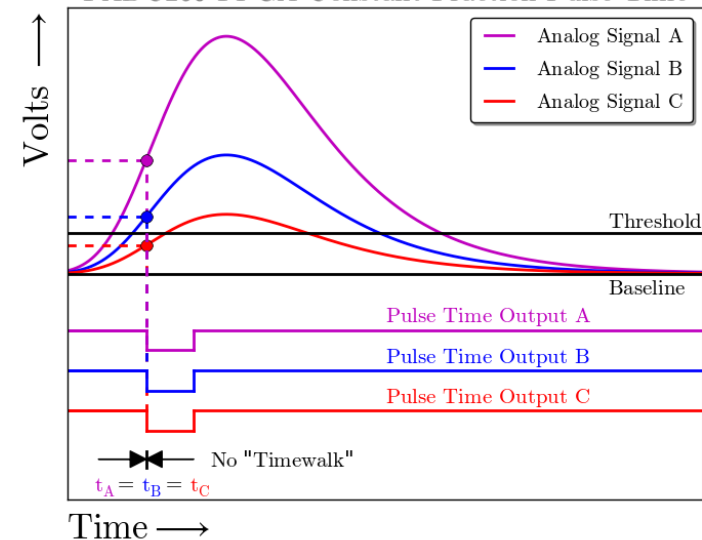Threshold

Baseline

Volts →

Time →

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FADC250: Production Mode (9)

- With V_{ped} & V_{peak} known, the half amplitude V_{mid} is computed: $V_{mid} = (V_{peak} - V_{ped}) / 2$

- Samples before and after V_{mid} are determined: SN-1 & SN+1

- The 4 ns time between V(SN-1) & V(SN+1) is divided into 64 sub-samples (62.5 ps)

- The high resolution time (t_{mid}) corresponding to Vmid is determined *via*. linear interpolation

- $t_{mid} = 64*(V_{mid} - V(SN-1)) / (V(SN+1) - V(SN-1))$

- The fine time is time-walk independent (CFD)

- Coarse time is reported as the time in which V(SN-1) occurred (4 ns jitter)

- If the high resolution pulse time algorithm fails, the time reported is the TC time (coarse) and time quality bits are set


FADC250 FPGA Constant Fraction Algorithm

Analog Signal
Pedestal Samples
V_{ped}
4 ns Samples
SN−1
(t_{mid}, V_{mid})
SN+1
V_{peak}

Threshold
Baseline

FADC250 FPGA Constant Fraction Pulse Time

Analog Signal A
Analog Signal B
Analog Signal C

Threshold
Baseline

Pulse Time Output A
Pulse Time Output B
Pulse Time Output C

No "Timewalk"
$t_A = t_B = t_C$

- In addition to calculating the pedestal, amplitude, integral, and high resolution pulse time, all the samples in PTW are recorded if there is at least one pulse identified
- All data written out includes both a trigger number, and trigger time

25 Raw Events of FADC Mode 10 Sample Data Slot 3 Channel 15

FADC Mode 10 Pulse Peak Data Slot 3 Channel 15 Event 6

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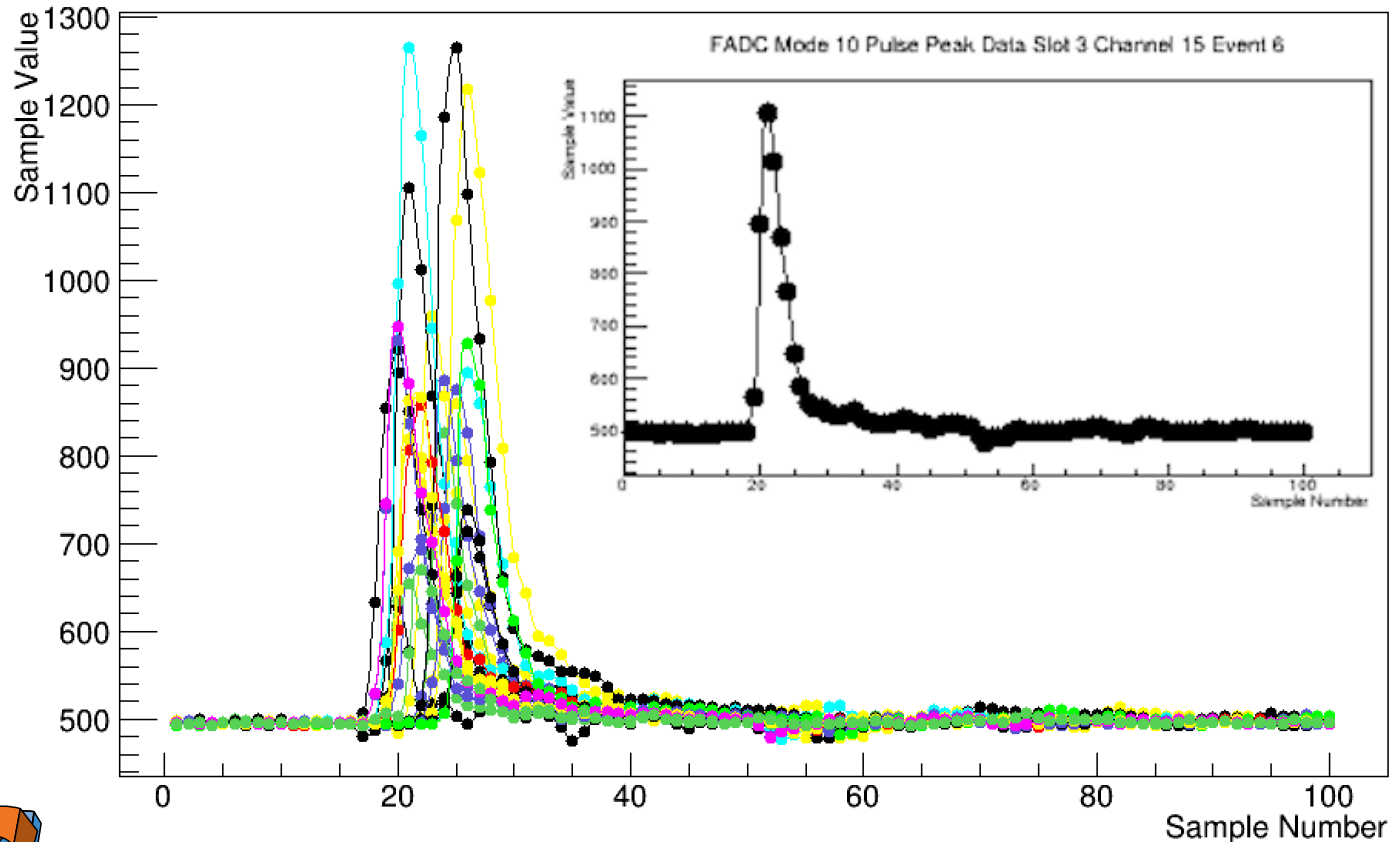
Hall A/C FADC250 Decoder

- Fadc250Module class is maintained in podd, resides in hana_decode directory
- Backwards compatible with pre 0x0C00 firmware versions
- Standalone utility tstfadc_main.C included in podd/hana_decode
- Scans crate for F250 modules, histograms all possible data in crate/slot identified as a F250

45 Raw Events of FADC Mode 10 Sample Data Slot 7 Channel 15
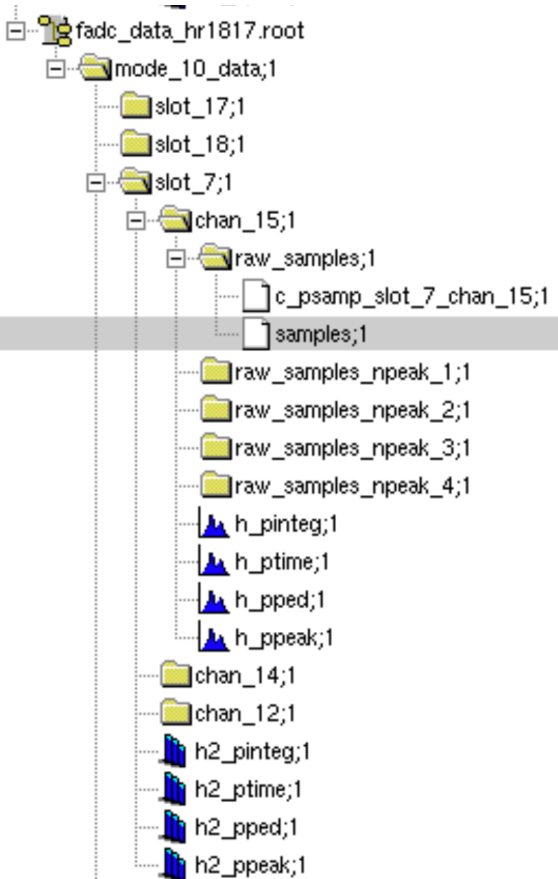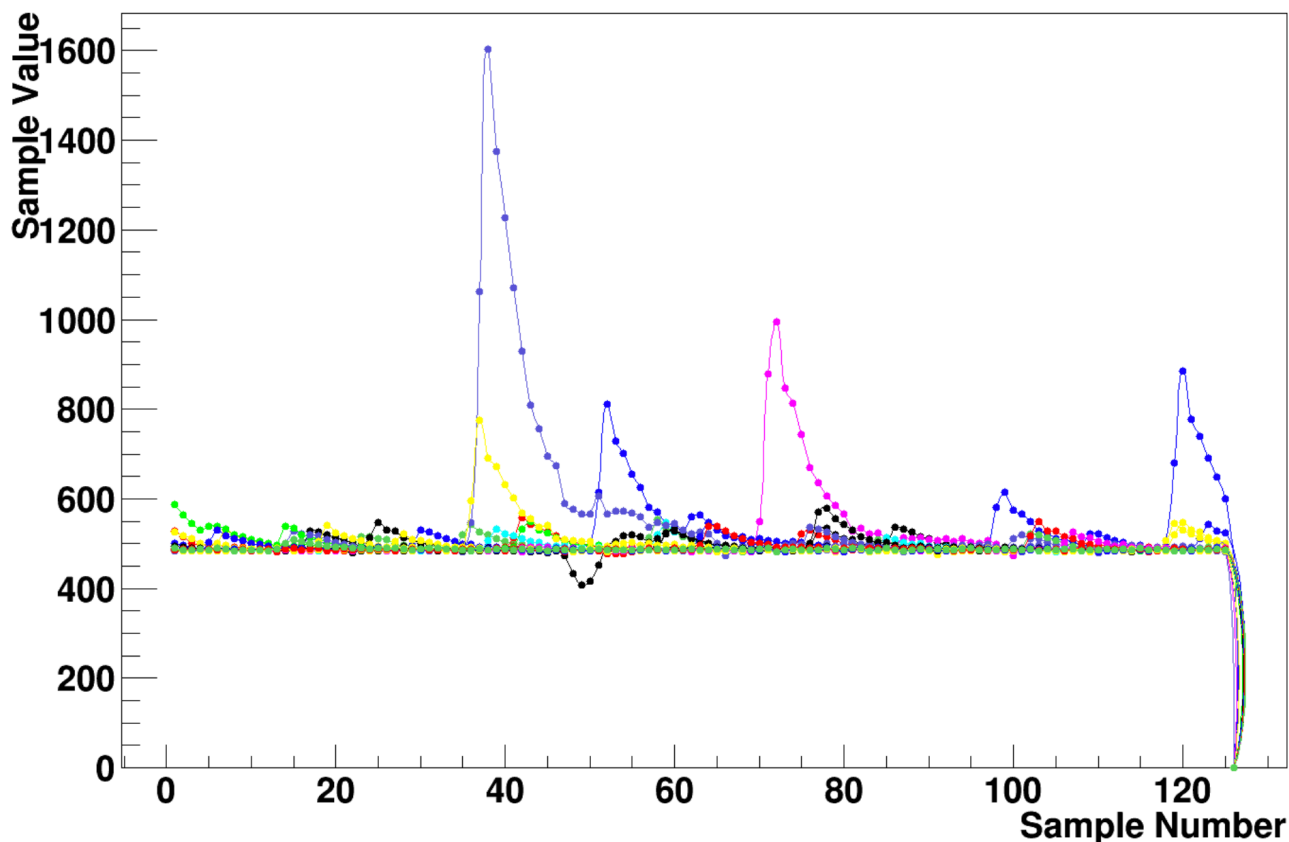
Hall A/C FADC250 Threshold Script

- calc_thresh.cxx in podd/hana_decode utilizes the output of tstfadc_main.cxx to produce a CRL readable file containing the individual thresholds for each FADC channel in a readout crate

- Currently, the script only applies a single global threshold for all channels in a single crate
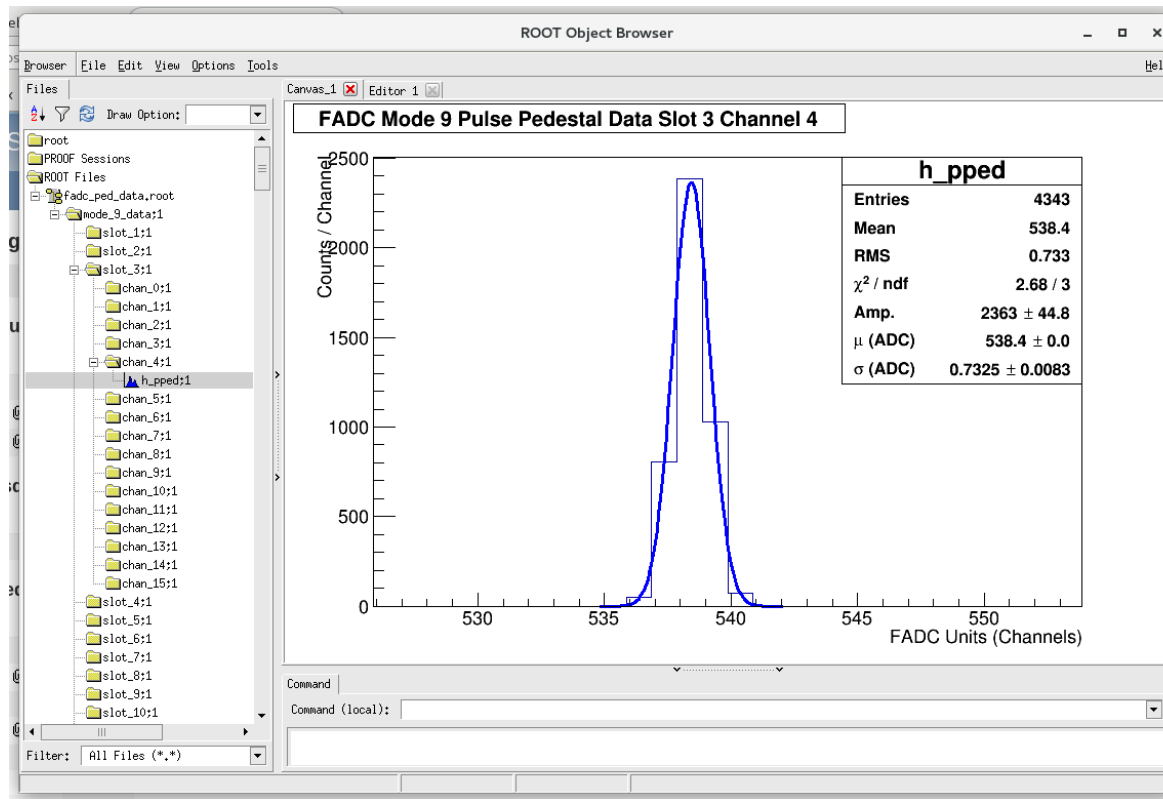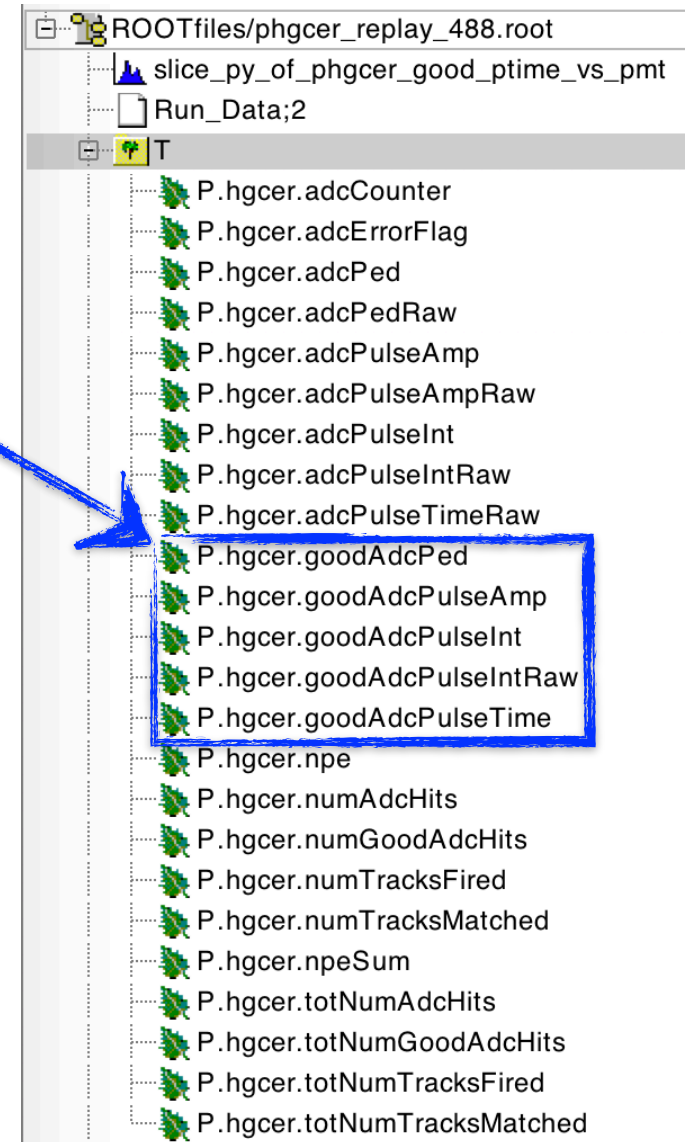
FADC250 Data Structures in HCANA

- "Good" ADC variables are calculated in the detector class CoarseProcess method

- FADC error flag cut

  - Removes events in which the FADC250 FPGA fails

  - adcErrorFlag is recorded for each detector for each event and is stored in the ROOT tree

- Pulse time cut

  - Removes events which are not within the defined "prompt-peak" time window

P.hgcer.adcPulseAmp

P.hgcer.adcPulseTimeRaw
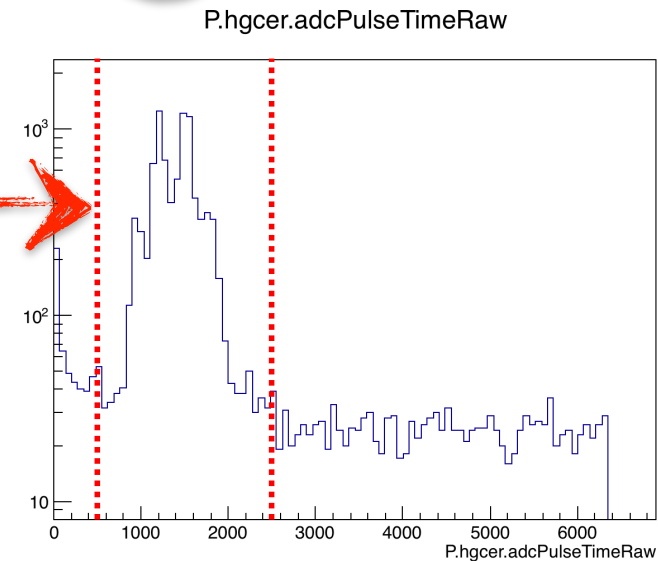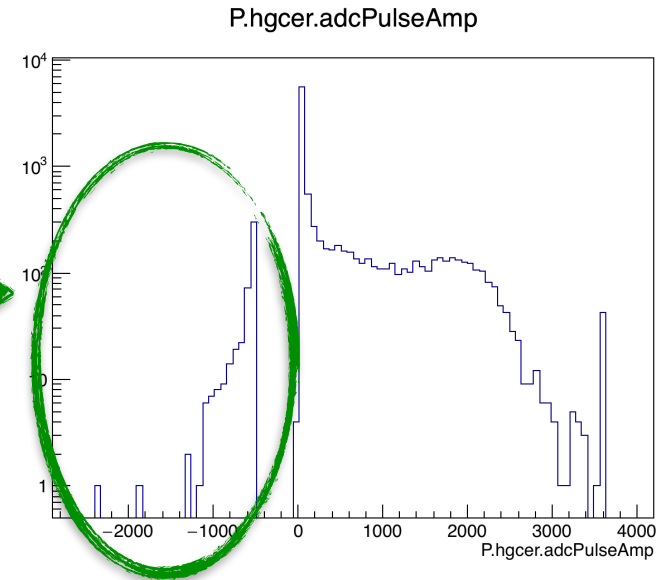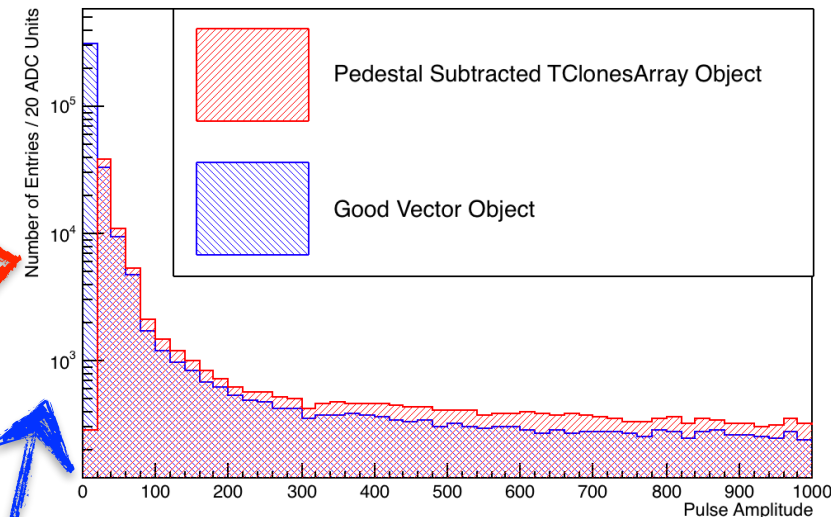
FADC250 Data Structures in HCANA

- Implementation of "Good" ADC & TDC Variables
  - vector <Double_t>
- Low-level fiducial event selection methods implemented to select best hits in each detector channel
- Currently present in all detector classes aside from the drift chambers
- Hodoscopes are only non-tracking detectors with TDC's

FADC250 Data Structures in HCANA

- "Raw" and "pedestal subtracted" ADC data are still constructed as TClonesArray objects

  - Sparsified scalar data objects

  - Only written to the ROOT tree if the "fDebugAdc" has been set to "true (1)"

- "Good" ADC & TDC data are constructed as unsparsified vector objects

SHMS Heavy Gas Cherenkov Good Pulse Amplitude

Pedestal Subtracted TClonesArray Object

Good Vector Object

SHMS Heavy Gas Cherenkov Good Pulse Amplitude

PMT 1
PMT 2
PMT 3
PMT 4
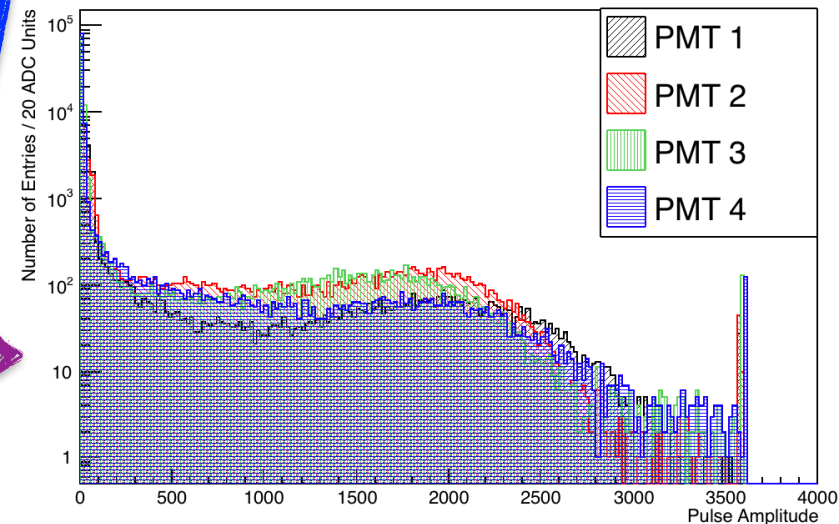
FADC250 Data Structures in HCANA

- Vector data objects can be histogrammed via. the "eye" variable in DEF-files

```
TH1F h1 P.hgcer.goodAdcPulseAmp[0]
TH1F h2 P.hgcer.goodAdcPulseAmp[1]
TH1F h3 P.hgcer.goodAdcPulseAmp[2]
TH1F h4 P.hgcer.goodAdcPulseAmp[3]
```

- The "eye" variable can have its index increased by an arbitrary integer amount

```
TH2F h1 [I+1] P.hgcer.npe
TH2F h2 [I+1] P.hgcer.goodAdcPed
TH2F h3 [I+1] P.hgcer.goodAdcPulseInt
```

- 2D histogram of scalars produces single scalar histogram

```
TH2F h1 P.hgcer.adcX P.hgcer.adcY
TH2F h2 P.hgcer.adcX P.hgcer.adcZ
TH2F h3 P.hgcer.adcY P.hgcer.adcZ
```

- 2D histogram of vectors produces vector of histograms

```
TH2F h1 P.hgcer.goodAdcX P.hgcer.goodAdcY
TH2F h2 P.hgcer.goodAdcX P.hgcer.goodAdcZ
TH2F h3 P.hgcer.goodAdcY P.hgcer.goodAdcZ
```

- Adding prefix "s" to 2D histogram of vectors produces single scalar histogram

```
sTH2F h1 P.hgcer.goodAdcX P.hgcer.goodAdcY
sTH2F h2 P.hgcer.goodAdcX P.hgcer.goodAdcZ
sTH2F h3 P.hgcer.goodAdcY P.hgcer.goodAdcZ
```
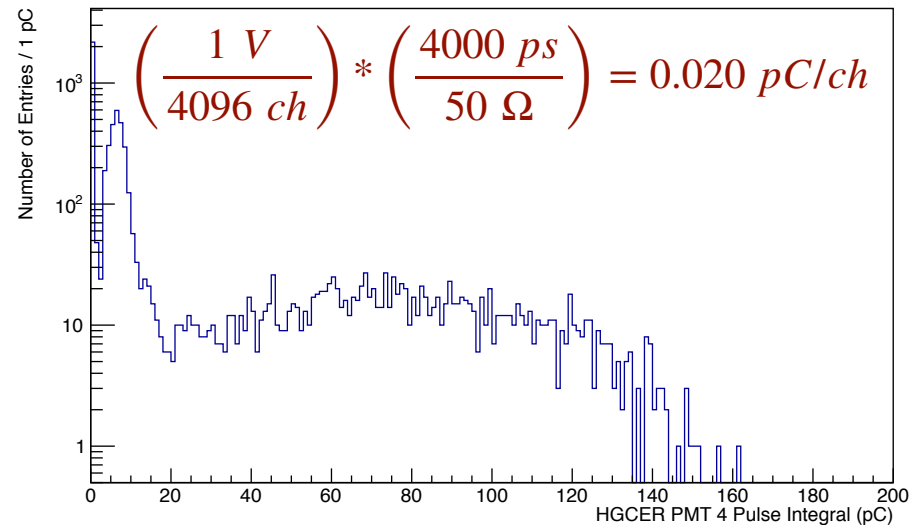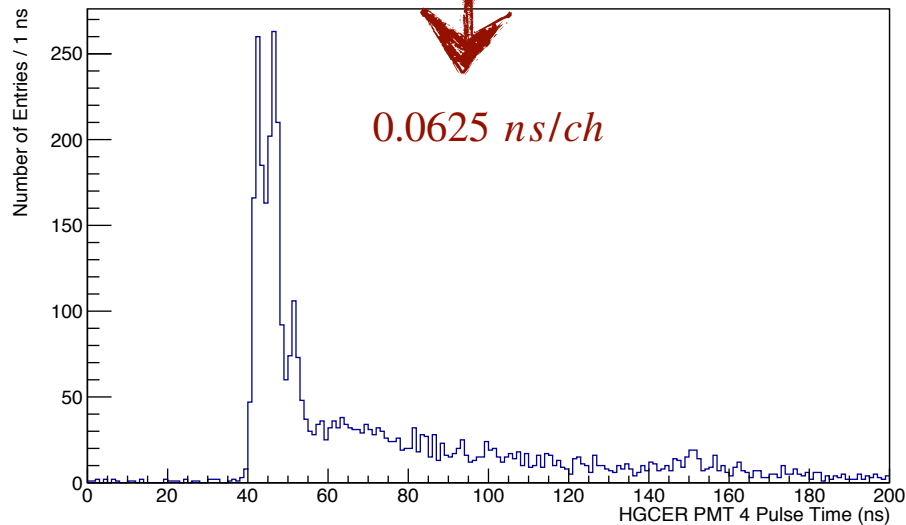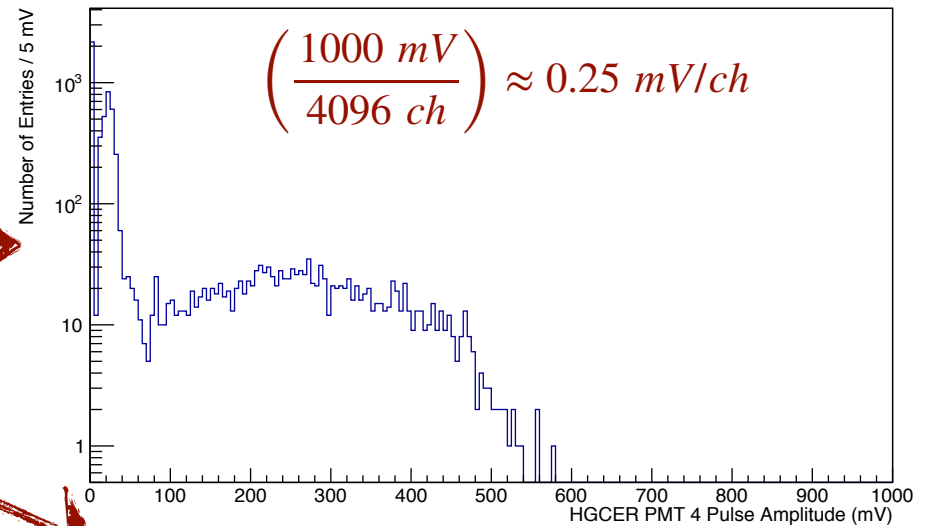
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FADC250 Data Structures in HCANA

- FADC data objects are reported in derived SI units instead of FADC channels

  - Amplitude → mV

  - Integral → pC

  - Time → ns

$$\left(\frac{1000\ mV}{4096\ ch} \right) \approx 0.25\ mV/ch$$

Number of Entries / 5 mV — HGCER PMT 4 Pulse Amplitude (mV)

$0.0625\ ns/ch$

Number of Entries / 1 ns — HGCER PMT 4 Pulse Time (ns)

$$\left(\frac{1\ V}{4096\ ch} \right) * \left(\frac{4000\ ps}{50\ \Omega} \right) = 0.020\ pC/ch$$

Number of Entries / 1 pC — HGCER PMT 4 Pulse Integral (pC)

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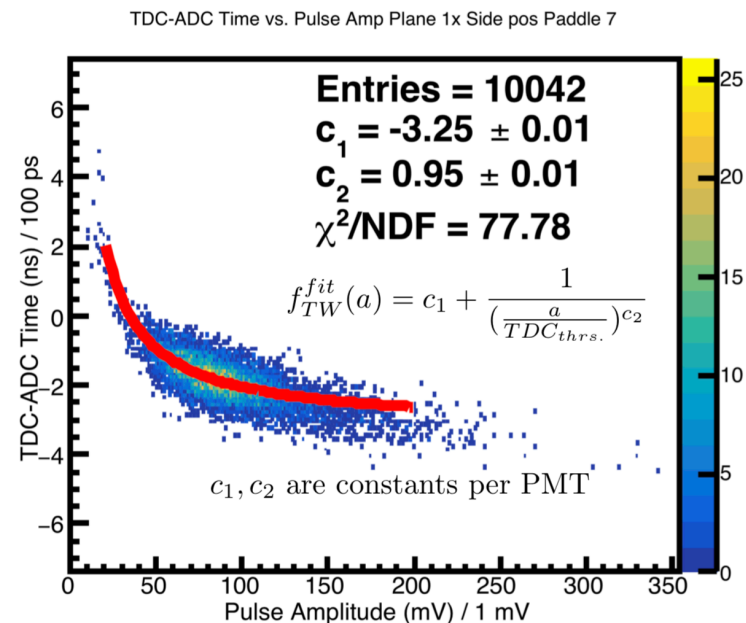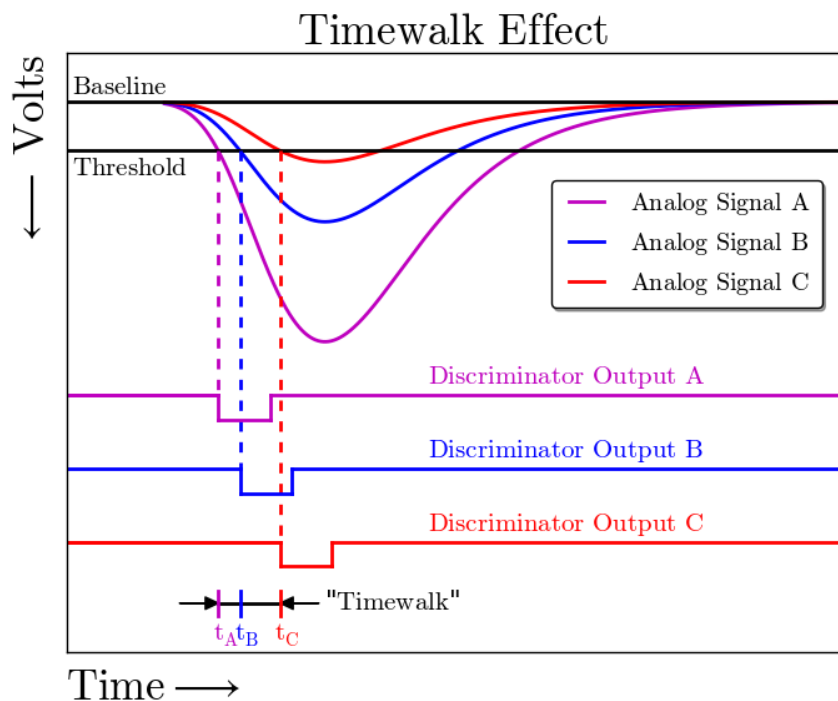
FADC250 Data Structures in HCANA

- FADC reference time present in all relevant ROC's

- A copy of the TDC reference time is fed into an RC circuit in order to smear out the NIM logic signal

- AdcPulseTimeRaw objects contain the raw FADC times

- AdcPulseTime objects are reference time subtracted via THcRawAdcHit class

- AdcTdcDiffTime objects are reference time subtracted FADC times minus the hodoscope start time
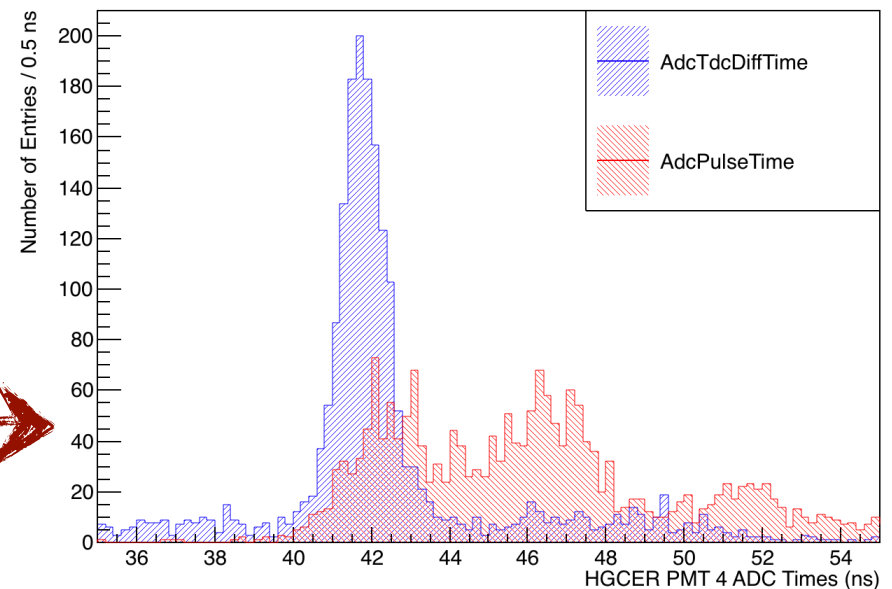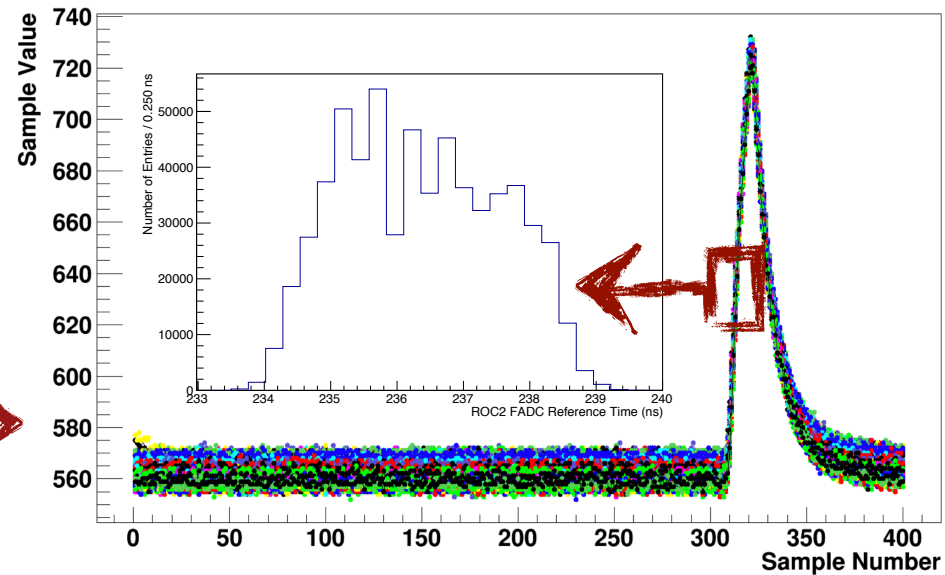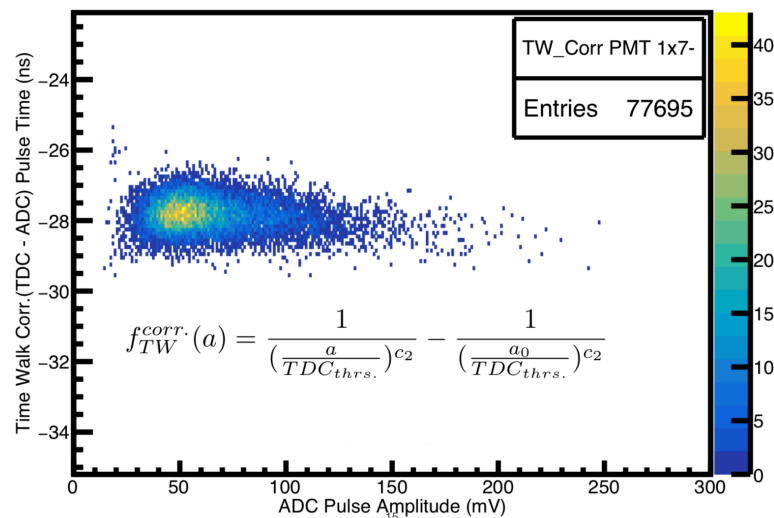
FADC250: Time-walk Calibrations

- For individual PMT's with both FADC and TDC readouts, time-walk corrections can be made on an individual basis

- High resolution, time-walk independent FADC time serves as self reference to time-walk dependent TDC time

Timewalk Effect

TDC-ADC Time vs. Pulse Amp Plane 1x Side pos Paddle 7

Entries = 10042
$c_1 = -3.25 \pm 0.01$
$c_2 = 0.95 \pm 0.01$
$\chi^2/NDF = 77.78$

$$f_{TW}^{fit}(a) = c_1 + \frac{1}{\left(\frac{a}{TDC_{thrs.}}\right)^{c_2}}$$

c_1, c_2 are constants per PMT

PMT 1x7-: Corr. (TDC - ADC) Pulse Time vs. ADC Pulse Amplitude

TW_Corr PMT 1x7-

Entries   77695

$$f_{TW}^{corr.}(a) = \frac{1}{\left(\frac{a}{TDC_{thrs.}}\right)^{c_2}} - \frac{1}{\left(\frac{a_0}{TDC_{thrs.}}\right)^{c_2}}$$

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FADC250: Clock Slippage

- FADC's modules with firmware version 0xC0D found to have their trigger times (internal 250 MHz clock) slip randomly by 4 ns with firmware present during fall 2017 and spring 2018 run

- Correction applied in **THcHitList::DecodeToHitList()** via of comparing trigger time provided by the TI module to the trigger time in each FADC module

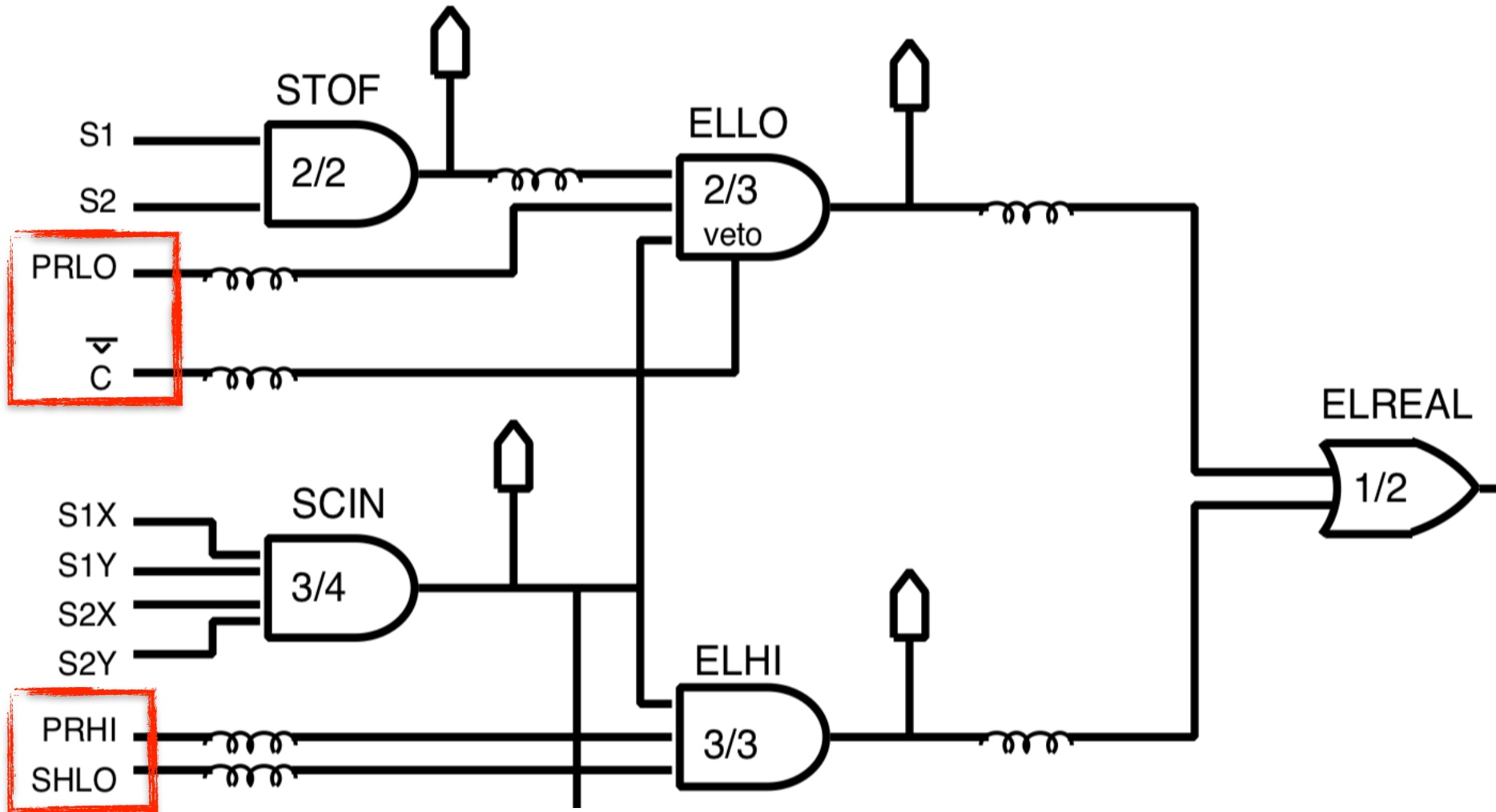- Addressed with firmware version 0xC0F

SHMS Defocused Run 1791 With No FADC Timing Corrections (Slot 3)
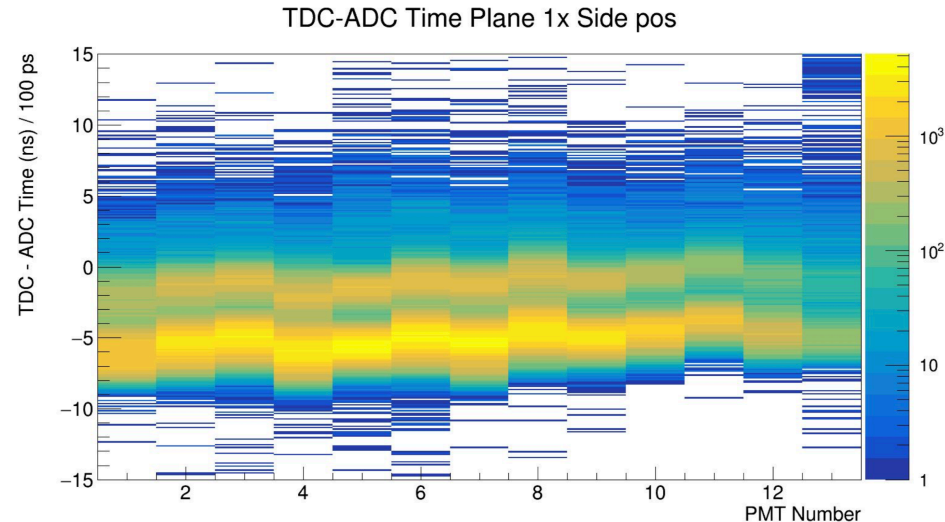
SHMS Defocused Run 1791 With FADC Timing Corrections (Slot 3)
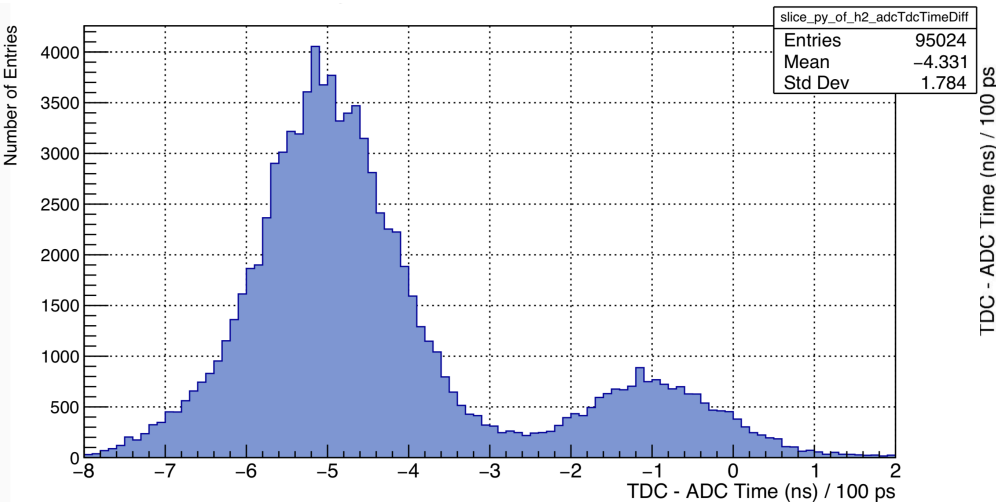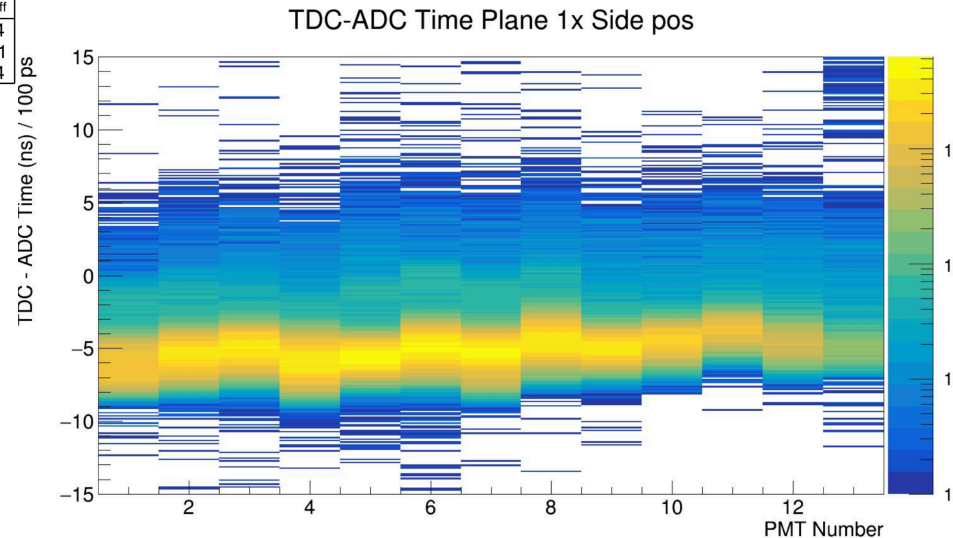
FADC250 Threshold Scans
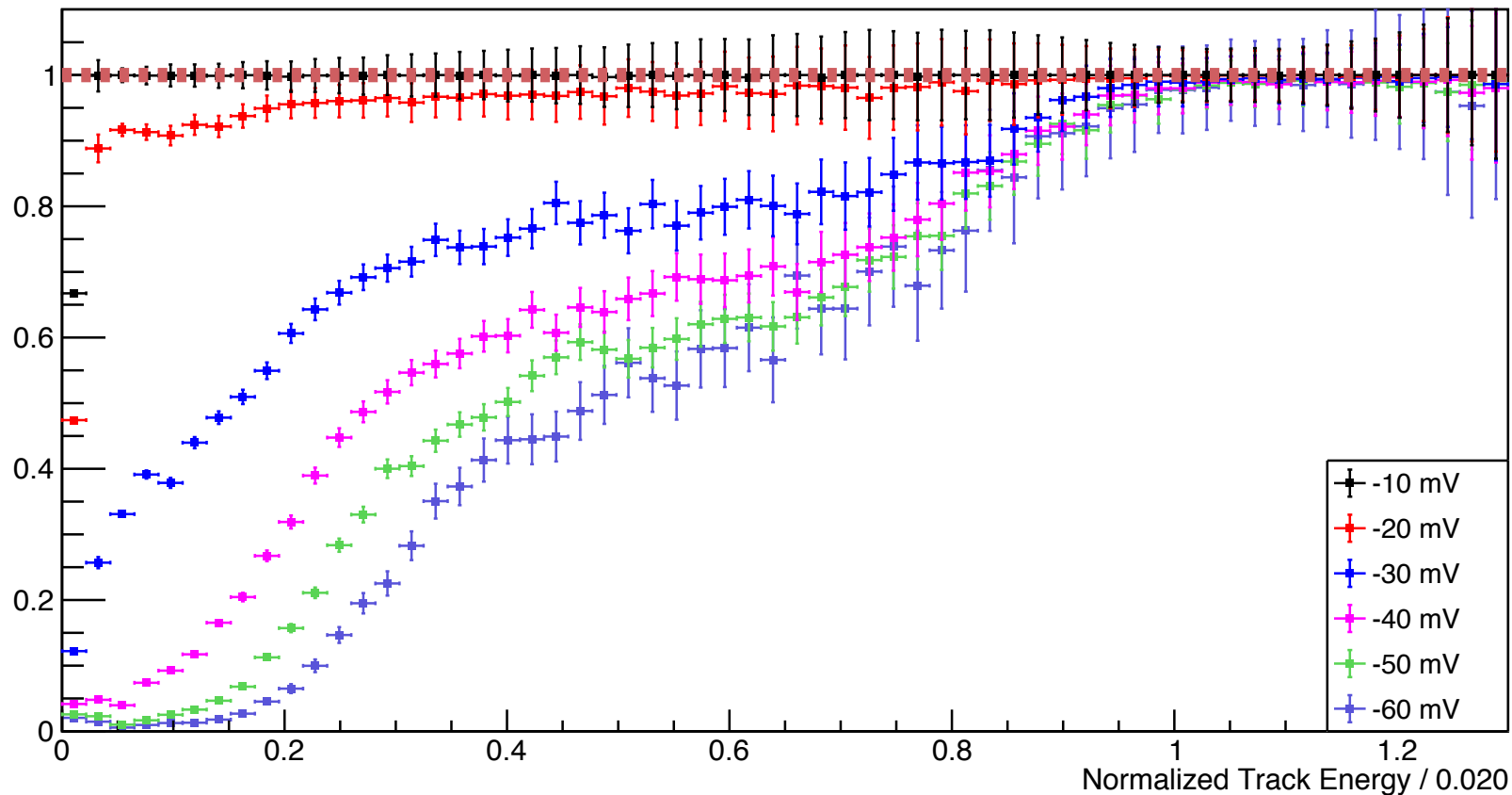
FADC250 Threshold Scans

- All trigger PID components reside in scalers, TDC's, and FADC's (where appropriate)

- One can study off-line the effects of imposing hardware discriminator threshold cuts via software cuts

- Consider an example for HMS:

  - E/P in calorimeter

  - Select pions via Cherenkov

  - Cut on PRHI TDC channel

  - Calculate ratio to determine appropriate threshold for pion suppression
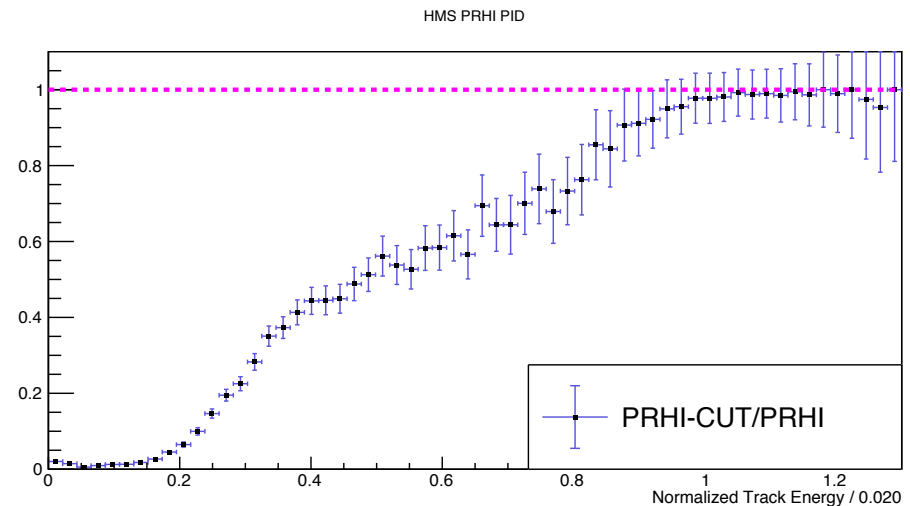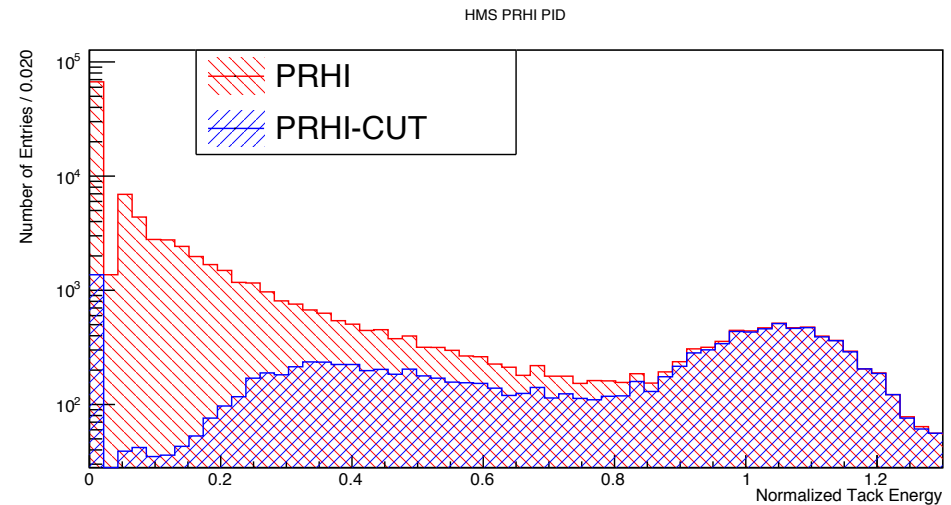
FADC250 Threshold Scans

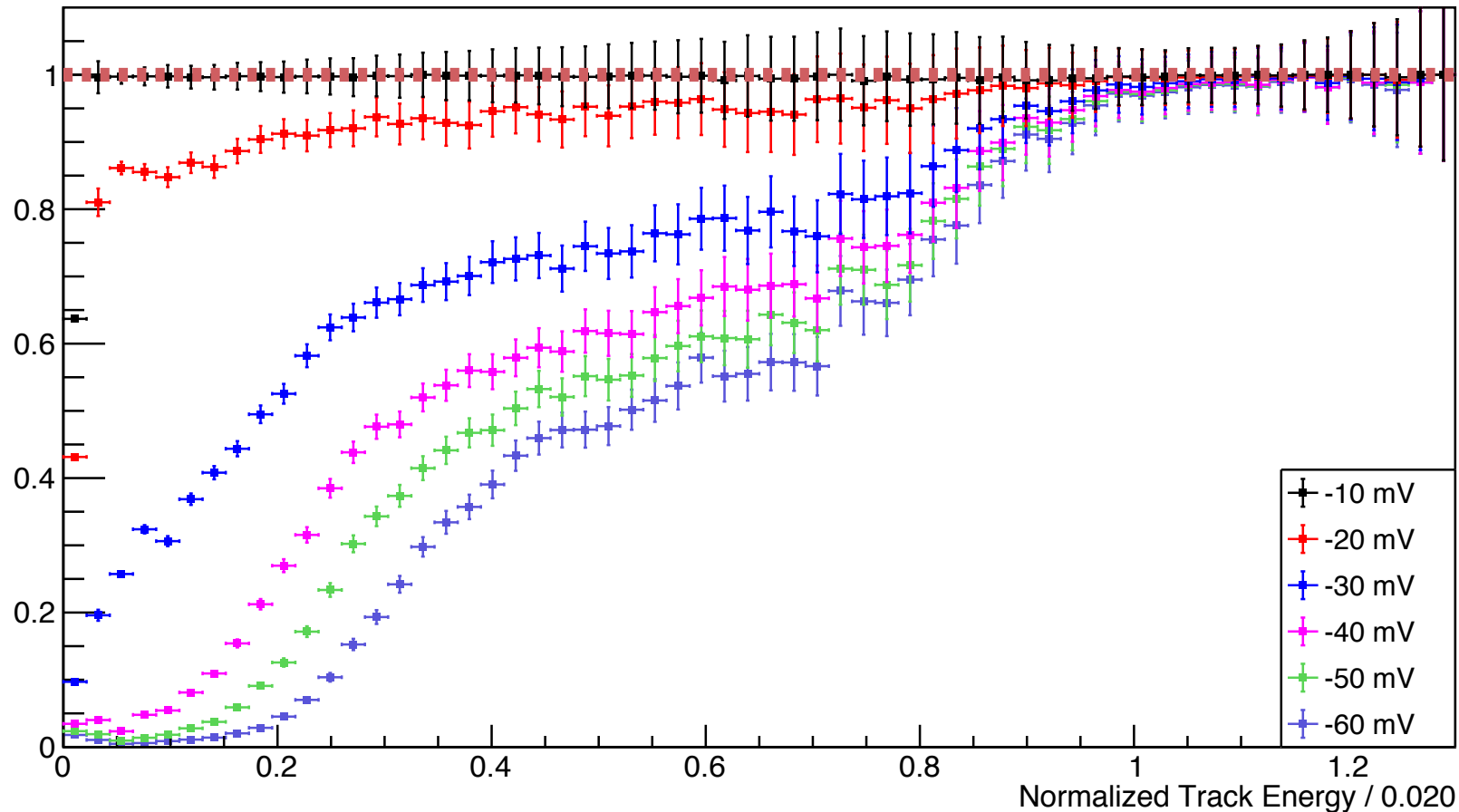- Perform hardware threshold scan of PRHI leg

HMS PRHI PID (NPE SUM = 0.0)

Slide Title

- Perform software threshold scan of PRHI leg

HMS PRHI PID (NPE SUM = 0.0)

Legend:
- -10 mV (black)
- -20 mV (red)
- -30 mV (blue)
- -40 mV (magenta)
- -50 mV (green)
- -60 mV (purple)

Normalized Track Energy / 0.020

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Questions?

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Backup Slides

Slide Title