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Data Acquisition for the Hall A High Resolution Spectrometers During 12 GeV

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Abstract

During the beginning of operations of 12 GeV beam, the data acquisition (DAQ) for measurements in Hall A will involve the two High Resolution spectrometers. This document provides detailed information on the DAQ for the two spectrometers, which includes miscellanous beamline detectors such as the beam position monitors, beam current monitors and raster. The common features of the detector package and associated DAQ of the two spectrometers and their distinctions are described. The last part is dedicated as a users guide to run the data acquisition software.

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1 Introduction

Hall A contains a nearly identical pair of magnetic spectrometers known as the high resolution spectrometers (HRS) [1]. For the reminder of this document, the two spectrometers will be referred to as HRS-L and HRS-R. The spectrometers transport charged particles in a small range of momenta and scattering angles to their respective detector packages. This document will discuss the details of the data acquisition system or DAQ during the 12-GeV era of beam operations. First a brief overview of the detector packages will be presented, followed by a discussion on the formation of the triggers, the hardware and software components of the DAQ, recording of scaler and slow-control information, and finally the HV controls.

2 Detector Overview

During 12-GeV running, the detector packages for the two spectrometers are almost identical and are optimized for electron detection, though aerogel Cherenkov detectors [2] and a RICH [3, 4] do exist for hadron detection. The configuration is shown in Fig. 1 for HRS-R.

A pair of vertical drift chambers (VDC) determine the particle trajectory for the target reconstruction and, coupled with the dipole, provides the momentum resolution. Then the particles pass through a pair of plastic scintillator planes, S0 and S2m [5], which can be used to form triggers for the data acquisition. Particle identification (PID) is provided by a gas Cherenkov sandwiched between the scintillator planes and a two-layer electromagnetic calorimeter. The only difference between the HRS-L and HRS-R packages is that in the second layer of HRS-R calorimeter, the blocks are oriented parallel to the particle tracks, whereas in the HRS-L calorimeter the blocks in the second layer are oriented perpendicular to the tracks as shown in Fig. 2.

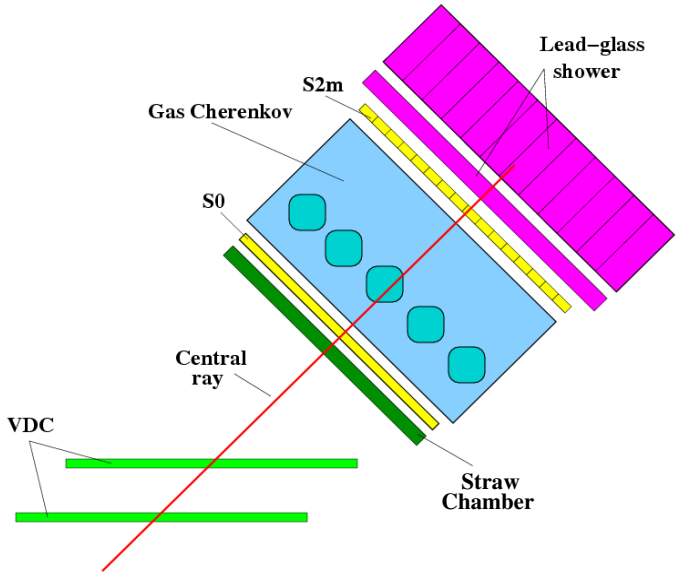

Figure 1: Detector package for HRS-R with three tracking chambers. The package for HRS-L is similar; however, the calorimeter blocks are arranged differently as shown in Fig. 2.

2.1 Straw Chambers

Additionally, one of the front straw chambers (SC) from the focal plane polarimeter has been added to both detector packages. The SC is an existing detector used several times in HRS-L. It is the only non-standard item in an otherwise traditional electron arm configuration. A gas flow system was added in the HRS-R to acommodate the straw chamber. By using this chamber, the plan is to resolve a long-standing problem of HRS tracking analysis whose efficiency of high-rate track reconstruction is less than 95% in spite of a high chamber efficiency of 99.5%.

Two major modifications have been made on the straw chamber detectors. First, the gas supply system was improved to ensure that there is enough gas flow for the SCs. Second, a modification of the low voltage power supply system was made to solve the problem of unstable signals.

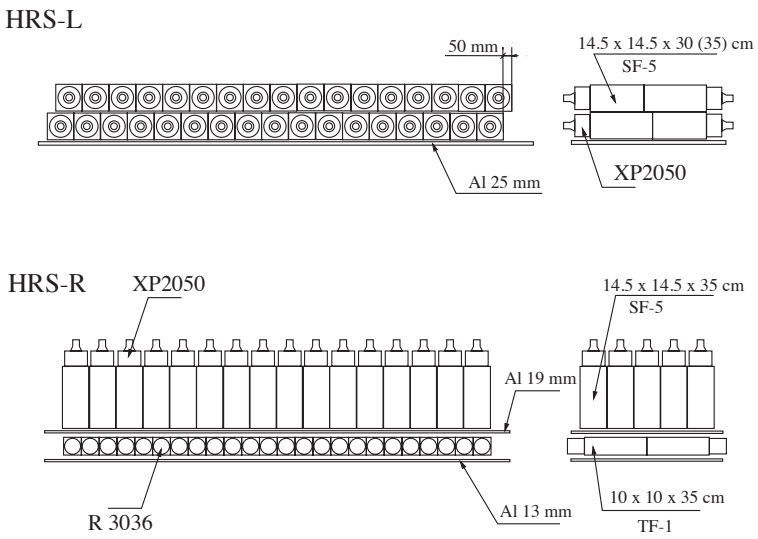

Figure 2: The electromagnetic calorimeter in the HRS-L (top) and HRS-R (bottom). Reproduced from [1].

2.2 VDC Electronics Upgrade

For the VDCs, the amplifier/discriminator (A/D) cards were replaced with those developed for the BigBite wire chambers [6]. The replacement cards use MAD chips, whose output stage works with LVDS signals, which produce significantly less feedback than ECL signals used in A/D cards by LeCroy Research Systems. This allows the VDCs to be operated at lower discriminator thresholds and lower high voltages. Currently, a HV of -3.5 kV was chosen based on the time resolution study, and the VDCs are operating with a threshold of 3.0 V for the A/D cards.

2.3 Scintillators

2.3.1 S2m Detectors

The S2m detectors [5] consist of 16 plastic scintillator paddles with a PMT located on each end of the bar. Each S2m signal is mixed with a logical pulse from an Electronic Dead Time Monitor (EDTM) module and sent to an ADC and TDC. Studies conducted on data taken during the March 2014 commissioning run with a liquid hydrogen target and using the GC and calorimeter as triggers show that the S2m detectors are greater than 99.4% efficient, covering the necessary acceptance range.

2.3.2 S0 Detectors

The S0 detectors consist of a single plastic scintillator paddle with a PMT at each end. S0 is attached to the frame of the GC detector, and located directly in front of the Cherenkov front window. The length of the paddle runs along the detector coordinate system x-axis.

The PMT analog signals are either sent to an ADC or mixed with a logical pulse from an EDTM module. The mixed signals are then sent to either a TDC or a coincidence unit.

2.4 Gas Cherenkov

The Gas Cherenkov (GC) detectors are mounted between the two scintillator planes and are filled with CO_2 at atmospheric pressure. For the front SC to fit into the HRS-L detector stack, the gas Cherenkov extension box was shortened by 10 cm, providing a pathlength of 120 cm in the gas radiator. The pathlength for the HRS-R detector remains at 130 cm. Thinner aluminum windows have been installed on the detectors. The detectors contain ten concave mirrors and each has been aligned to focus light onto a specific PMT. Ten PMTs are installed on each detector with ET 9390KB PMTs on the HRS-L and Photonis XP4572B on the HRS-R. A wavelength-shifting (WLS) paint has been applied to all twenty PMTs.

The high-voltage is applied to the PMTs so that the single-photoelectron peak is at approximately ADC channel 100. The amplified analog signal from each PMT, as well as the analog sum, is mixed with a logical pulse from an EDTM module. The mixed signals are sent to discriminators and then proceed to TDCs. The GC logical sum is sent to a trigger module based on Versa Module Europa (VME) programmable logic.

Analysis conducted on data taken during the March 2014 commissioning run show 15−20 photoelectrons produced for electron events that are fully contained on an individual PMT coated with WLS paint. Electron detection efficiencies on the HRS-L are greater than 99.5% and cover the necessary acceptance range. The results with WLS paint have been submitted for publication.

2.5 Electromagnetic Calorimeters

As shown in fig. 2, there are two layers of lead glass blocks in each HRS for separation of electrons from heavier particles such as pions and protons. For the HRS-L calorimeter, the total thickness encountered by electrons is 11.8 radiation lengths. On HRS-R, the total thickness is 17.4 radiation lengths, which results in a better energy resolution than that of the pion rejectors on the left arm.

Additional details of the status and upgrades of the HRS detectors are discussed in Ref. [7].

3 Discriminator Thresholds

Table 1 lists the discriminator threholds for the individual detector channels as well as the threholds for the summations of the Gas Cherenkov and calorimeters. The summation signals are used as the triggers for these detectors as will be discussed in the following section.

Detector	Threshold
VDCs	3.0 V
Straw chambers	3.0 V
S0	−15 mV
S2m	−10 mV
GC (individual channels)	−15 mV
GC sum	−10 mV
Calorimeter sums	−20 mV

Table 1: The discriminator thresholds associated with each HRS detector.

4 Triggers

In this section, the classification of trigger types will be discussed. There are two main types: those formed from detectors and those from pulsers.

4.1 Triggers Formed from Detectors

The various detectors in the Hall A spectrometers can be used to form logic signals to trigger the DAQ. From these base triggers, coincidence triggers can also be created among the detectors. Some of these will be discussed in Section 4.3.

4.1.1 Scintillator Triggers

The S0 and S2m scintillator planes are installed inside the HRS detector huts. The S0 scintillator is a single paddle with a PMT on each end, whereas the S2m detector consists of 16 paddles with one PMT on both ends. As shown in Fig. 3, the S2m signals travel through a mixer circuit with one-sixth of the signal amplitude going to an ADC and the remaining signal into a discriminator. The thresholds on the discriminators are set to −10 mV. From the discriminators, the signals from each side of the detector form an "OR" of the signals. Finally, the left and right-side "OR"s are then anded together to form the S2m trigger. Copies of the individual discriminated signals are also sent into a FASTBUS TDC and a VME scaler.

In the bottom of Fig. 4, the S0 trigger is formed in a similar way, but the two PMT signals are first sent into an amplifier module (10x amplification) prior to discrimination and formation of the S0 trigger.

4.1.2 Gas Cherenkov Trigger

The trigger for the Gas Cherenkov detector involves the ten PMT signals also being sent through an amplifier prior to discrimination as seen in Fig. 4. However, the trigger is formed by sending the pulses into a linear fan-in/fan-out module to produce a sum of the signals.

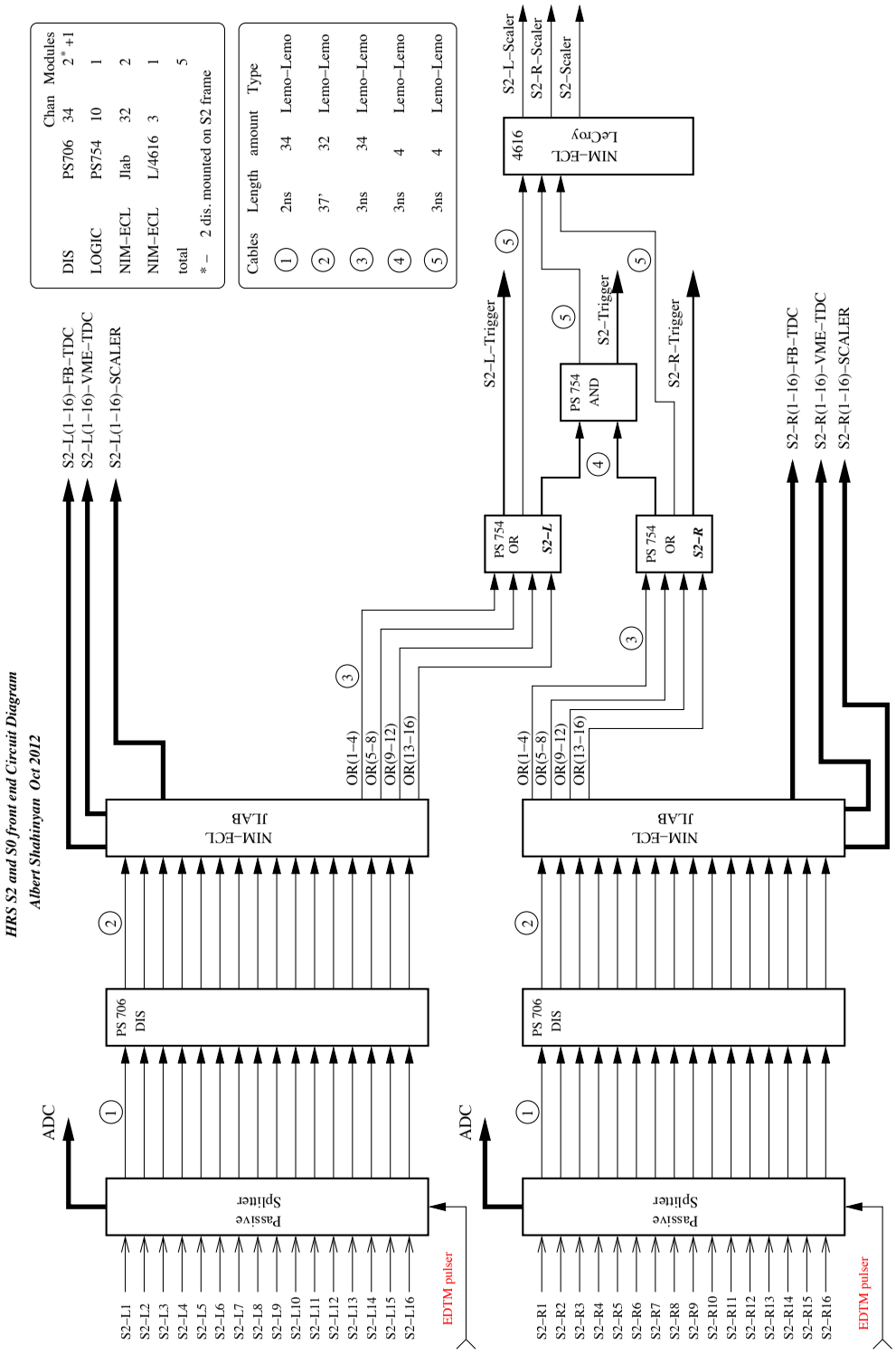

Figure 3: Schematics for the S2m trigger formation.

The PMT signals are grouped into groups of 4, 4 and 2, which are then combined into one sum to form the trigger for this detector.

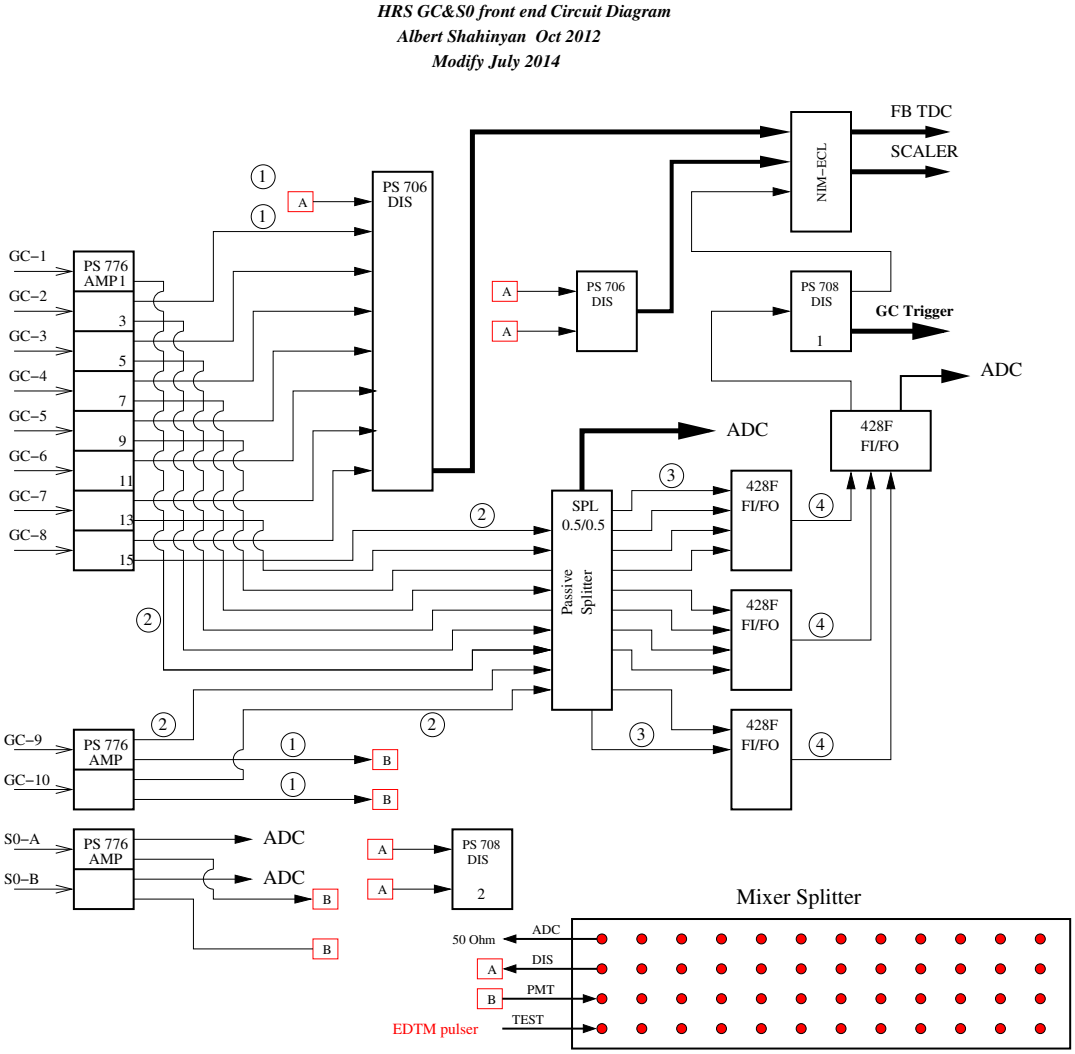

Figure 4: Schematics for the formation of the Gas Cherenkov and S0 triggers.

4.1.3 Calorimeter Trigger

The calorimeter triggers for the L-HRS and R-HRS are created in a similar procedure by first forming the detector sum for each layer and the summation for the two layers together as illustrated in Figs. 5 and 6, respectively. The summing modules contain eight inputs from one layer of the calorimeter. The sums from the modules are then passed through a linear fan-in/fan-out to form the summation for that layer. Once the summation for each layer is formed, the calorimeter trigger for the entire detector is created.

The Gas Cherenkov and calorimeter triggers are passed through a discriminator prior to being sent to the rest of the DAQ system, which involves the TDCs and scalers. The undiscriminated analog signasl from the summing modules are carried to ADCs.

4.2 Pulser Triggers

The pulser triggers are primarily used as clocks and aid in the verification of synchronization between the DAQ crates. There are two primary clocks: the 1024 Hz and 104 kHz (fast clock). The 1024 Hz clocks originates from a NIM module on the R-HRS, whereas the fast clock is produced from a VME module on the L-HRS. The slower clock provides the time to calculate scaler rates, and the fast clock is used to check the crate synchronization, especially when the DAQ is in buffered mode. Typically only the 1024 Hz clock is included as a trigger to the DAQ.

4.3 Majority Logic Unit

Once the triggers from the detectors are formed, more sophisticated triggers between the detectors can be created. On the two spectrometers, this is accomplished using a CAEN 1495 VME board as a Majority Logic Unit (MLU).

In Fig. 7, the input signals are arranged in the section labeled as 'E' (NIM inputs) with channel 1 at the bottom. The corresponding channel inputs are as follows:

1. S0 trigger
2. S2m trigger
3. Gas Cherenkov (GC) trigger
4. Shower (SH) trigger
5. Electronic Dead time Monitor (EDTM) signal
6. Clock.

The module has two output sections labeled 'C' and 'F', where section C contains 32 LVDS outputs and section F contains 8 NIM outputs. The outputs are arranged so that C(1-8), C(9-16), C(17-23), C(24-32), and F(1-8) are identical, and provide 5 copies of the programmable output signals.

The programming for the MLUs is separately set up by two VME-based IntelPCs on the HRS-L and HRS-R. At present there are two programmable configurations: "GMp Standard Triggers" and "Single Detector Triggers" as shown in Tables 2 and 3, respectively. For the single detector triggers, output channel 5 is historically referred to as the "2 out-of 3" trigger to measure the trigger efficiency.

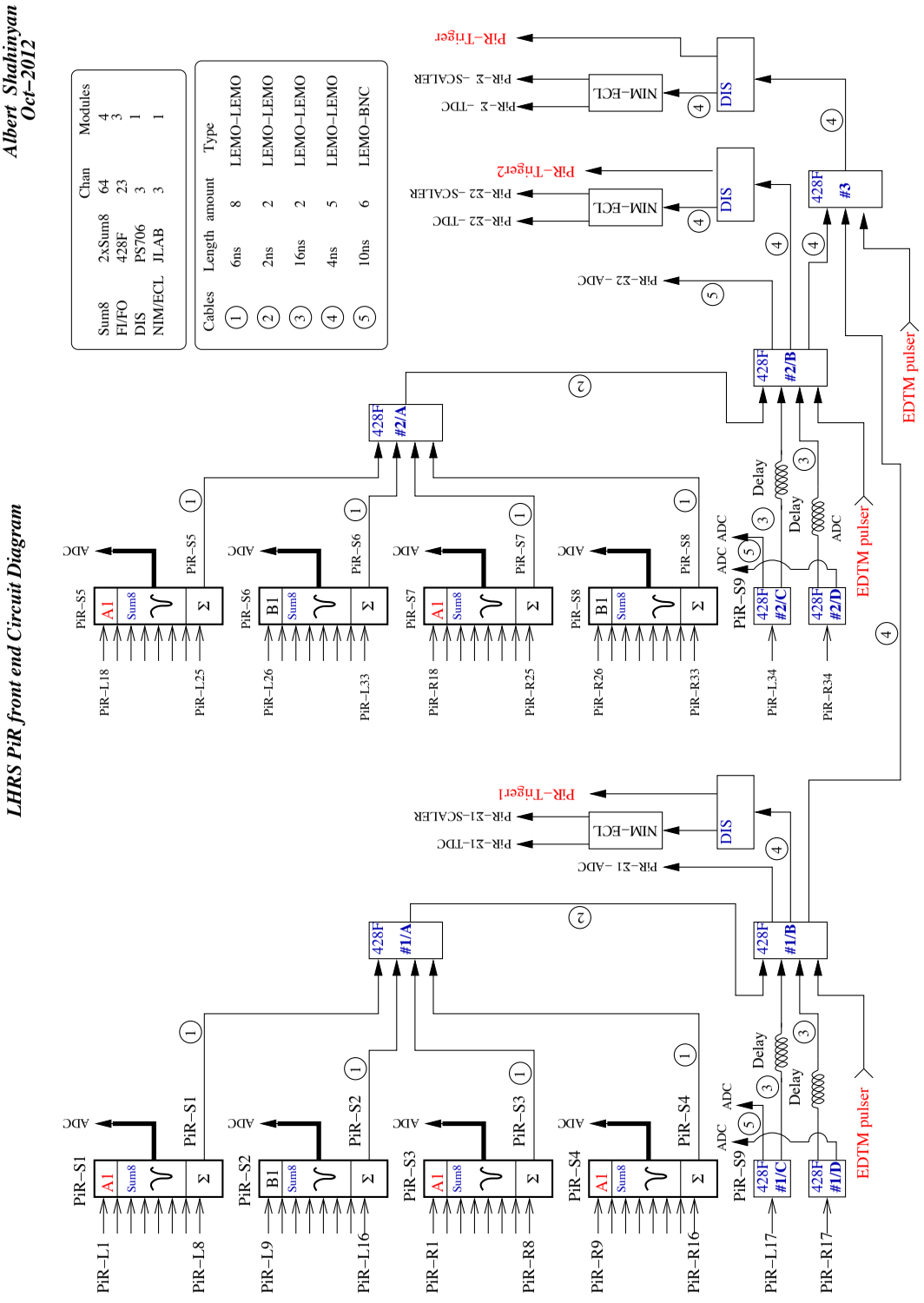

Figure 5: Schematics for the L-HRS calorimeter trigger.

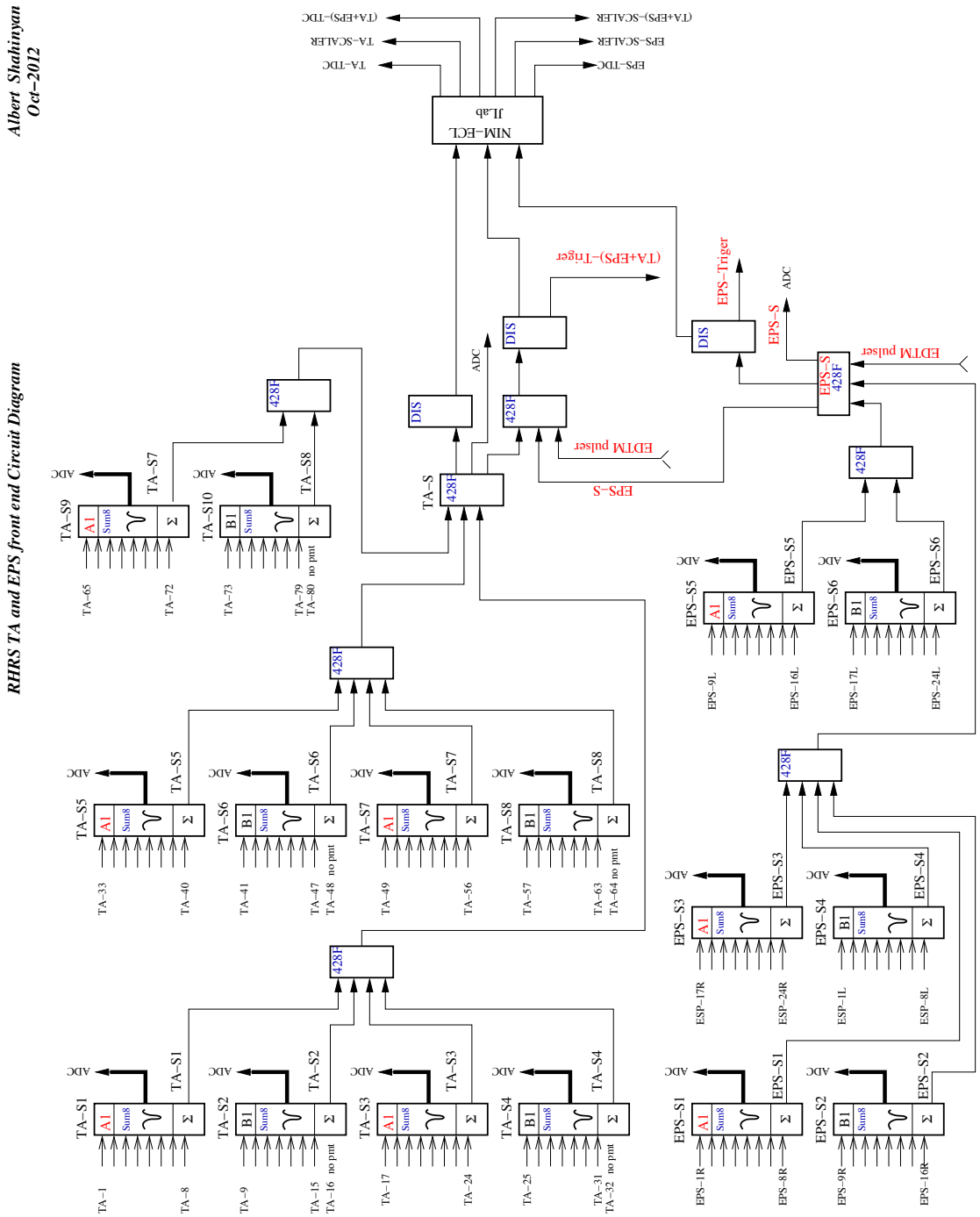

Figure 6: Schematics for the R-HRS calorimeter trigger.

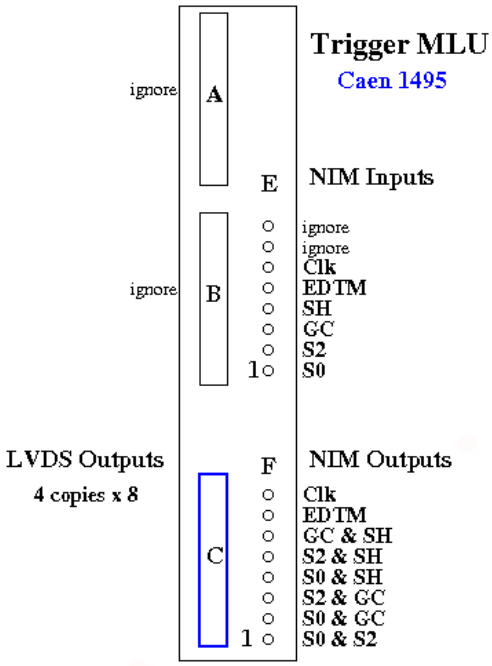

Figure 7: Diagram of the front panel input and output channels for the CAEN 1495. Reproduced from [8].

Channel	Output Signals
1	S0 & S2m (logical "and")
2	S0 & GC
3	S2m & GC
4	S0 & SH
5	S2m & SH
6	GC & SH
7	EDTM
8	Clock

Table 2: MLU configuration for the GMp standard triggers.

Channel	Output Signals
1	S0
2	S2m
3	GC
4	SH
5	(S0 & S2m) ‖ (S0 & GC) ‖ (S2m & GC)
6	GC & SH
7	EDTM
8	Clock

Table 3: MLU configuration for the single detector triggers.

4.3.1 MLU GUI

A new graphical user interface (GUI) has been written to control the programming for the MLU as shown in Fig. 8. The HRS-L and HRS-R have separate controls, which currently support choosing between the GMp Standard and Single Detector triggers. The GUI also features a "HELP" button for more information on its use. Instructions on where and how to run the interface can be found at Ref. [8].

5 Data Acquisition

The Hall A DAQ is CODA [9] (CEBAF online data acquisition) based using version 2.6.2 of the software. This software is used to build events from the various hardware components, which include FASTBUS and VME crates with ADC, TDC and scaler modules to digitize the signals from the various detectors. The triggers, which were discussed in the previous section, are formed using standard NIM modules for discrimination and logic. The scalers are implemented with VME based modules and their readout are also controlled by the CODA software. Compared to earlier running in Hall A, the DAQ is primarily the same, except

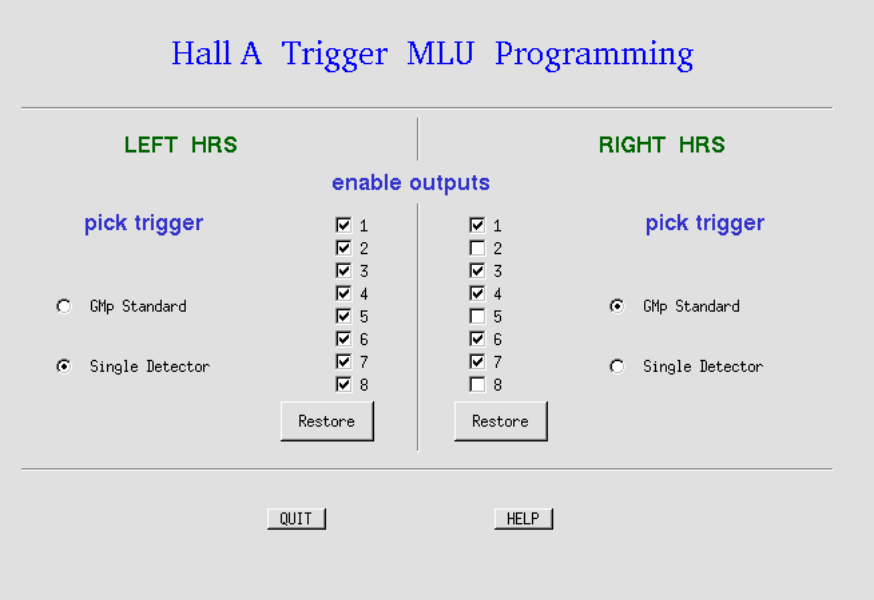

Figure 8: GUI for control of the MLU board. Reproduced from [8].

the old CAMAC modules were replaced with NIM modules. This transition was relatively minor, since a large part of the DAQ already included NIM electronics. In addition, EPICS information related to various instrumentation in Hall A and related to the accelerator is inserted into the datastream every 10 to 30 seconds.

5.1 Hardware Crates

For the two Hall A spectrometers, the detector signals are recorded in FASTBUS or VME modules, which are housed in hardware crates. Traditionally, these crates are referred as Read-Out controllers (ROCs), which in CODA are assigned a unique identification number. The ROC is actually a software routine that runs in a CPU housed in the same crate as the digitizing electronics. Data are collected in parallel by assembling event fragments from the ROCs. Figure 9 shows a typical DAQ system and the flow of information among the various components. Currently on each spectrometer, there are three FASTBUS crates and one VME crate read out by CODA for standard running; their names are listed in Table 4.

The FASTBUS crates host a number of LeCroy 1881/1881M ADCs and LeCory 1877S TDCs. Spreading the modules out among the three crates aids in reducing the read-out time, which increases the ceiling for the maximum DAQ rate while keeping a reasonable dead time. Communication and control over the crates is accomplished with a Motorola MVME CPU module. Additionally, a scaler module is also incorporated into each crate to record a copy of the fast clock and other important signals required by the running experiment.

The two VME crates are commonly referred to as the Trigger Supervisor (TS) crates. The crates have two sections: one for 6U cards and another for 9U modules. These crates contain scaler modules from either CAEN, LeCroy or Struck Innovative Systeme (SIS). As

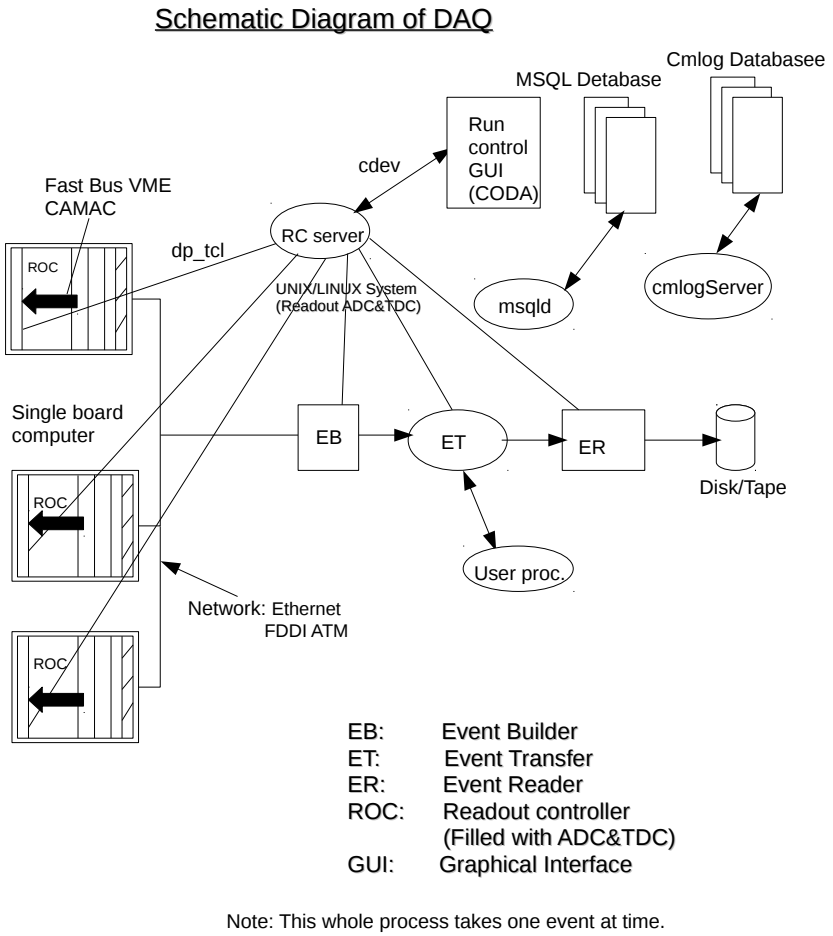

Figure 9: A block diagram of a typical DAQ system based on CODA. After accepting hits from the detectors, the crates are readout by ROCs, running either the VxWorks kernel or UNIX. The information from the ROCs are then passed to an Event Builder (EB). The EB collects event fragments from all ROCs and then orders and merges the pieces of information into a single data structure in the CODA format. These events are then transferred to the Event Transport (ET) system. From the ET, the events are gathered by the Event Recorder (ER), which writes them to permanent storage. Reproduced from Ref. [10].

Crate Type	L-HRS	Rack	R-HRS	Rack
VME	TS11	HRSH_RR3	TS0	HRSE_RR3
FASTBUS	ROC3	HRSH_RR4	ROC1	HRSE_RR4
FASTBUS	ROC4	HRSH_RR4	ROC2	HRSE_RR4
FASTBUS	ROC5	HRSH_RR4	ROC6	HRSE_RR4

Table 4: The list of crates associated with the L-HRS and R-HRS, including their electronics rack location in the detector stack.

with the FASTBUS crates, communication and control is accomplished with a Motorola CPU. The 9U section of the TS crate hosts the Trigger Supervisor version 2 module (TS2) and the Transition Module (TM).

Figure 10 shows a flow chart of the trigger system starting from the MLU at the top of the diagram through the trigger supervisor, which eventually leads to the formation of the ADC gates and TDC stops. The TS2 and TM modules along with the processing of the triggers are discussed in the following subsections.

5.2 Trigger Supervisor and Trigger Interface

The Trigger Supervisor system provides the link between the triggering system and the ROCs. This system includes a TS2 module and a individual interface card for each crate. Hence, the TS2 behaves as the central control point for the DAQ. This module can accept and prescale several distinct triggers, while maintaining system busy during the time an accepted trigger is being processed. The module also provides signals for timing and gating of the front-end electronics, which will be further discussed in Section 5.3. Finally the module counts the number of events in the front-end module buffers and communicates information to the ROCs via a parallel link to the ROC interface cards.

The TS crates make use of a VME Trigger Interface (TI) module, which enables the VME ROC to have access to trigger information. This module can accept triggers either from the TS2 module or external triggers. The TS mode is the normal running condition in Hall A with multiple ROC systems. In this mode, the TI module allows the VME ROC to execute the procedure of maintaining the read-out sequence of the various components. Each FASTBUS crate contains a "CEABF SFI Auxiliary Card" in its backplane, which connects with the TS2 module.

The TS2 module supports up to 32 ROCs on four separate ROC branches. Each of these branches contains a FIFO 8-deep memory buffer, buffer counter, and read sequencer. For each branch, an external cable links up to a maximum of 8 ROC interface cards, which transmits the event type and two status flags.

5.3 Level-One-Accept, Retiming, ADC Gates and Common Stops

The TS2 can accept twelve separate *Level 1 Trigger* inputs simultanesouly. Of these inputs, four can be prescaled by 24-bit factors (triggers 1–4), and an additional four can be prescaled

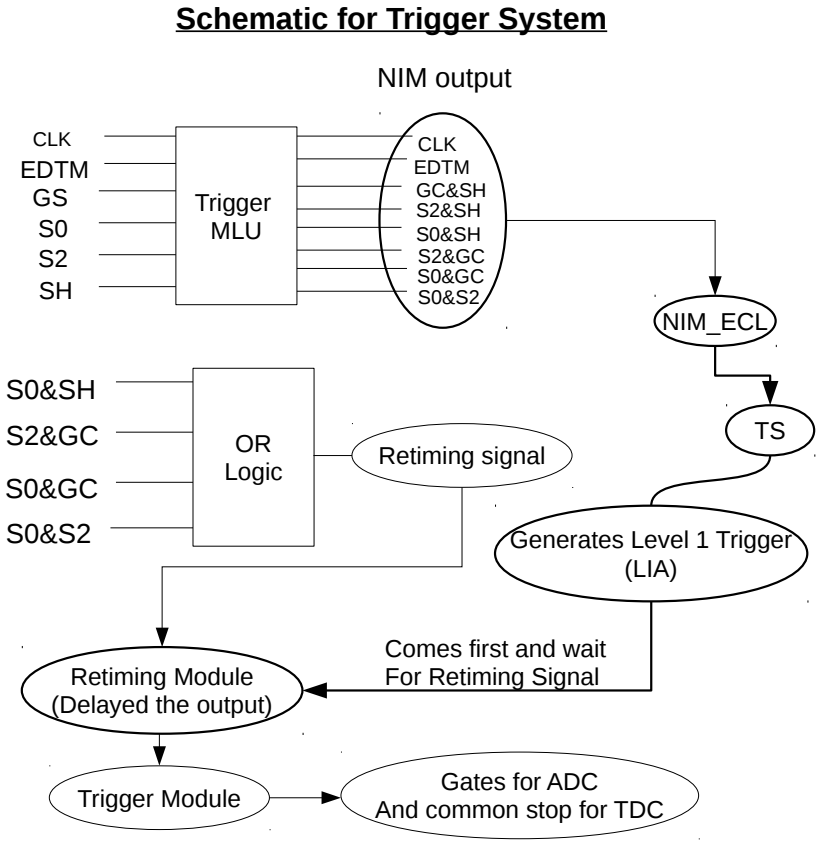

Figure 10: The triggers from the MLU module are input to the TS via a NIM-ECL level-translator. When a trigger is accepted by the TS, a level one-accept (L1A) signal is generated. The L1A and the retiming signals are then sent to a retiming module where they form a coincidence. Then this coincidence signal is fed to the TM module where copies of an ADC gate, TDC start/stop, and scaler gate are generated. These are then distributed to the front end electronics on the FASTBUS and VME crates, where ADCs, TDCs and scalers begin to record data once these signals arrive. Reproduced from Ref. [10].

by 16-bit factors (triggers 5–8). The remaining four triggers cannot be prescaled. It is also possible to disable individual inputs within the TS. When the module is ready to accept triggers, an input trigger will latch up the TS, and any triggers that occur on any of the twelve input channels are latched during this time period. The input triggers are used to generate a pattern of *Level 1 Accept* (L1A) signals, which have a precise time relationship to the input trigger. The L1A signals are used by external electronics to create ADC gates and TDC starts/stops.

A "trigger bit pattern" for accepted events is stored in an FIFO on the TS2 module and provides the pattern of triggers which co-exist for a given event. This bit pattern is sent to a 1877 TDC with one trigger on each of 12 channels and each channel containing a separate trigger **after** prescaling. As an example, if a T5 trigger is accompanied by a T3 trigger, which survived prescaling, one would see a signal on the third and fifth channels with the appropriate timing. During analysis, the Hall A analyzer [11] parses the data from the TDC, and provides the bit pattern for each event.

The latched trigger pattern can be programmed as one of three possible classes: Class 1, Class 2, or Class 3. In Hall A, typically only Class 1 is used, which does not require a higher-level trigger decision to read out the event.

5.3.1 The Transition and Re-timing Modules

The Transition Module (TM) provides a useful interface between the TS2 and front-end electronics. This module generates and distributes ADC gates, TDC starts/stops, and various control signals to the crates. In Hall A, there are two modes of operation for the TM module: either independent or paired mode. In *independent mode*, the gates and common stops are created independently for each spectrometer. These are generated from the L1A signal of the local TS. In *paired mode*, which is needed for coincidence experiments, the trigger system of one arm is in control of both spectrometer arms. The TM has been designed to allow for ease of switching between the two modes.

When the spectrometers are used in independent mode, the TM is set to be in LOCAL mode, where the local TS provides the L1A signal. The L1A signal could be taken directly from the TS2 module to form the stops and gates, but typically this signal is retimed relative to one or more detector signals from the local trigger logic. When implemented, the timing of the gates and stops is set by local detector signals in coincidence with the L1A signal. Here the detector signal's leading edge must occur within a time window that is started by the L1A's leading edge. As a precaution, if a detector signal does not occur within the time window, the L1A is retimed on a delayed copy of itself with the use a retiming (RT) module contained inside the TS crate.

5.3.2 Hall A Implementation of Re-timing

In Hall A, the L1A signal is taken directly from the TS2 module to the RT module. The retiming signal, commonly referred to as the strobe, is also sent to the RT module. The stobe has to be delayed with-respect-to the L1A so that it occurs within the time window of the L1A. Typically, this delay is chosen to be about 60 ns after the L1A window opens,

and for most of the previous experiments in Hall A, the strobe was the "OR" between the S1 [1] and S2m detector signals, see Section 4.1.1.

In the 12-GeV era of running experiments, the strobe will now be the "OR" between different combinations of the S0, S2m, GC and SH detector signals. Clearly, the strobe signal can be customized depending on the requirements for a given experiment and is expected to change between experiments. The re-timed L1A signal is then sent from the RT module to an L1A input on the TM. The TM provides various copies of the gates for ADCs and common stops for TDCs. The width of the gates and stops can be independently adjusted, though all the gates have the same width, and likewise the stops have a shared pulse width. For the initial experiments after the upgrade, the gate width is 100 ns; whereas, the common stop length is 1.5 μs. The ADC that digitizes the BPM and raster information must have a shorter gate width due to the voltage size of these signals. This particular ADC is sent a separate gate that is only 50 ns wide to avoid saturating the ADC.

5.4 Event Types

In Hall A, event types less than 15 are physics triggers of various types; see Section 4. The CODA transitions of prestart, go, and end are also treated as separate events. Event types greater than 99 are referred to as *special events*. These events are data inserted into the CODA datastream, which are meaningful to record with the physics events. Table 5 provides the *special events* that exist.

Event Type	Format	Description
100	integer	Last scaler reading
120	integer	Prescale registers from TS
131	character	EPICS Data
133	character	Prescale Factors
135	character	ESPACE Detector Map
136	character	Trigger Setup
140	integer	Scaler Data

Table 5: The list of *special* event types used either previously or currently in Hall A.

5.5 DAQ Live time/Dead time

When the event rate is high, the DAQ system is unable to record all the events. The fraction of events recorded by the DAQ is represented by a quantity called the live time (LT) or dead time ($DT = 1 - LT$). Dead Time results mostly from computer data processing and can be decreased by prescaling the events with a prescale factor (ps) at the TS; for every ps events, only one is sent to the DAQ system. Electronic dead time is also present due to the response of the detectors. However at rates below 1 MHz, the electronic contribution is small compared to the computer dead time.

The live time is event type and helicity dependent and is determined by dividing the total number of triggers accepted by the DAQ system $T_i^{\rm acc}$ by the number of triggers T_i recorded by scalers:

$$LT_i^{\pm} = \frac{ps_i T_i^{\rm acc,\pm}}{T_i}, \tag{1}$$

where i is the event type, ps_i is the prescale factor for event type i and $\pm$ denotes the helicity of the electron beam.

The main reason the trigger bit pattern as discussed in Section 5.3 is important is that it affects the calculation of dead time. The online calculation does not have available the information on how many triggers of each event type were accepted, so an estimate of the dead time for online display is determined by accounting for correlations among the triggers. As an example, if trigger T5 is defined as the coincidence between triggers T1 and T3, then every T5 is also a T1 and a T3. Offline, it is easy to calculate the trigger-specific dead time using the bit pattern.

5.5.1 Electronic Dead Time Monitor

The electronic dead time will also be monitored by sending a well-defined, distinct pulse into the trigger's front-end. Copies of the pulser signals are mixed in with the signals of the S2, S0, and GC detectors. If the DAQ is not busy, this trigger will be accepted and show up in the datastream as an event. The fraction of events that are lost is the dead time correction. The pulse is also sent to both a TDC and scaler so that the pulses can be tagged separately from triggers generated by the detectors.

Figure 11 illustrates the passive splitter circuit diagram for the S2m detectors. A VME flexio module with 32 outputs is driven by a pulser at the rate of 5−10 Hz. Each output can also be turned on and off individually. The mixer circuit produces a mixed output signal, which consists of a NIM logical standard pulser signal for each S2m PMT signal. These mixed signals then proceed to the ADCs and discriminators.

For the Gas Čerenkov and S0 detectors, a separate VME flexio module driven by the same pulser is used. The circuit board to mix the pulser is the same; however, the analog signal from each PMT is split: one signal goes to an ADC and the other is mixed with the EDTM pulse before proceeding to a discriminator and TDC.

5.6 Buffering and Synchronization

The CODA system also supports buffered front-end modules. This helps to decouple the read-out dead time from the conversion dead time, which effectively allows the system to run as fast as the front-end operation permits. However, as the event rate increases the probability of a full buffer also increases, and the read-out time begins to dominate the dead time. The DAQ system at Jefferson Lab is designed to support buffering of up to 8 events. The depth of the ROC branch buffers can be set from 1 to a maximum of 8, which allows support of a mixed system of buffered and unbuffered front-end modules. As an example, the TS crates contain unbuffered modules and have traditionally resided on branch 4 of the TS2 module, which is connected to the branch input of the VME TI module.

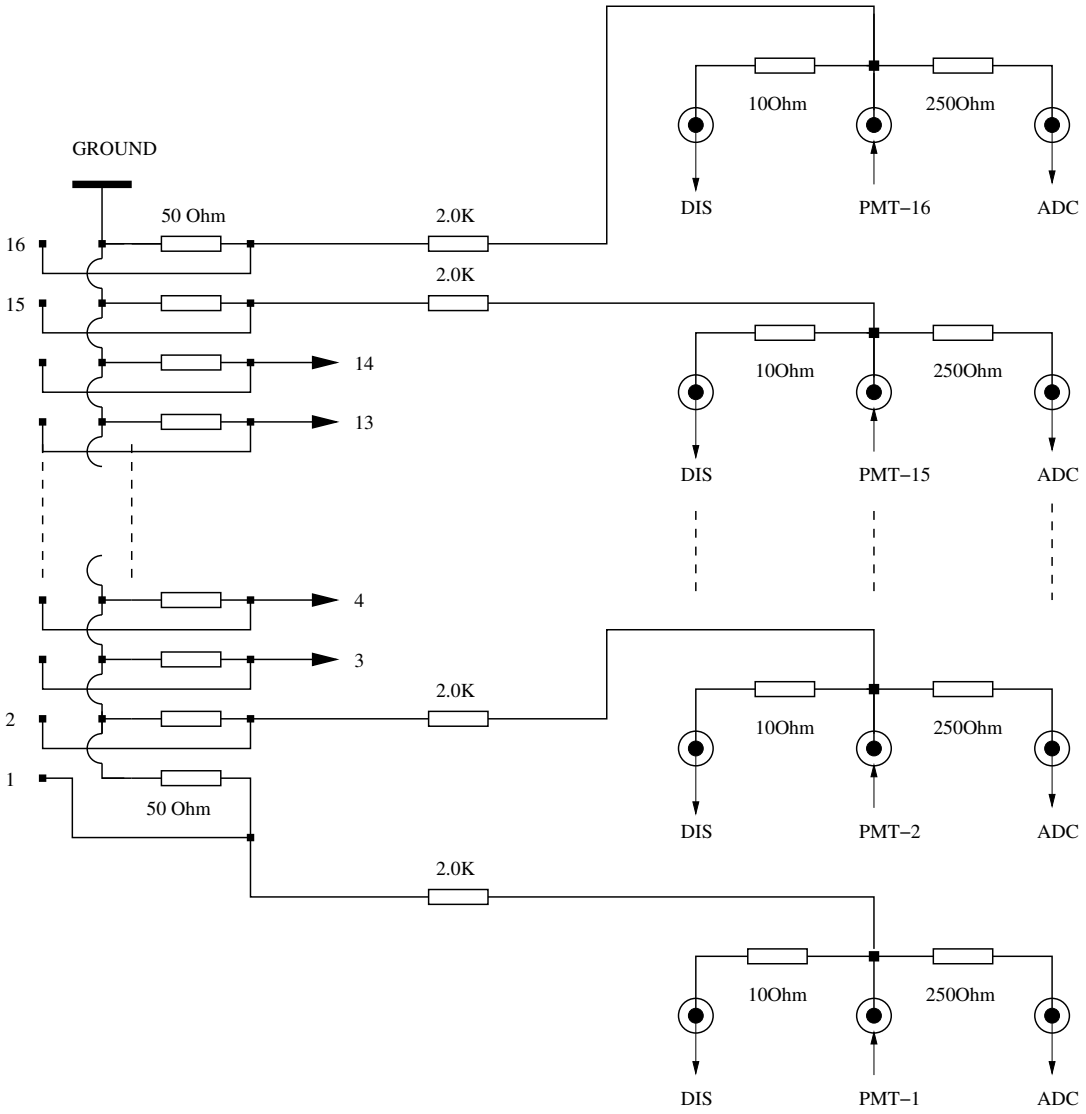

Figure 11: The EDTM splitter circuit diagram for the S2m detectors. The EDTM pulses arrive from the far left portion of the figure. The 2 kΩ resistors near the center of the diagram have been replaced by 1 kΩ resistors to allow a larger EDTM pulse output from the splitter.

When the DAQ is run in buffered mode, the busy signals from the front-end electronics need to be gathered and sent to the TS2 module. For the FASTBUS crates, each crate contains a signal distribution card, which contains a set of various connectors for busy signals, TDC common starts/stops, ADC gates and fast clear signals. This card provides an output busy signal required by the TS. In regards to the VME crates, the busy signal from each module needs to be gathered separately. The transition module has inputs to gather the various busy signals from both the local and remote front-ends. The TM module also provides an output that is the "OR" of all the input busy signals. This "OR" of the busies can then be used as the front-end busy input to the TS2 module. Finally, a special flag is required in the configuration of CODA to indicate to the system if the DAQ is in buffered or unbuffered mode.

In buffered mode, there is a potential of data misalignment due to hardware failures, which will result in all subsequent events being corrupted. The TS system has the capability to test periodically for synchronization. During the procedure, the TS stops accepting triggers and checks that all front-end buffers are empty. Missing or excess data are evidence of a synchronization problem. The TS uses a special status flag and a programmable counter to handle synchronization. When the programmed number of events is reached, the TS maintains and writes the status flag to the branch buffers. While in this state, the ROCs continue to read the event fragments from their front-end modules until the buffers are empty. If a 'no data' response occurs from any module, then this indicates a loss of synchronization and the section of events since the last successful synchronization should be marked as corrupted.

6 Scalers

In addition to raw hits on phototubes, scalers count important quantities such as charge and triggers, which are needed to normalize experimental data. In Hall A, the scaler data appear in the raw data as event type 140 as well as in the ROC10 (R-HRS) and ROC11 (L-HRS) data [12]. The event type 140 scalers are inserted into the datastream asynchronously every few seconds; whereas, the ROC10 and ROC11 information are read every synchronization event, which is either every 100 events in buffered mode or every 200 events regardless of the mode. The readout also contains helicity and timestamp information that is required for helicity decoding. Finally, event type 100 is the last scaler reading from ROC10/ROC11.

The scaler information in the datastream is identified by headers in the form of 32-bit words: "0xcebN00XY" for R-HRS scalers and "0xabcN00XY" for L-HRS scalers, where N is the *software slot* and XY encodes the number of scaler channels in the lowest 6 bits. The *software slot* is an arbitrary index used by various software and for historical reasons it may not be the hardware slot.

6.1 Scaler Gates

In Fig. 12, the behavior of the scaler gate signal is shown. The scalers are cleared at the start of a run and after the last scaler reading is completed at the end of the run. In between runs, the scalers are allowed to count so that the scaler rates can be monitored to check

experimental conditions and to adjust parameters before starting a new run. For the scaler

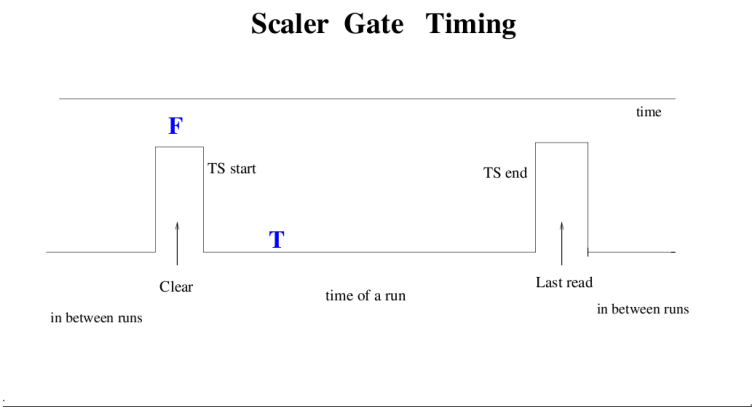

Figure 12: Schematic of scaler gating on HRS. When the scaler gate is true (T), the scalers count; whereas, when the gate is false (F), the scalers do not count.

gating, the Transition Module generates the scaler gate from the TS control signals *Go* and *Enable Level 1*. These signals along with *Clear* come from the TS2 module and are input to the differential ECL inputs on the TM module. From the Transition Module, the scaler gate signal can then be fanned out to the various scaler modules. The *Go* signal is maintained throughout the entire run period. The *Enable Level 1* is a control bit that can be set any time. At the start of the run, this bit is asserted, and then the scalers are cleared. During the run, the signal remains asserted, and then it is released after the last scaler reading.

The scaler data is also typically gated by the helicity period of the electron beam so that during a helicity transition it does not count. The helicity-gated scaler receives a gate which is "AND'd" in the appropriate way with the scaler gate from the Transition Module. The helicity gated scaler data are created from two *virtual* scalers in VME software, which are formed from one hardware scaler module.

6.2 Scaler Display

The online scaler data is displayed via the xscaler GUI. Traditionally, the L-HRS and R-HRS have their own separate GUI. In Fig. 13, an image of the L-HRS xscaler display is shown. At the top of the display is a series of tabs, where each tab represents a set of scaler channels; the scaler information may be from either a physical scaler module or *virtual* as in the case of the helicity gated channels. The xscaler GUI can either display the scaler information in counts or rates, where the rates are obtained by nomarlizing the counts by one of the clock signals. The name of each scaler channel appears on a button, which if clicked opens a graph with the most recent scaler readings plotted versus time. By continuing to click the button, the graph will be updated with any new scaler readings that have occurred since the last time the button was clicked.

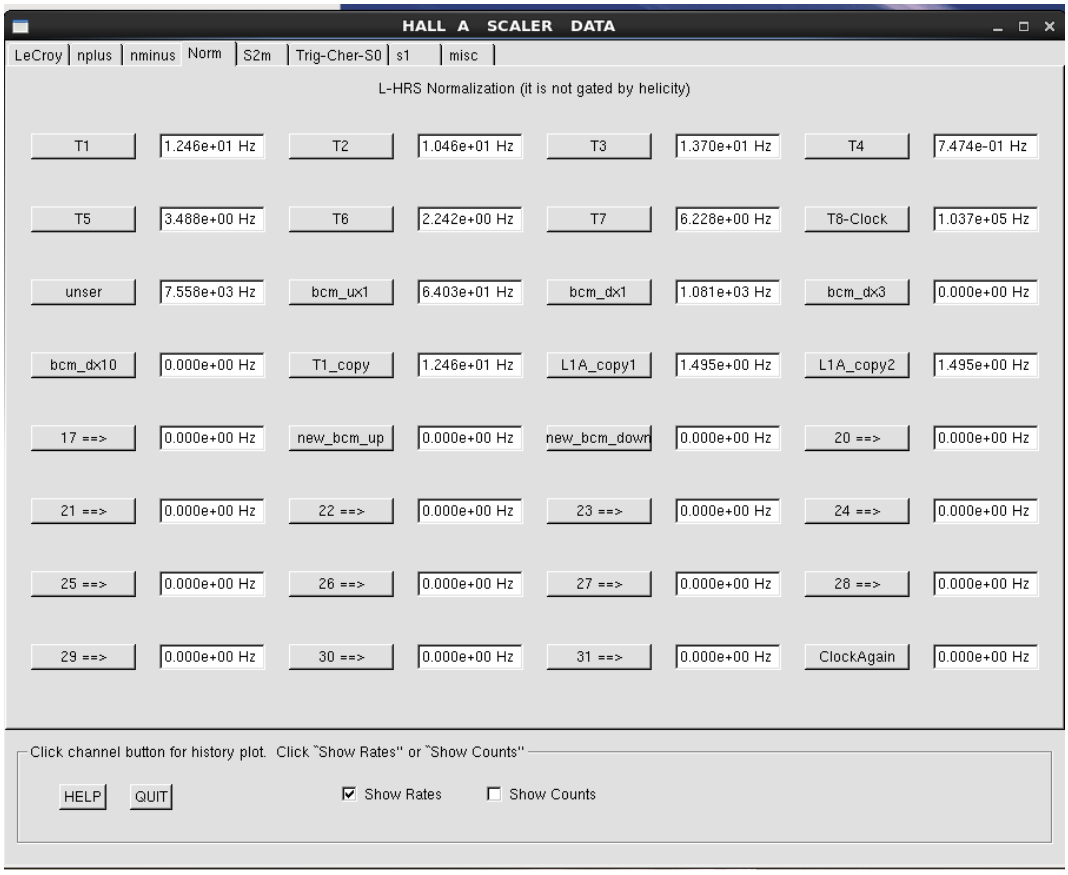

Figure 13: Image of the L-HRS xscaler GUI.

The *scaler.map* file [13] contains directives that control xscaler, including tab and channel names and the page layout. This file provides time-dependent mapping of the Hall A scaler channels, which includes obtaining scaler data by common names. Finally, directives also exist to simplify the map by tying the helicity scaler map to the non-helicity scalers. Since the information is time-dependent, the user most have a correct scaler map file for the relative time period of the data being analyzed.

7 Slow Controls

8 High Voltage Control

The detector high voltages (HV) are controlled by LeCroy 1458 crates, which host up to 16 modules such as the 1461N (P) for negative (positive) HV. Each of these cards has 12 HV channels, which can be individually set and remotely controlled. All the HV crates were refurbished. Their old motherboards (which were 20 years old and failing) were removed and replaced by serial cards designed by Hall A staff. These serial cards talk directly to the HV cards. The serial cards, in turn, are controlled by a PC. In the summer of 2014, the PC was replaced with a tiny PC called a raspberry (rPI board its the size of a credit card), which has the major advantage that it can service interrupts from the serial cards. This takes out some latency since now instead of waiting a safe period of time for cards to be ready, you simply let the HV cards tell you when they are ready. A Perl server runs on the PC, which "emulates" the old motherboard. The Perl server talks, via the network, to a Java GUI; this GUI displays the HV information and provides the control to the user.

The HV crates in use in the Hall A spectrometers are listed in Table 6.

Location	PC	Configuration
L-HRS (1 crate)	rpi8	LEFT
R-HRS (bottom crate)	rpi7	RIGHT
R-HRS (top crate)	rpi4	RIGHT

Table 6: The list of HV crates associated with the L-HRS and R-HRS.

Figure 14 displays a screen shot of the HV GUI for the R-HRS crates. At the top of the GUI, the tabs for the HV crates are listed: *rpi4:2001* and *rpi7:2001*. Within each tab, the slots with HV cards physically present in the crate are listed with a prefix "S" followed by the index for the slot number (starting from 0). Then for a given slot each channel number in the HV card is represented by a row in the table, starting from channel 0 to channel 12. For each HV channel, the channel name, measured current, measured voltage, target voltage, ramp up and down voltage rates, trip current, channel enable, and status are displayed in a different column. The columns shown in blue text can be adjusted by the user.

Finally, the TCP protocol instead of Telnet is now being used. This has already been deployed on the HRS now as an upgrade for the HV controls. It is a faster, more stable, and

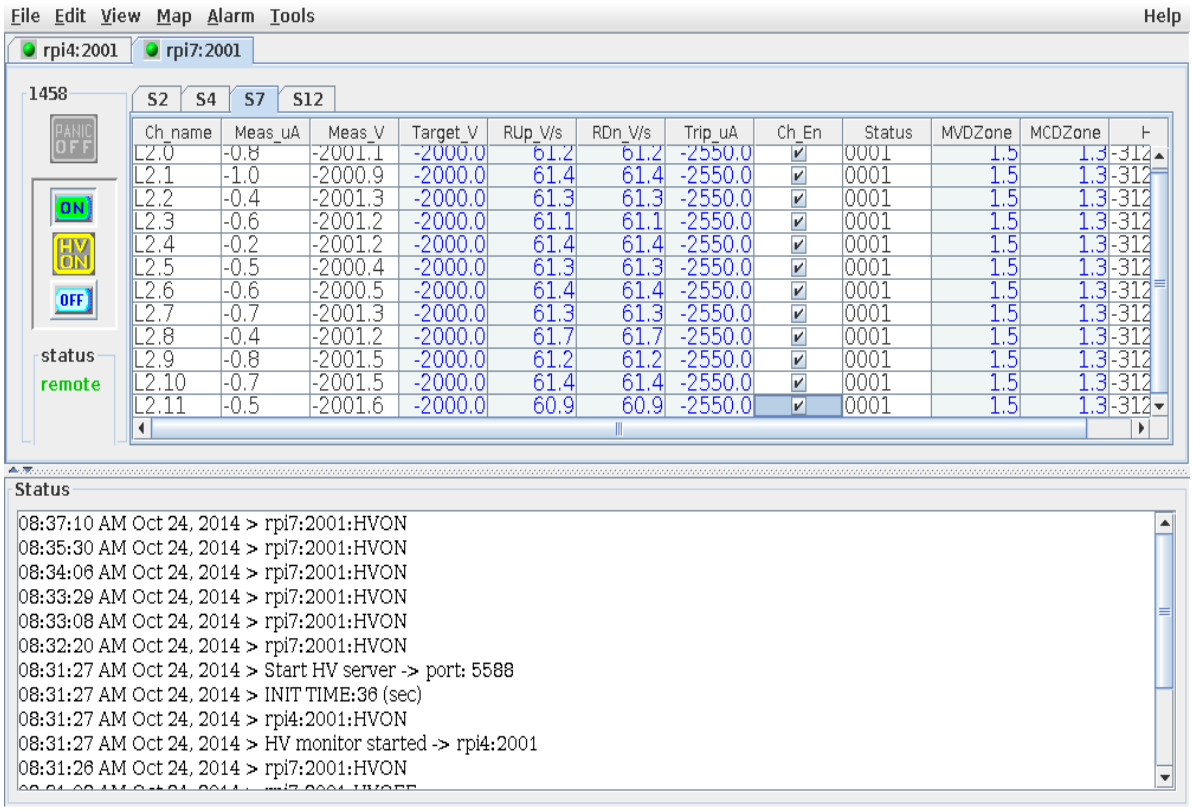

Figure 14: Image of the R-HRS bottom crate HV display.

more secure protocol. Instructions on how to run the HV software can be found at Ref. [14].

Acknowledgments

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