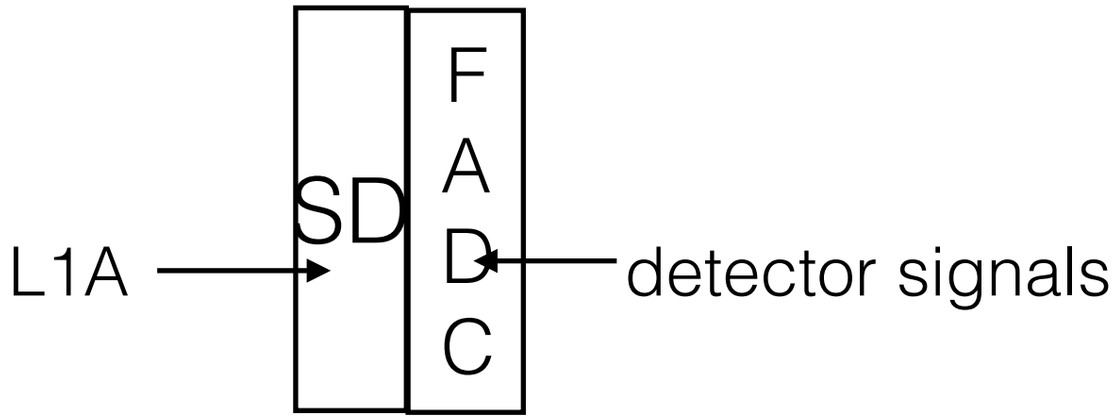
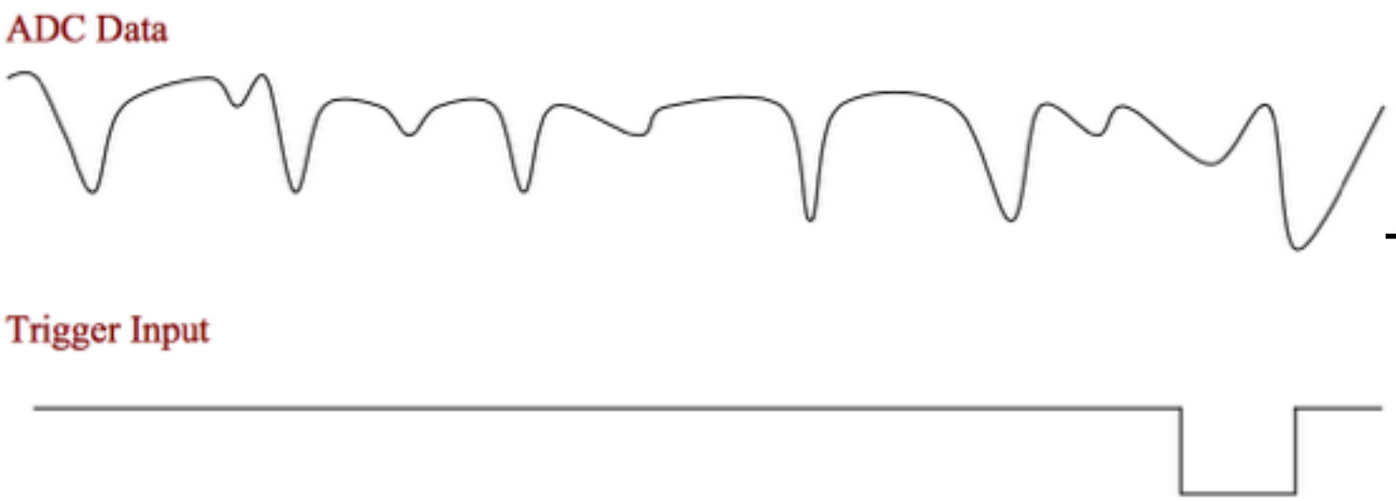
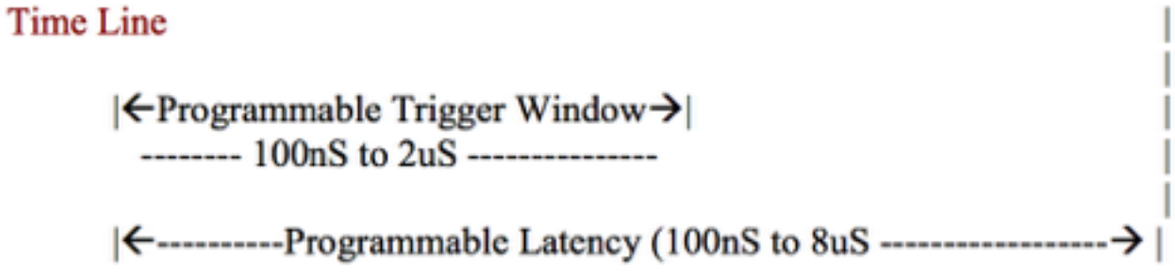
FADC status update

Hanjie Liu
2017.10.10

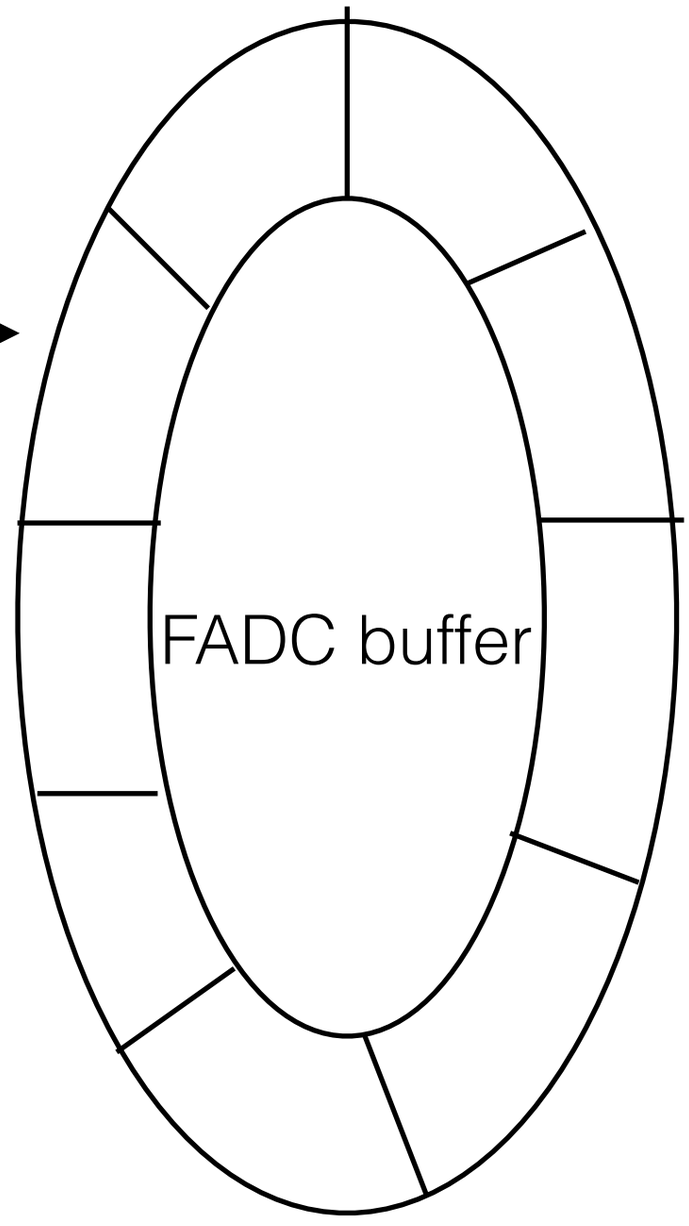






put in

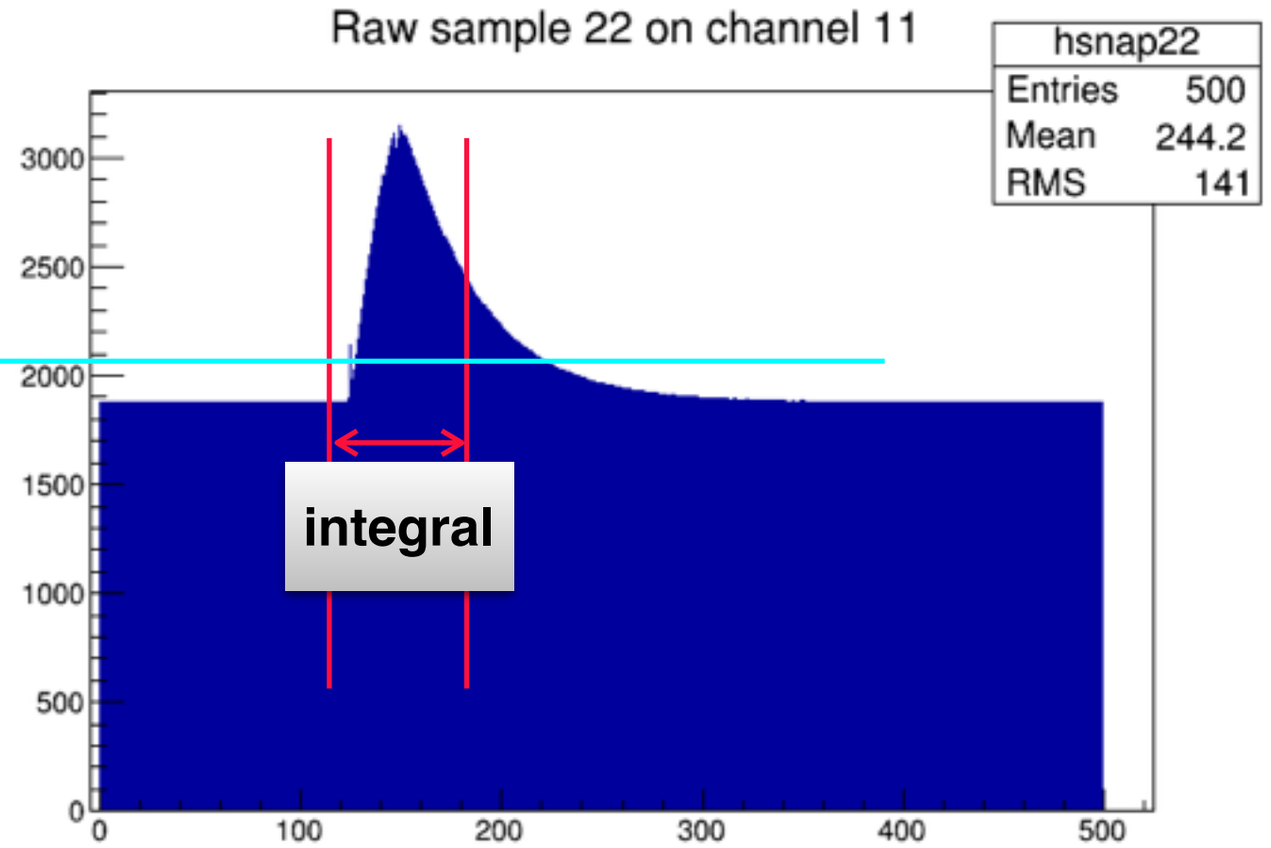
readout



FADC mode

1. Raw mode (mode 10)

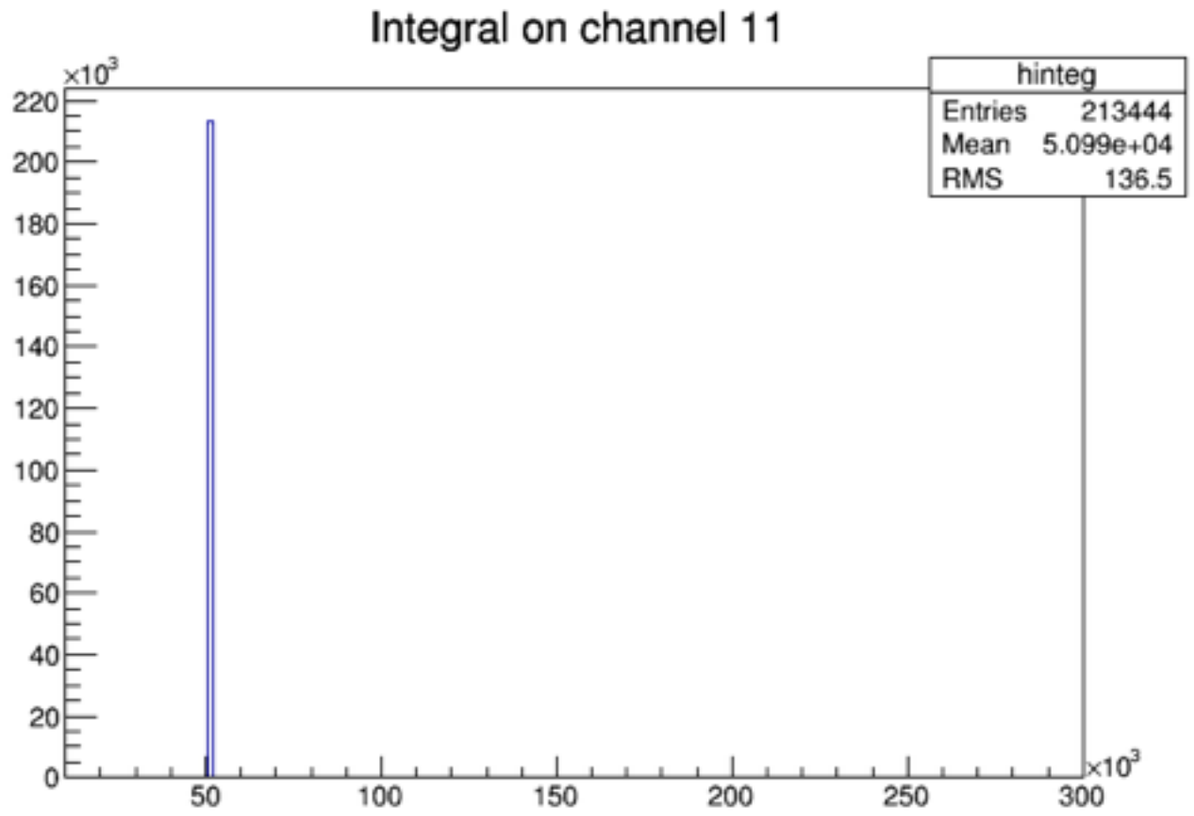
threshold

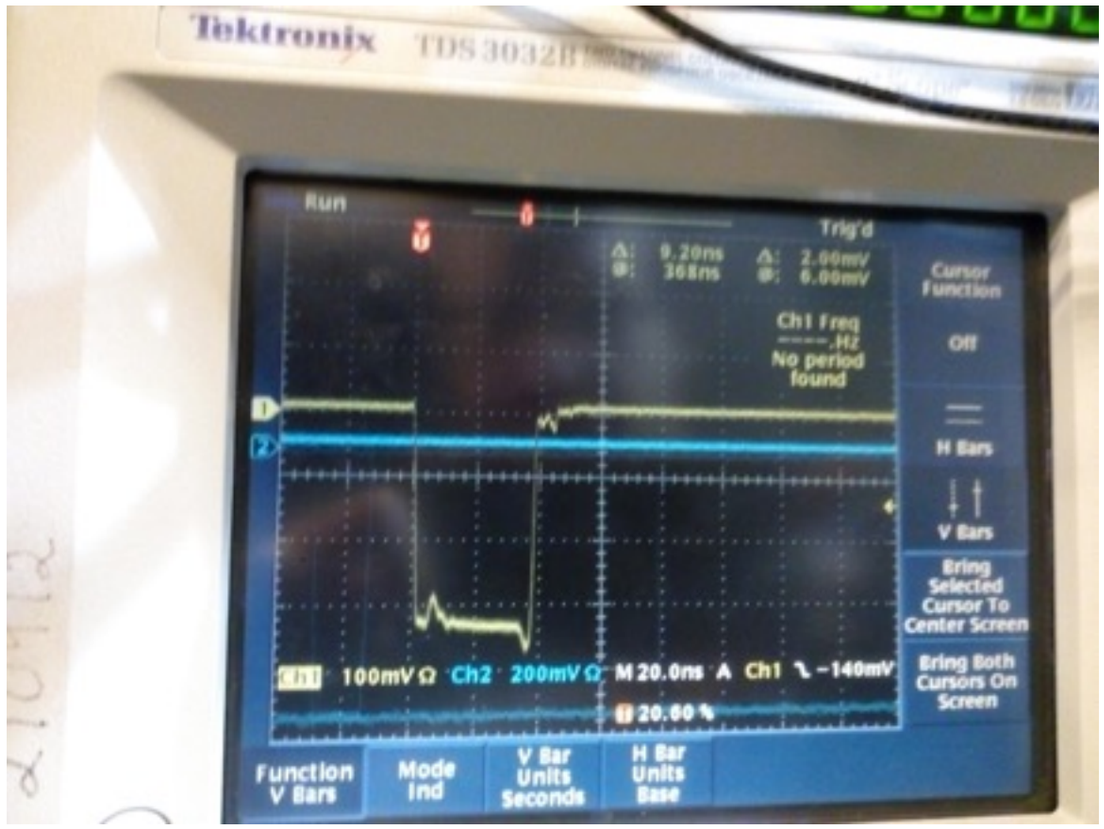


2. Pulse integral mode (mode 9)

for each event:

- integral number
- time crossing the threshold
- pedestal





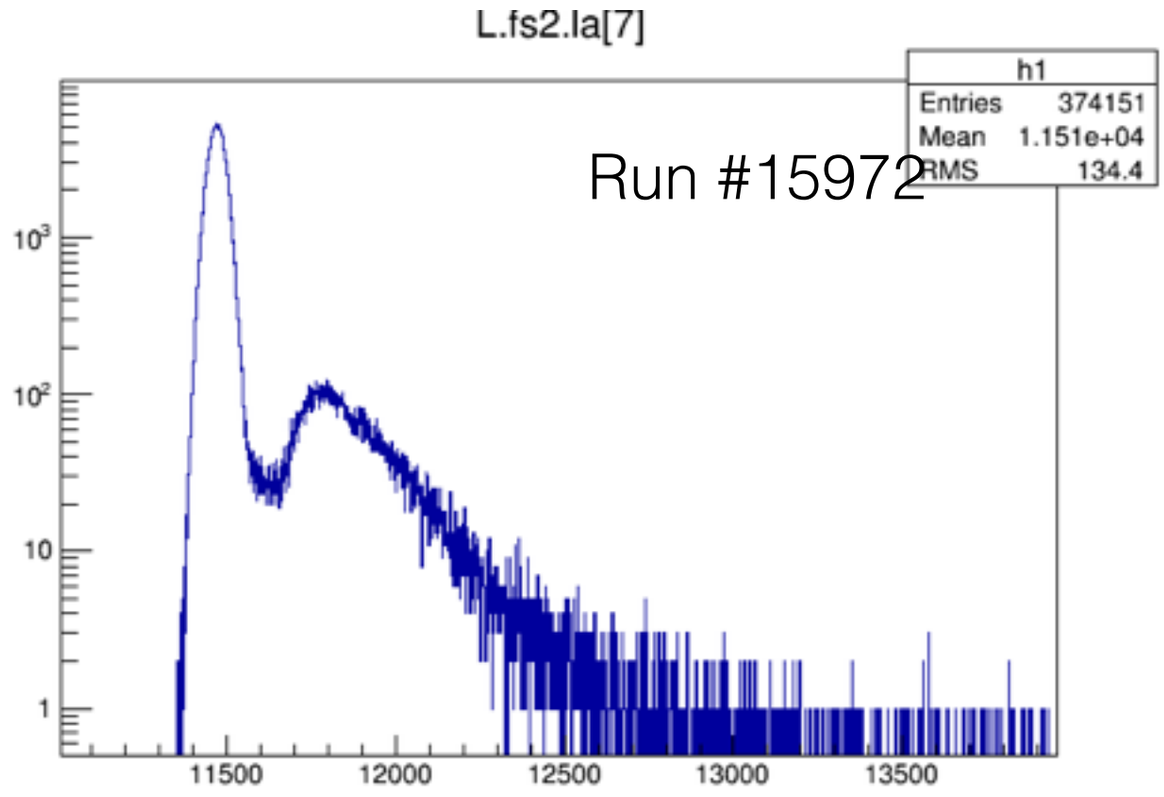
without filter

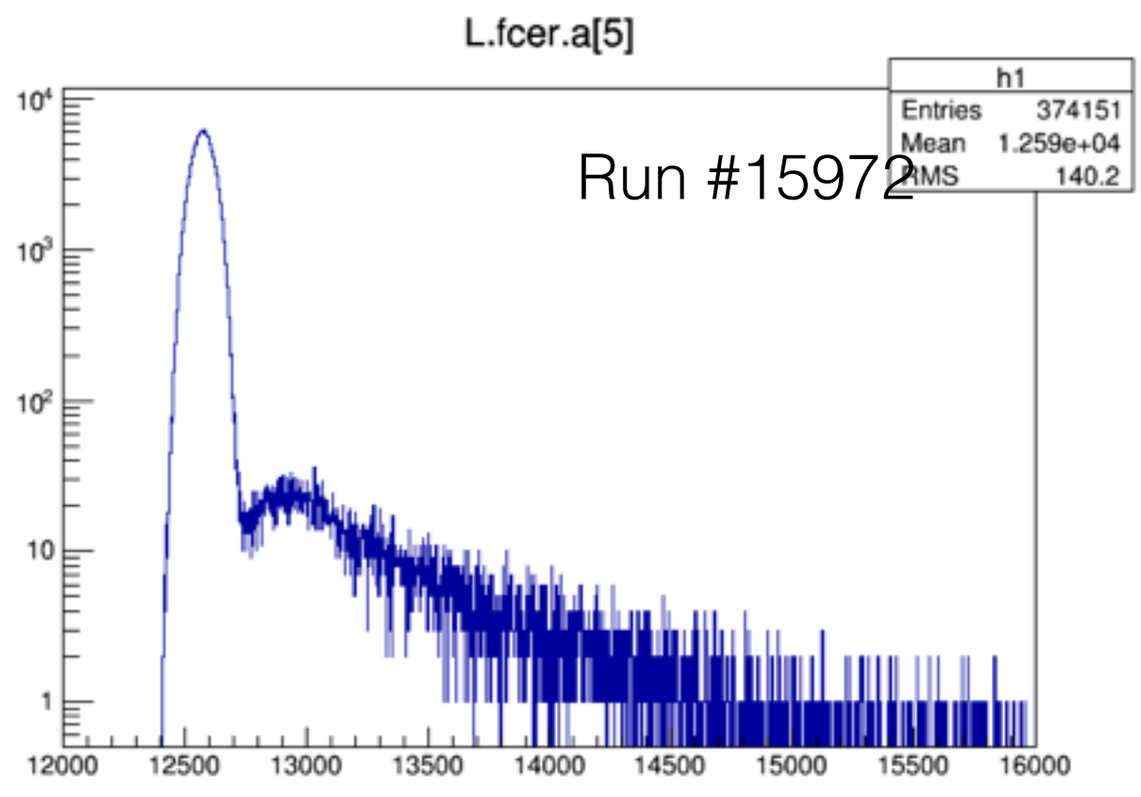
with filter

not use filter

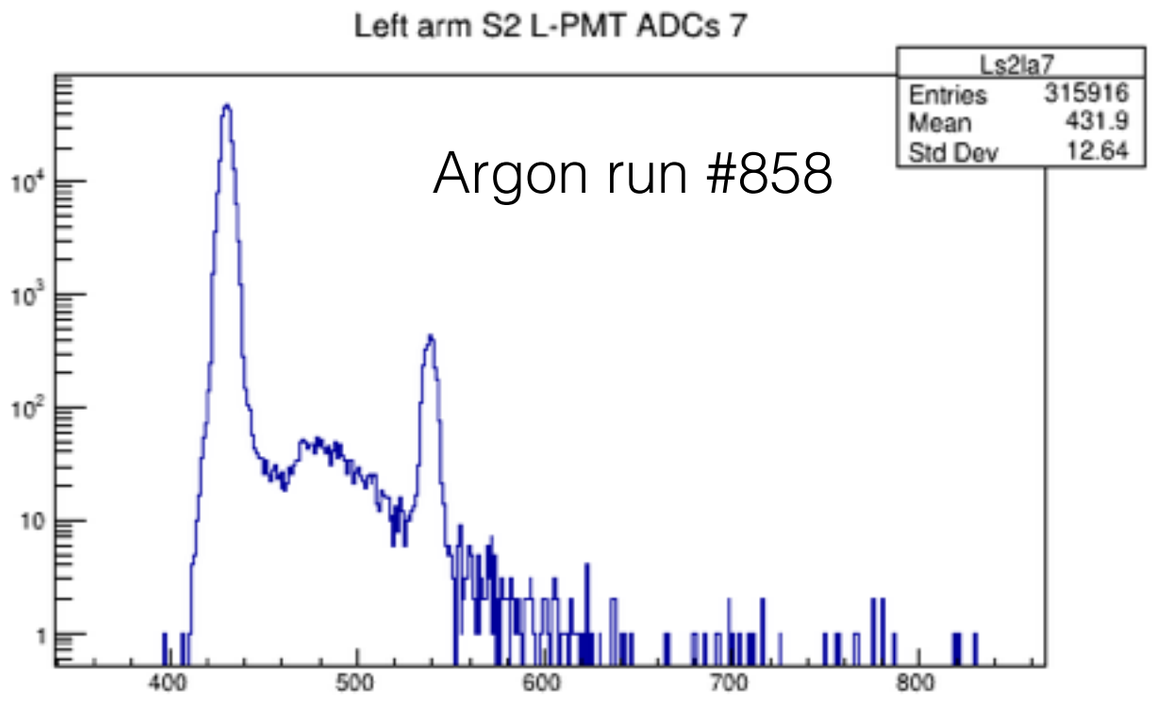
Set threshold 0 and integral width equal to window width:

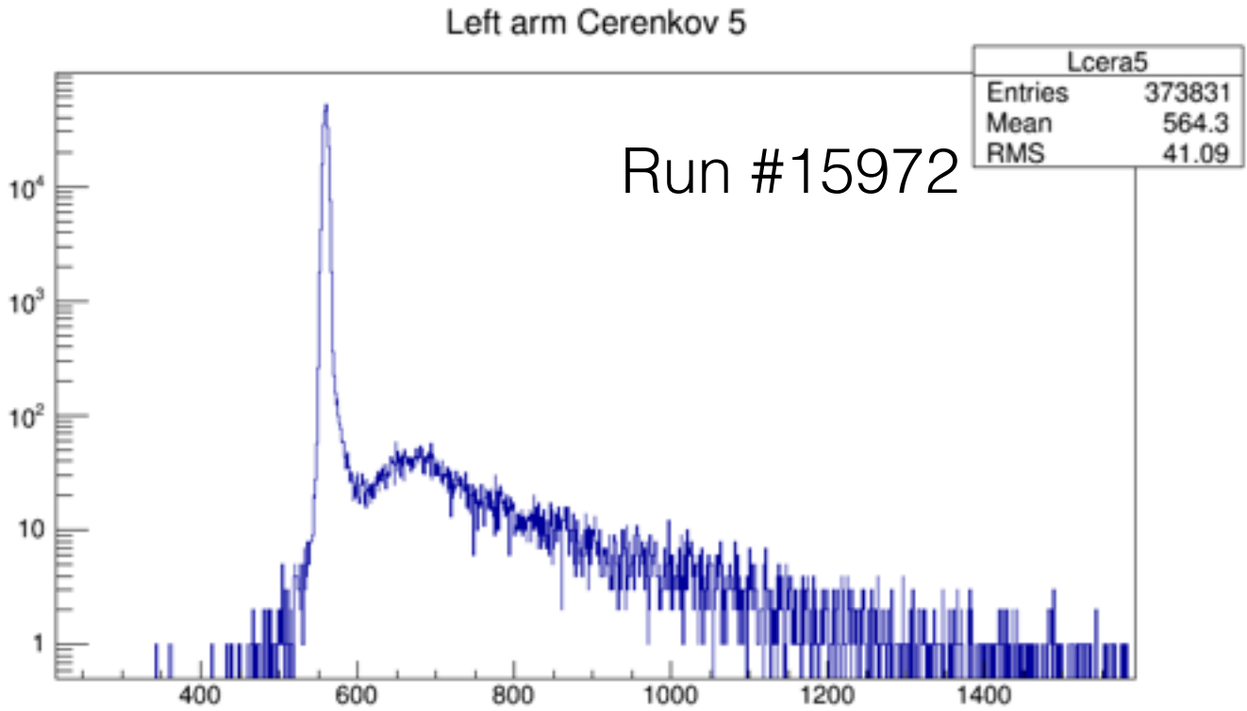
FADC



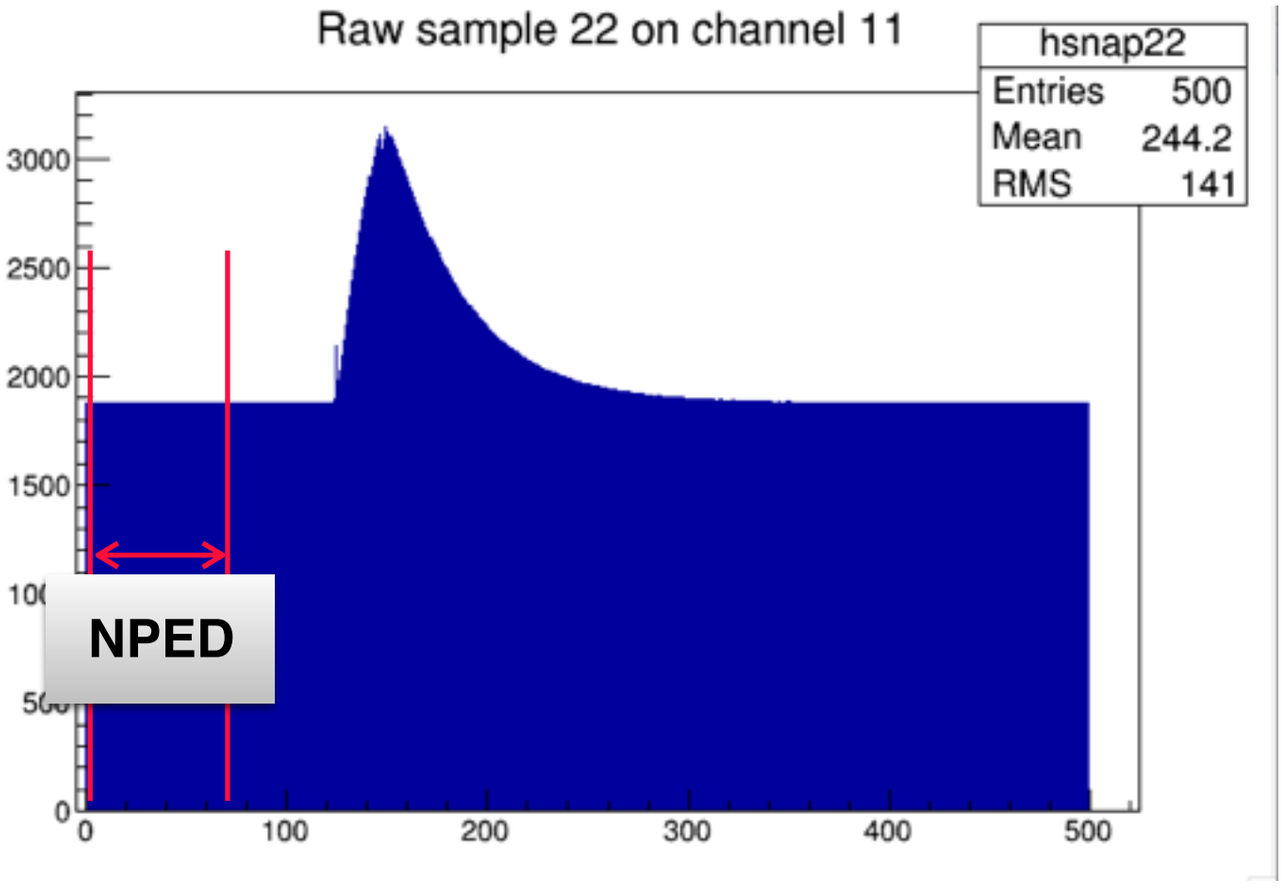


FastBus





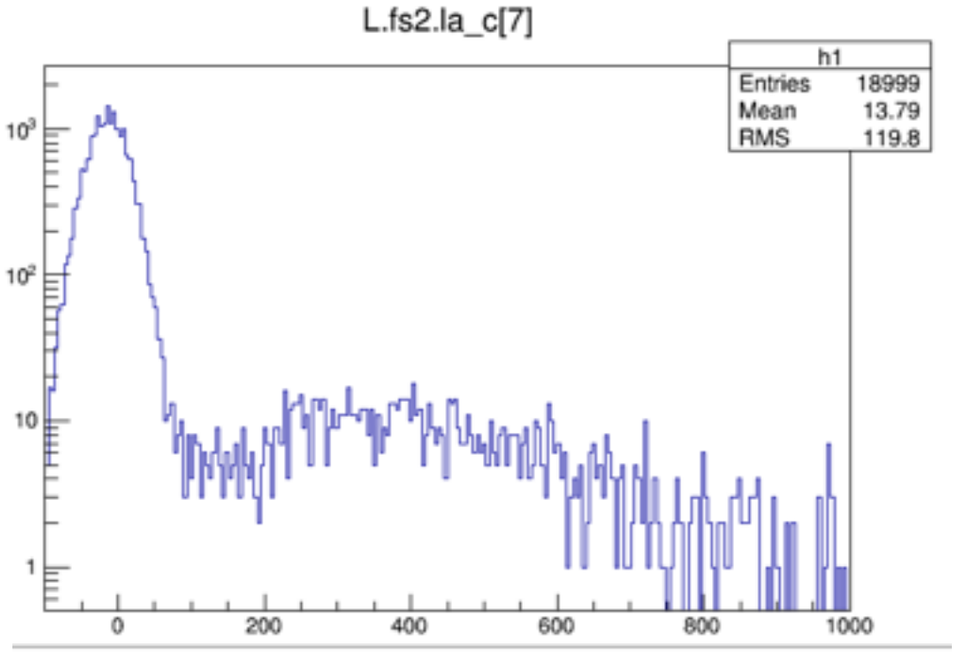
FADC record pedestal for every event



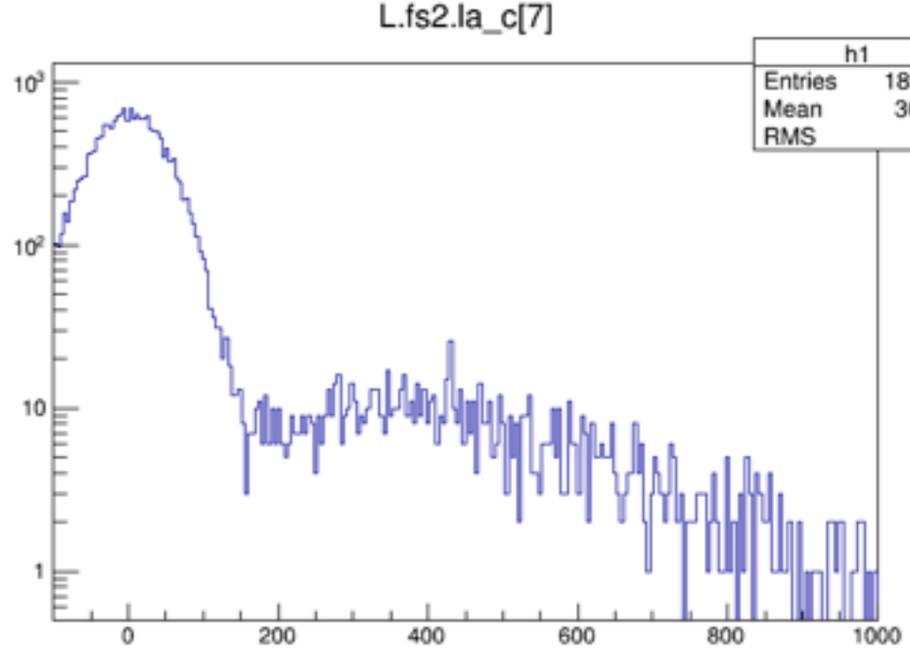
sum first (NPED+1) samples as pedestal sum

each event has its specific pedestal value

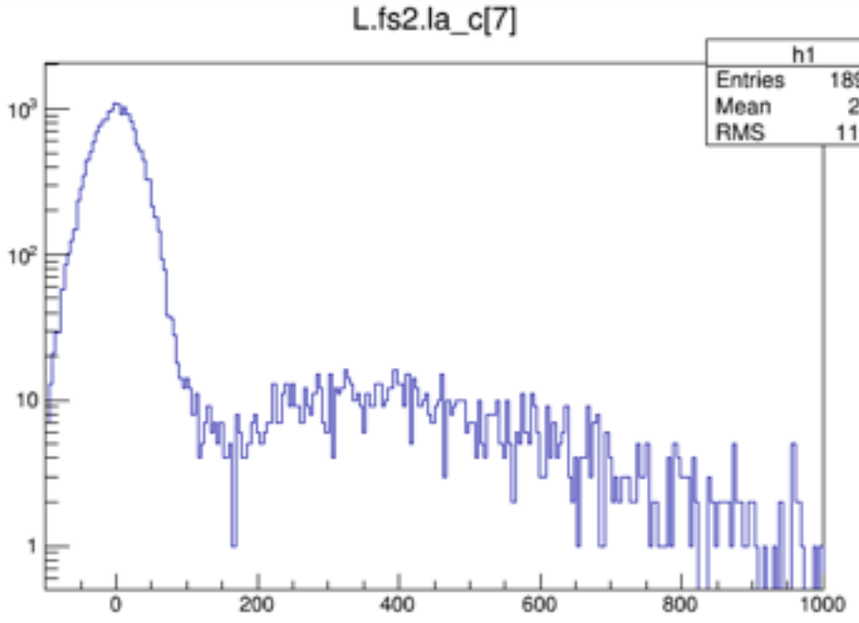
db



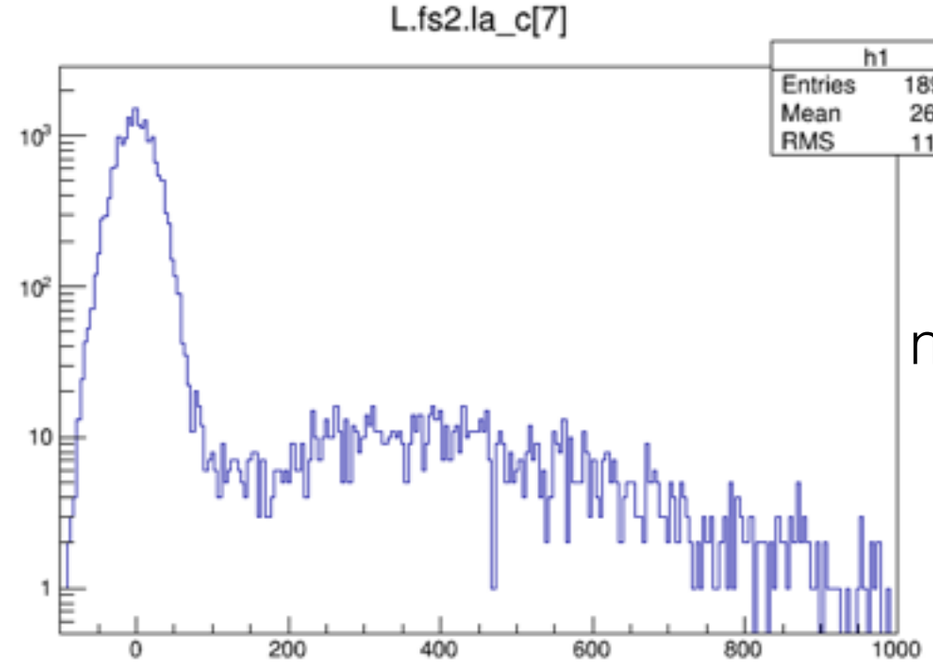
nped=4



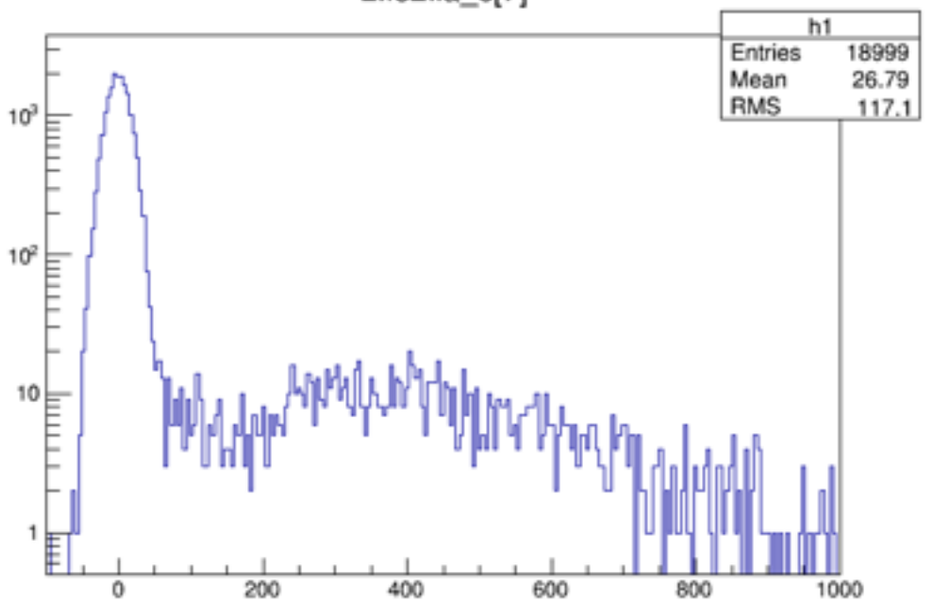
nped=10



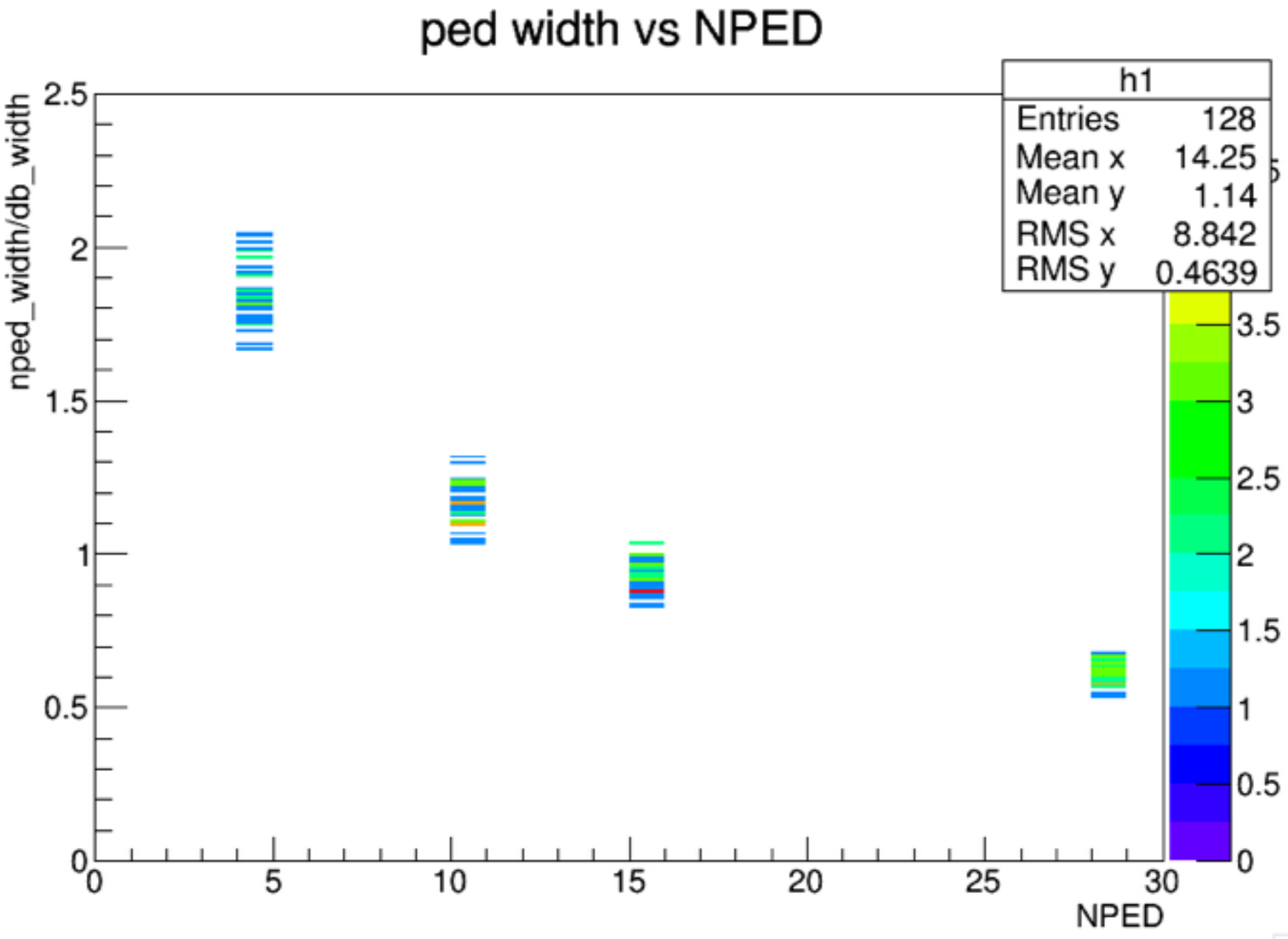
nped=15

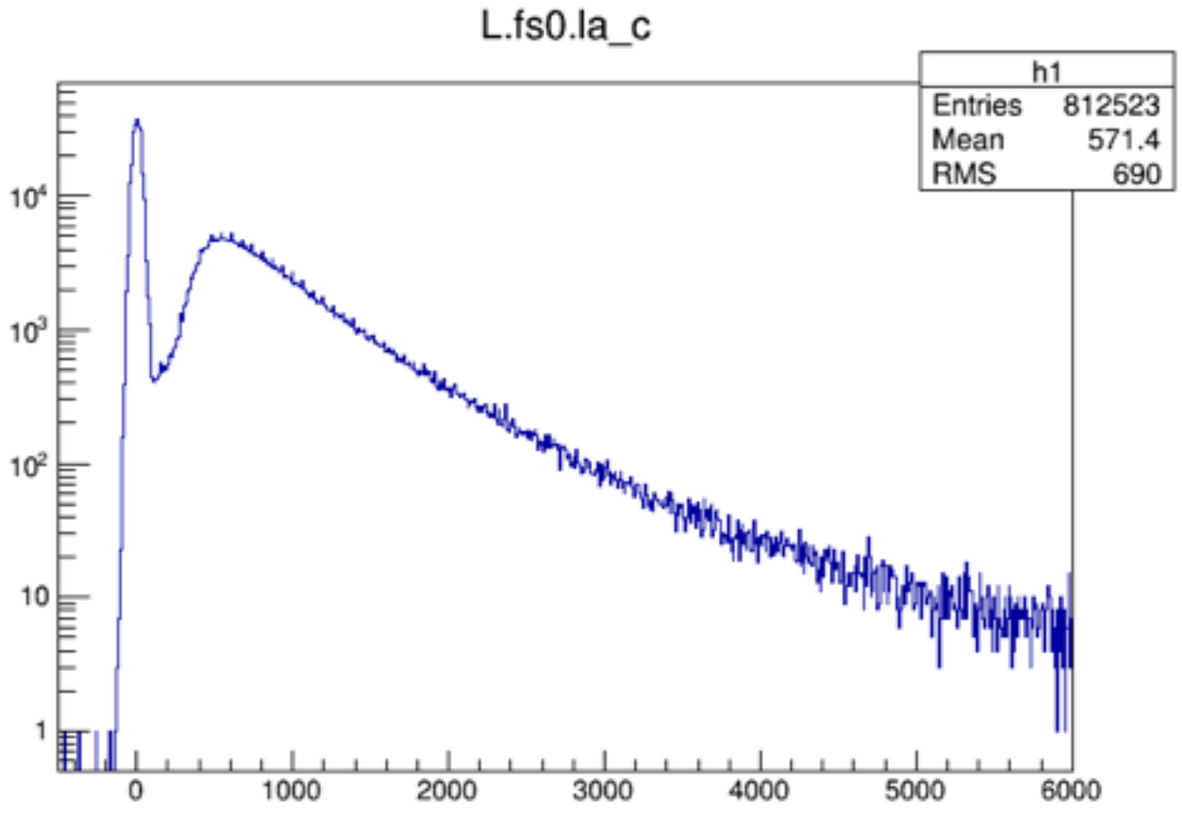


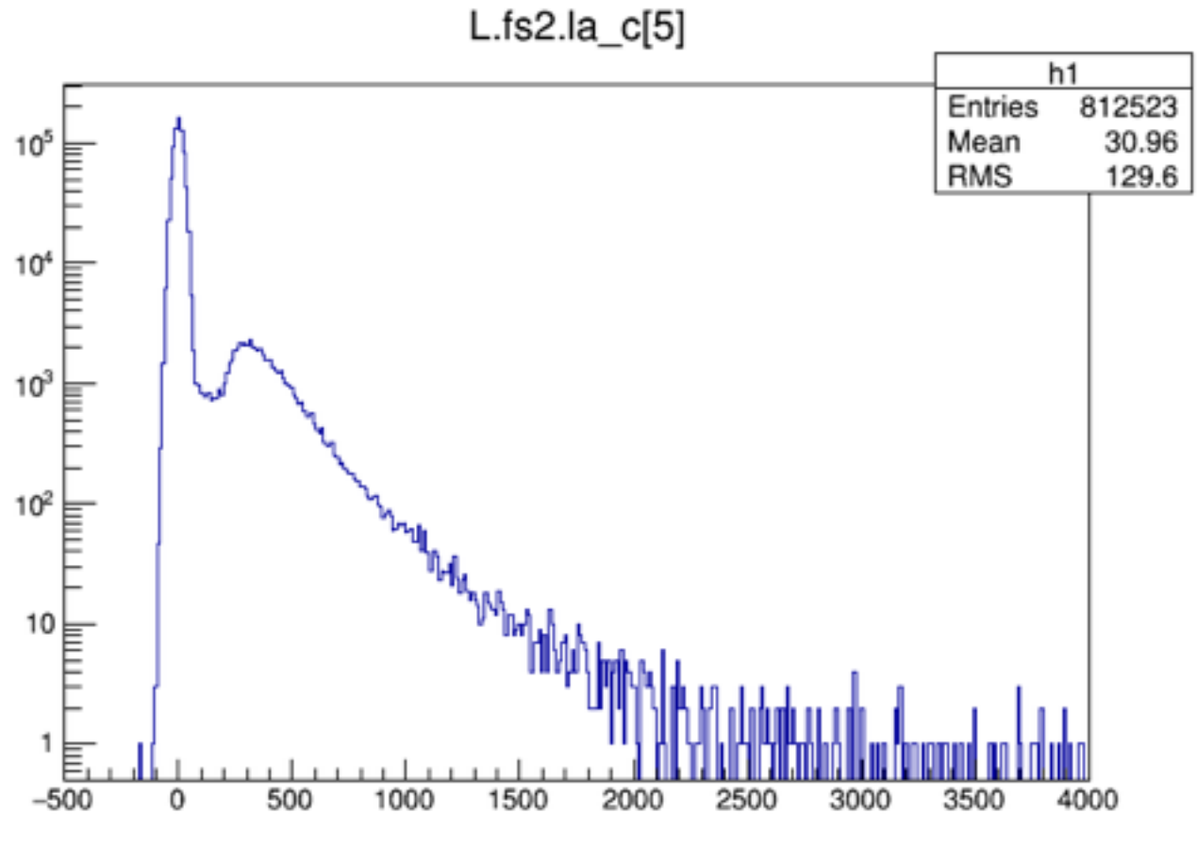
nped=28

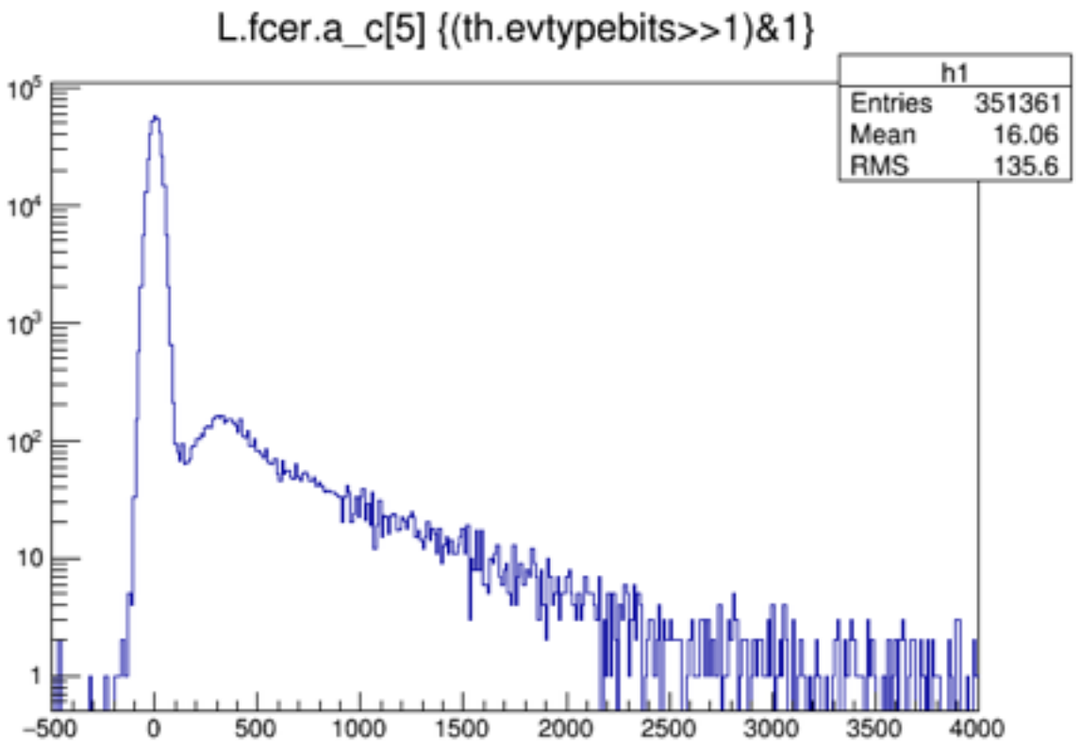


Run #130


ped width vs NPED
h1
Entries 128
Mean x 14.25
Mean y 1.14
RMS x 8.842
RMS y 0.4639
nped_width/db_width
NPED
0
0.5
1
1.5
2
2.5
5
10
15
20
25
30
3.5


L.fs0.la_c
h1
Entries 812523
Mean 571.4
RMS 690


L.fs2.la_c[5]
h1
Entries 812523
Mean 30.96
RMS 129.6


L.fcer.a_c[5] {(th.evtypebits>>1)&1}
h1
Entries 351361
Mean 16.06
RMS 135.6

Run #138

problems:

- the scaled fadc signal peak is not aligned with FastBus;
- check if the splitter affect the scale factor between FastBus and FADC