Coincidence Trigger and Retiming

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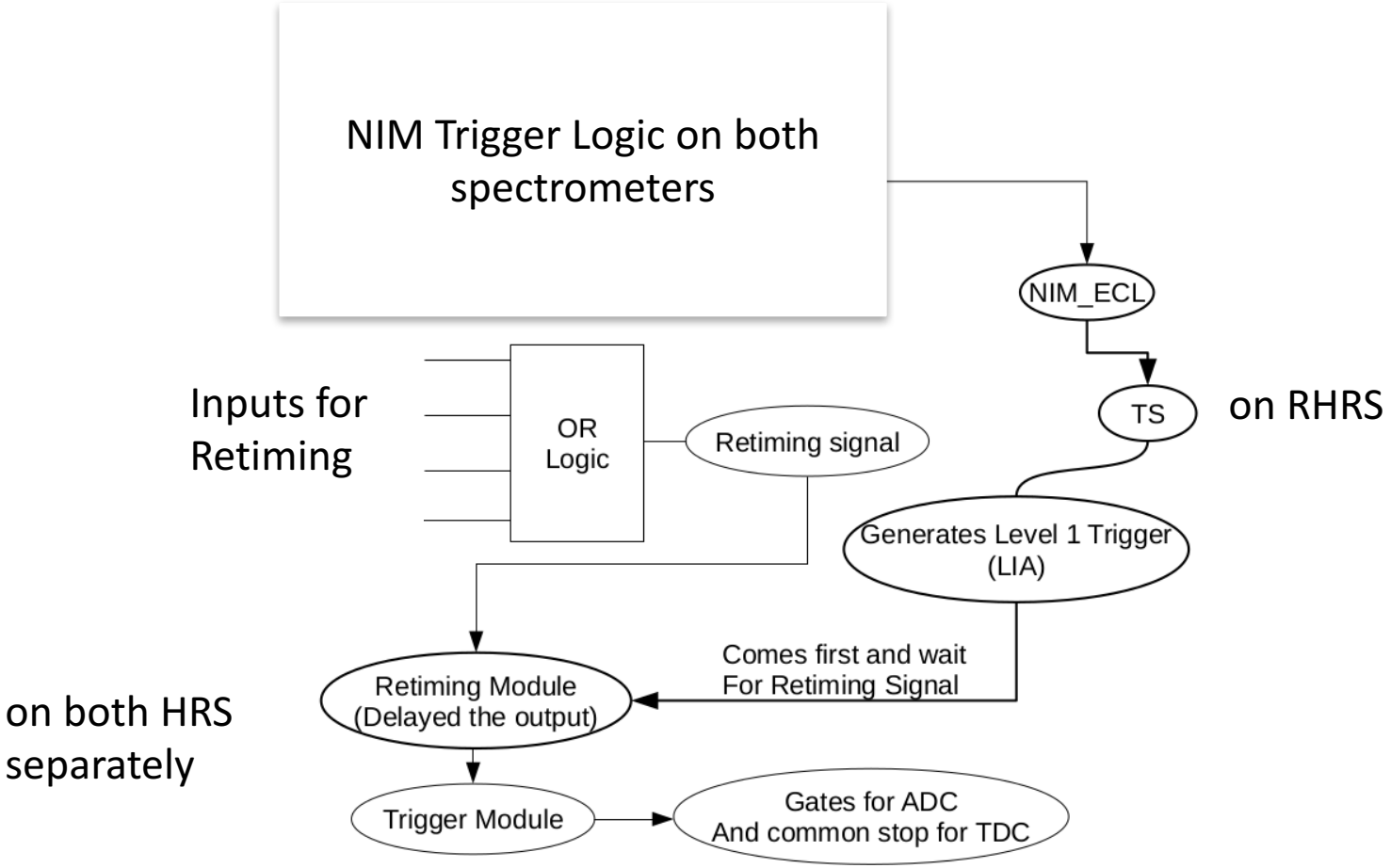
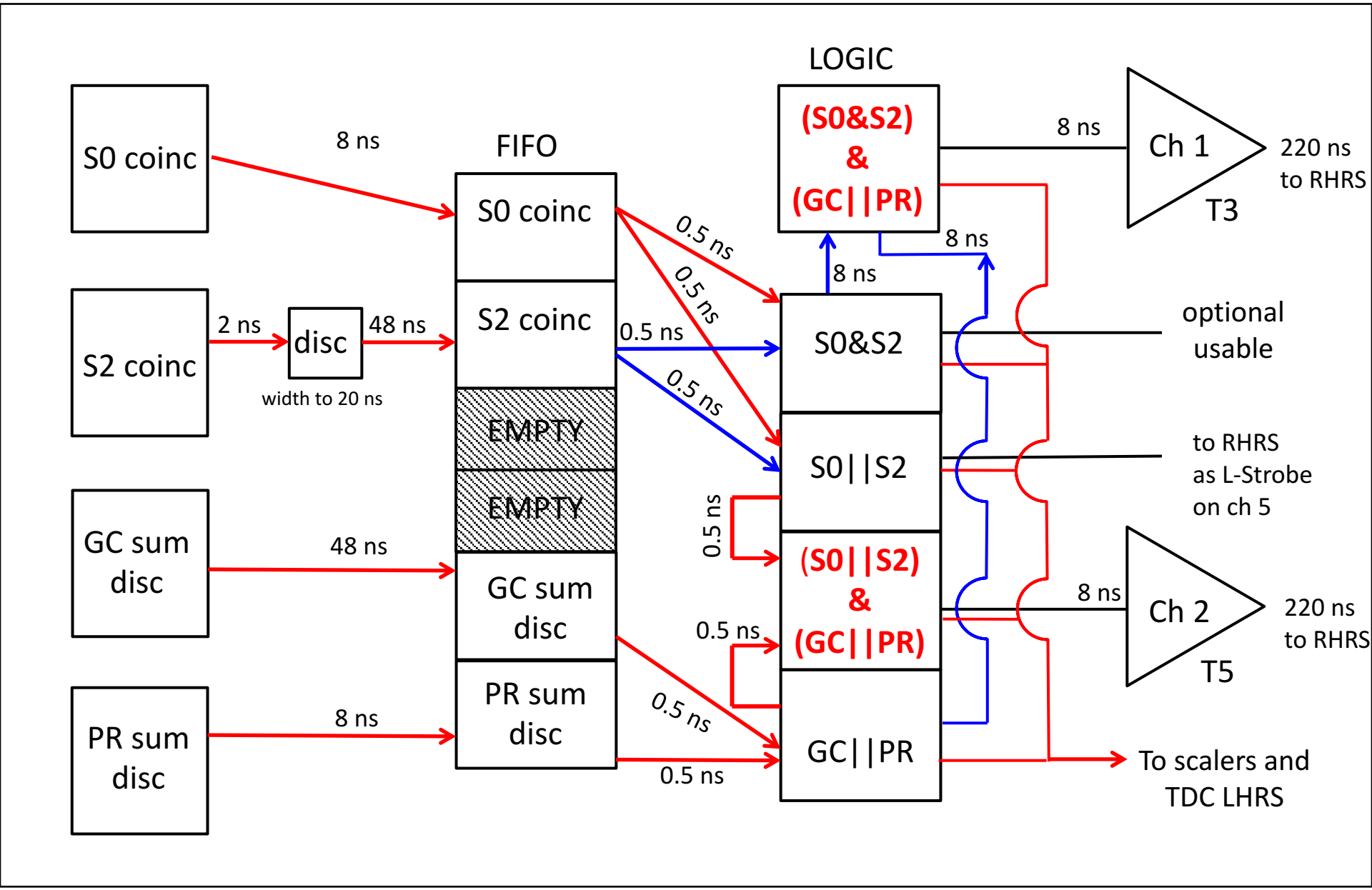
Overview

- LHRS Trigger Setup
- RHRS Trigger Setup
- Coincidence Trigger
- L1A Accept and Retiming
- ADC gate
- (Modifications from first setup)
- (What has to be changed for fall)

Introduction



Schematics of Trigger Setup LHRS (valid till 03/07/17)



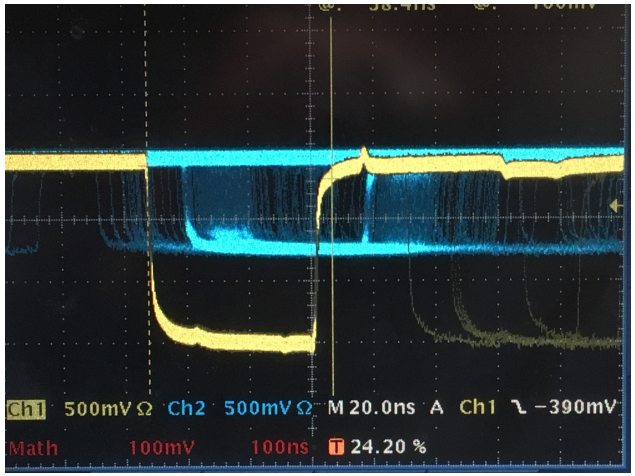
GC: Gas Cherenkov PR: Pion Rejector

LHRS: S0 & S2 Coincidence

before changes

S0 (blue)
S2 (yellow)

S0 defines time

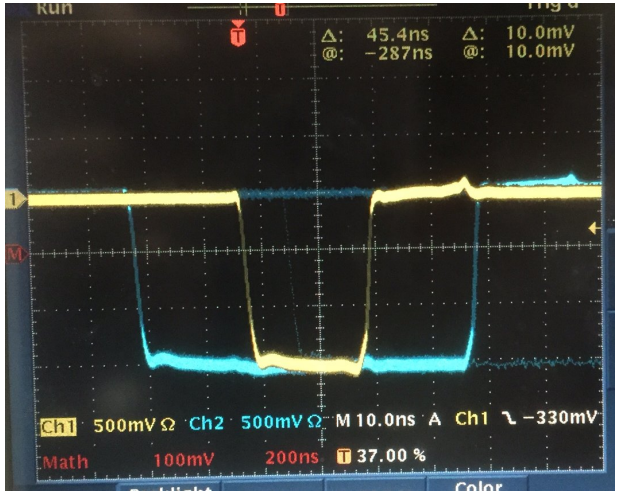


after changes

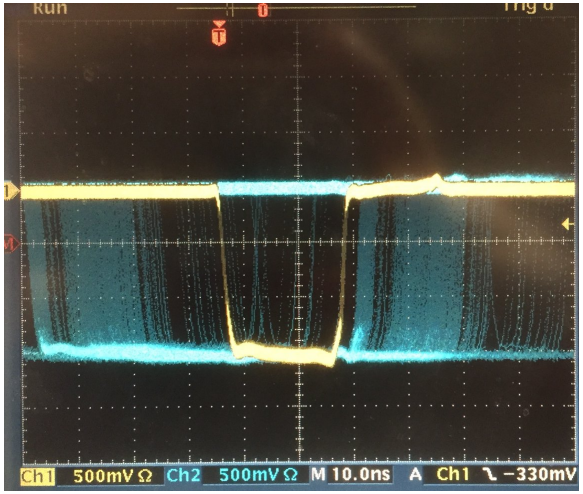
S0 (blue)
S2 (yellow)

S2 defines time

→ better timing

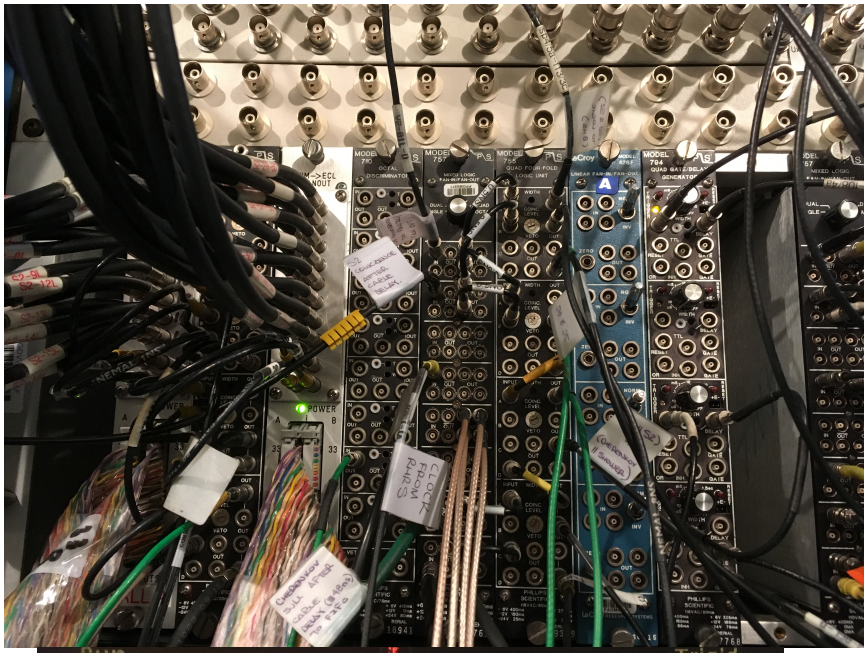


clock

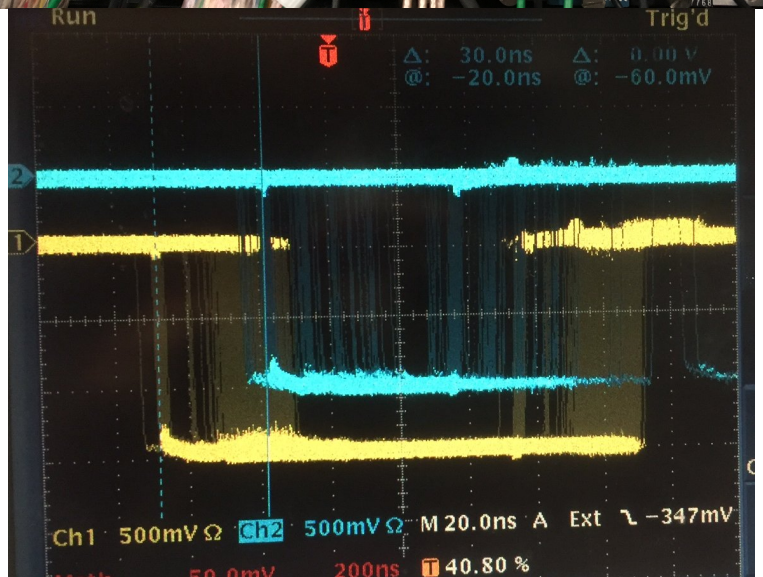


cosmics

LHRS Trigger Pictures



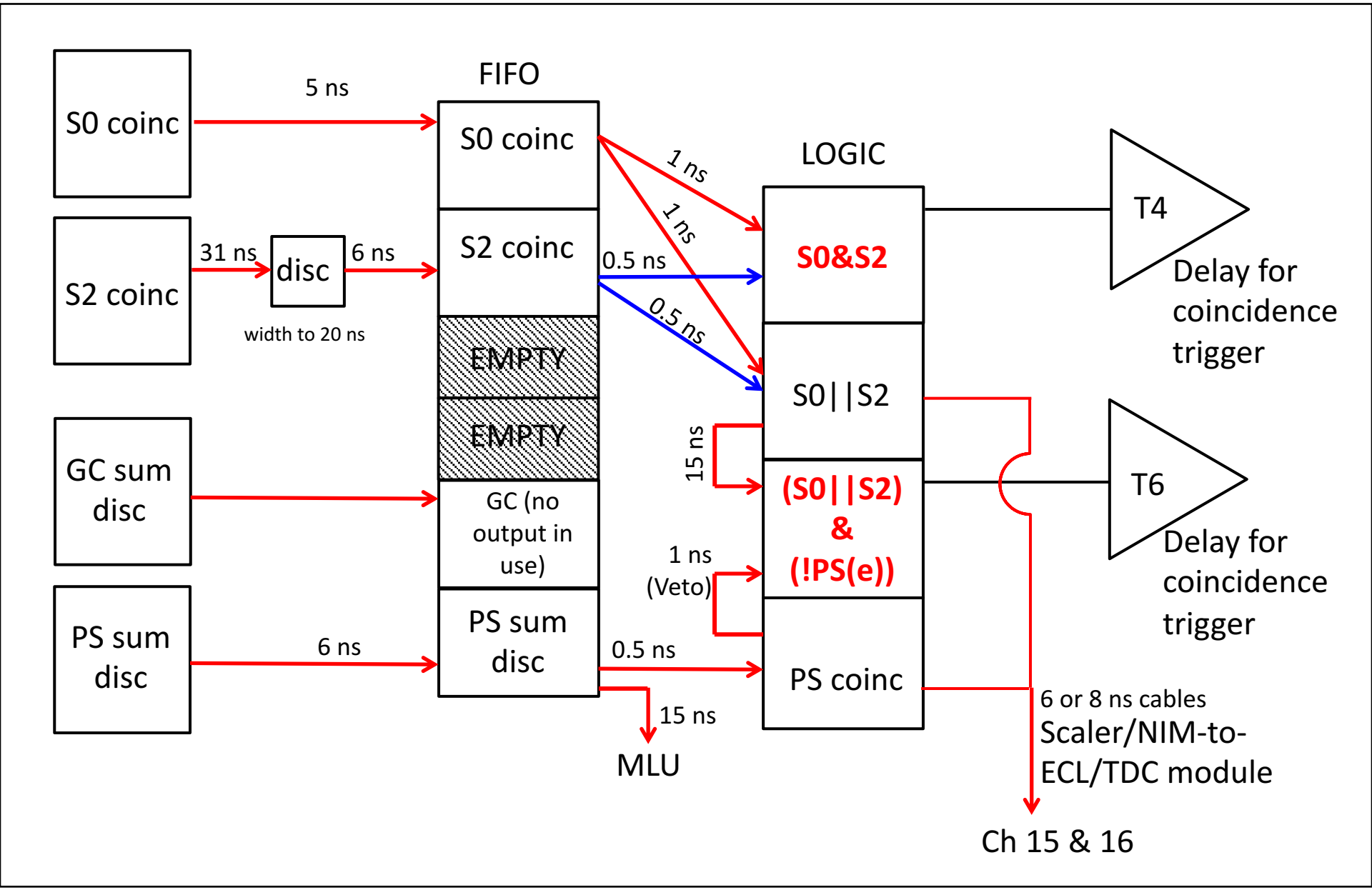
Middle Rack (R2),
Top NIM Crate (N1)
Modules 2 - 11



External trigger S0&S2

S0||S2 (yellow)
GC||PR (blue)

Schematics of Trigger Setup RHRS



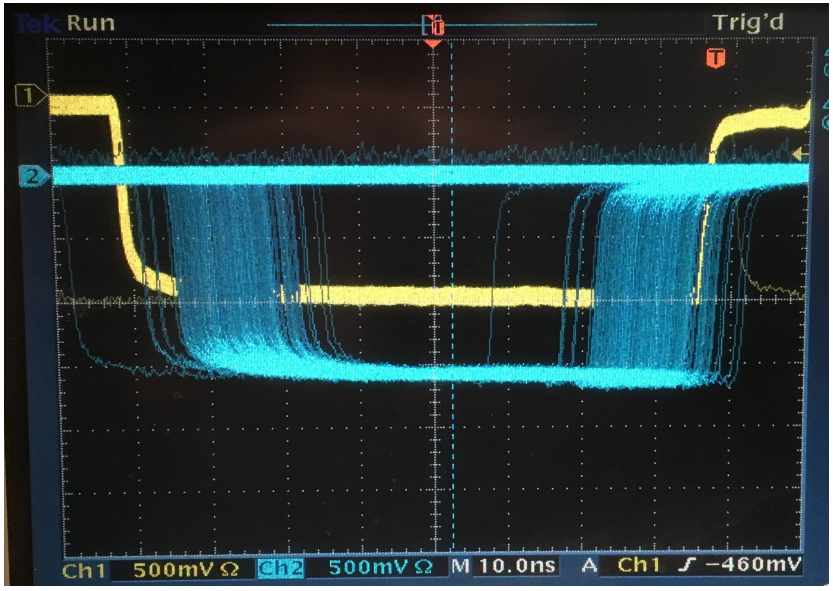
GC: Gas Cherenkov PS: Preshower/shower

RHRS: S0 & S2 Coincidence

<u>before changes</u>

S0 (blue)
S2 (yellow)

S0 defines time

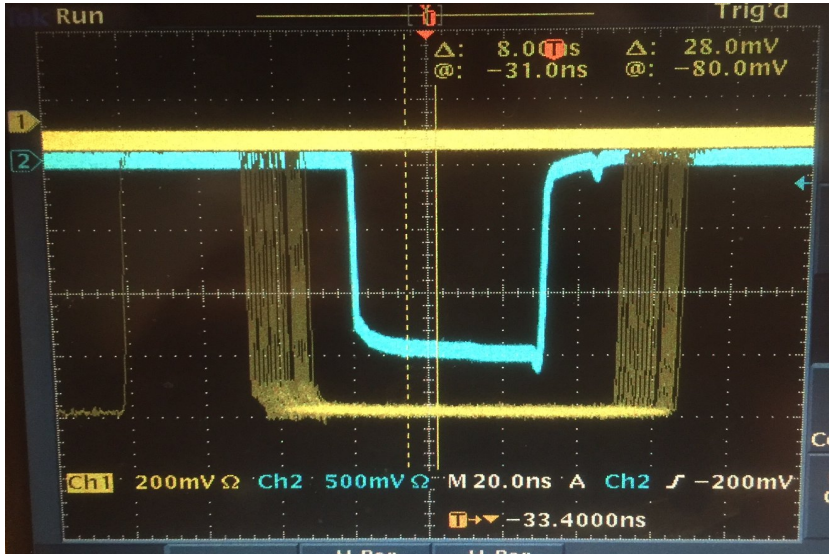


<u>after changes</u>

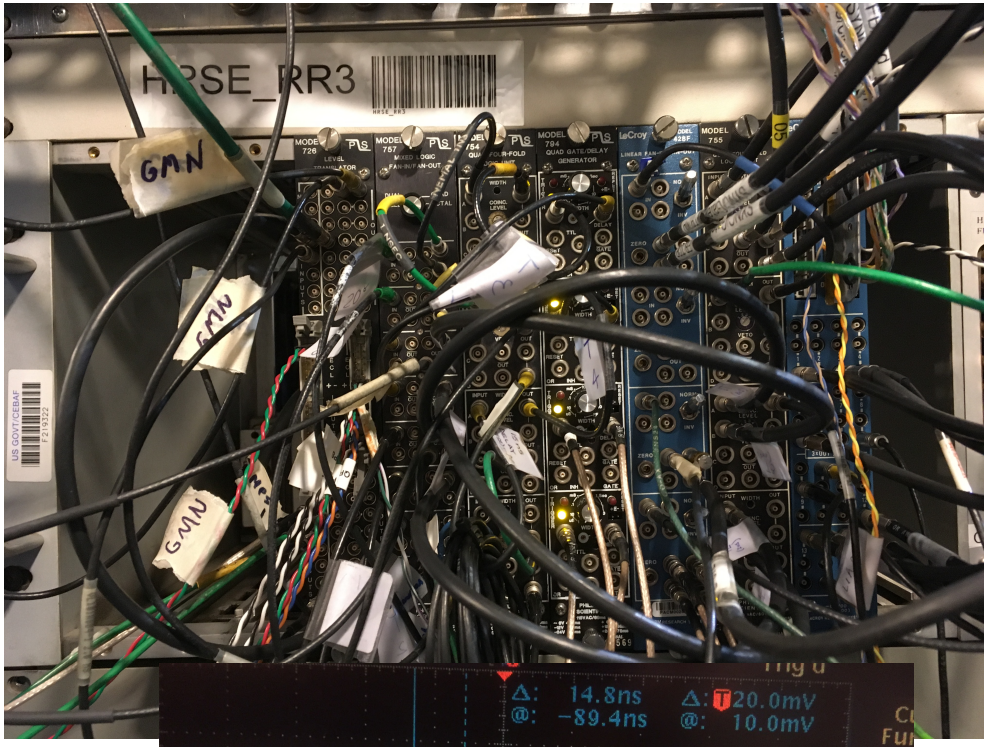
S0 (blue)
S2 (yellow)

S2 defines time

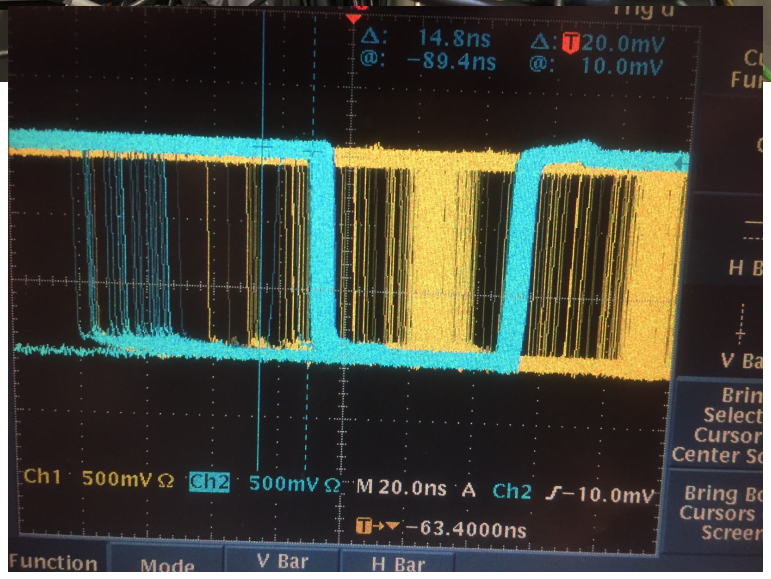
→ better timing



RHRS Trigger Pictures



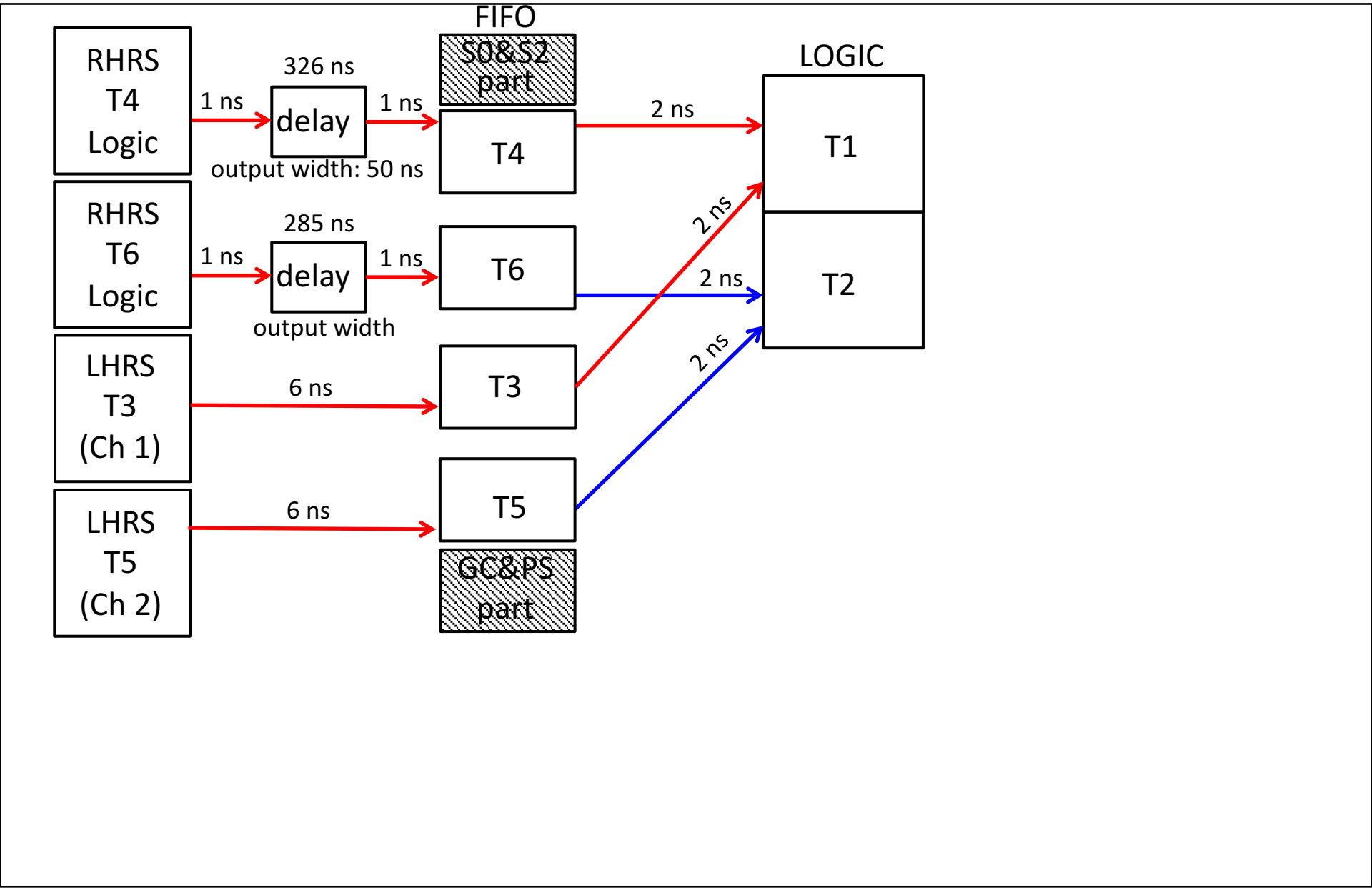
Middle Rack (R3),
Top NIM Crate (N1)
Modules 4 - 9



Test PS veto

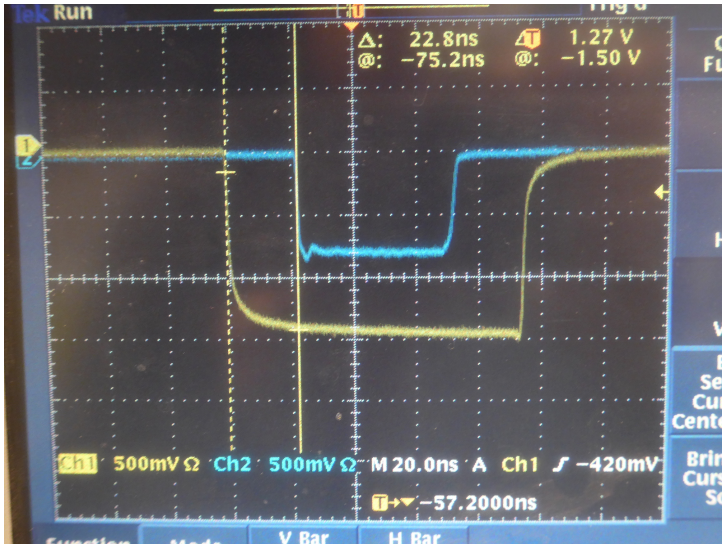
S0||S2 (yellow)
PS (blue)

Coincidence Schematics (on RHRS R3, N1)



Delay: Delay generator

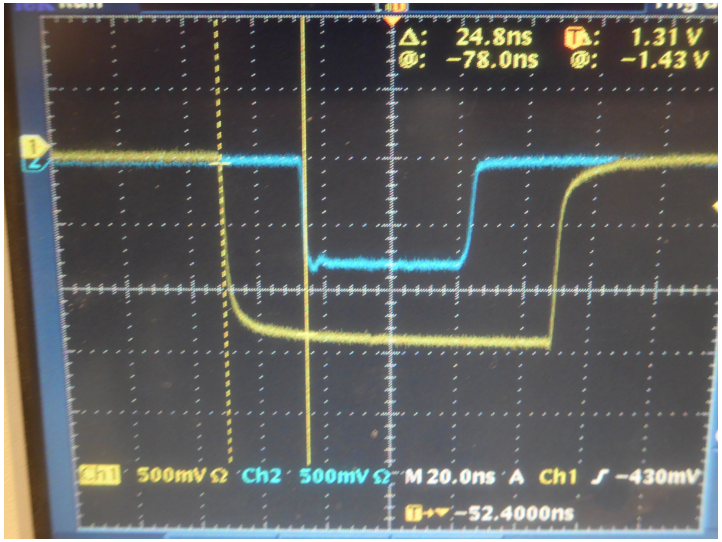
Coincidence Trigger



T1 coincidence

T3 (yellow)
T4 (blue)

→ Coincidence window and signal width changed later



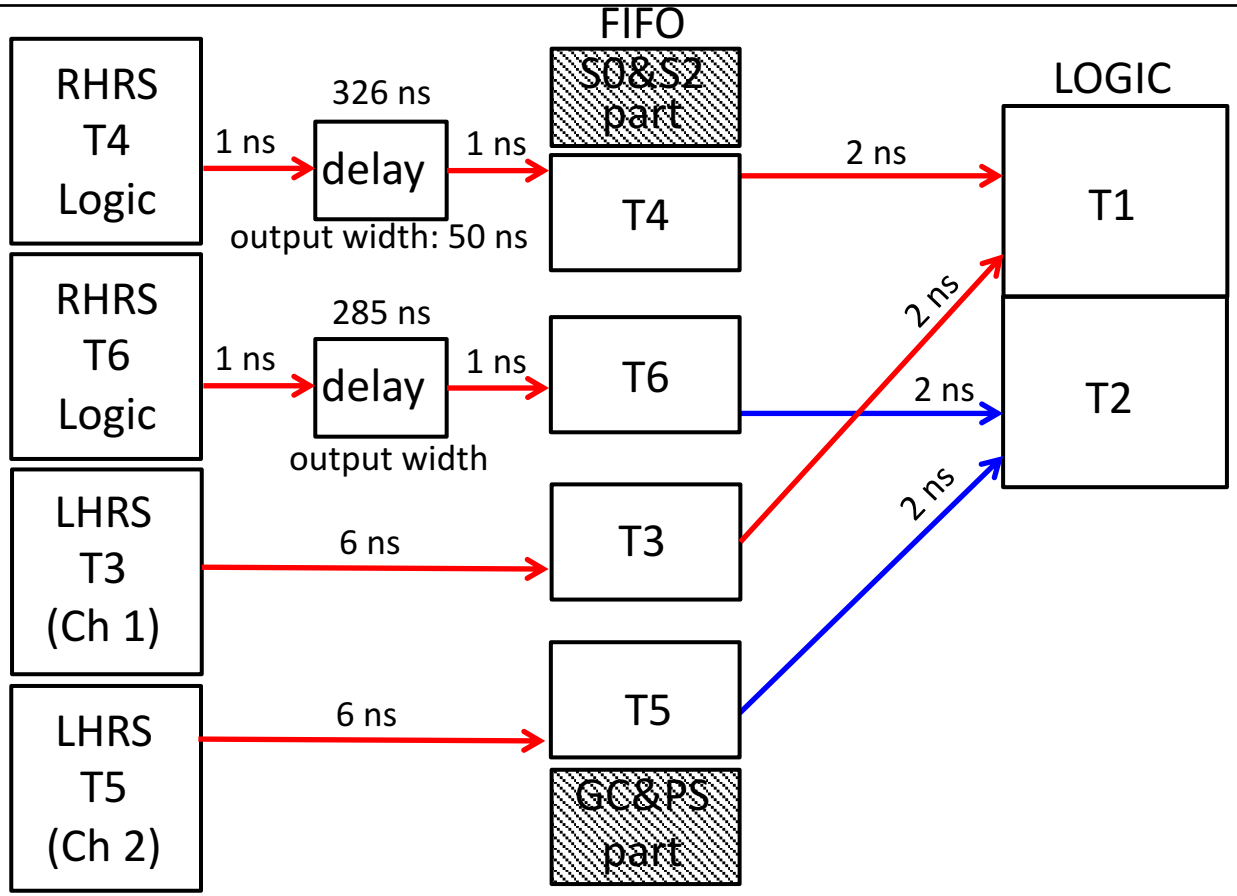
T2 coincidence

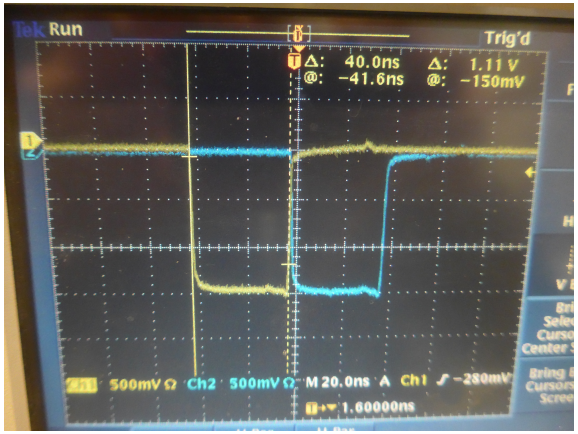
T5 (yellow)
T6 (blue)

→ Coincidence window and signal width changed later

→ Coincidence simulation with clock

Coincidence Schematics (on RHRS R3, N1)





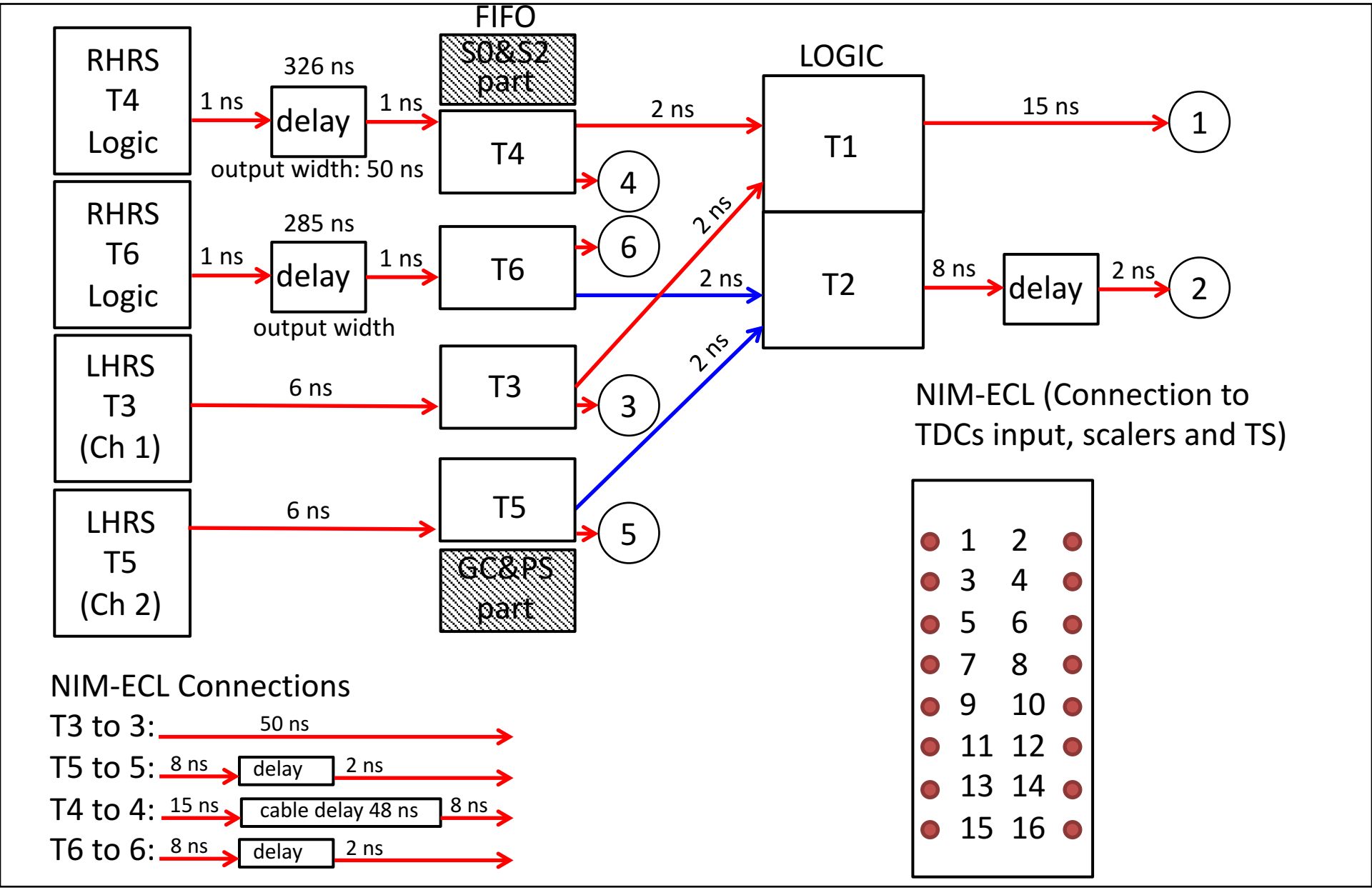
T1 (blue)
T2 (yellow)

→want to have other order

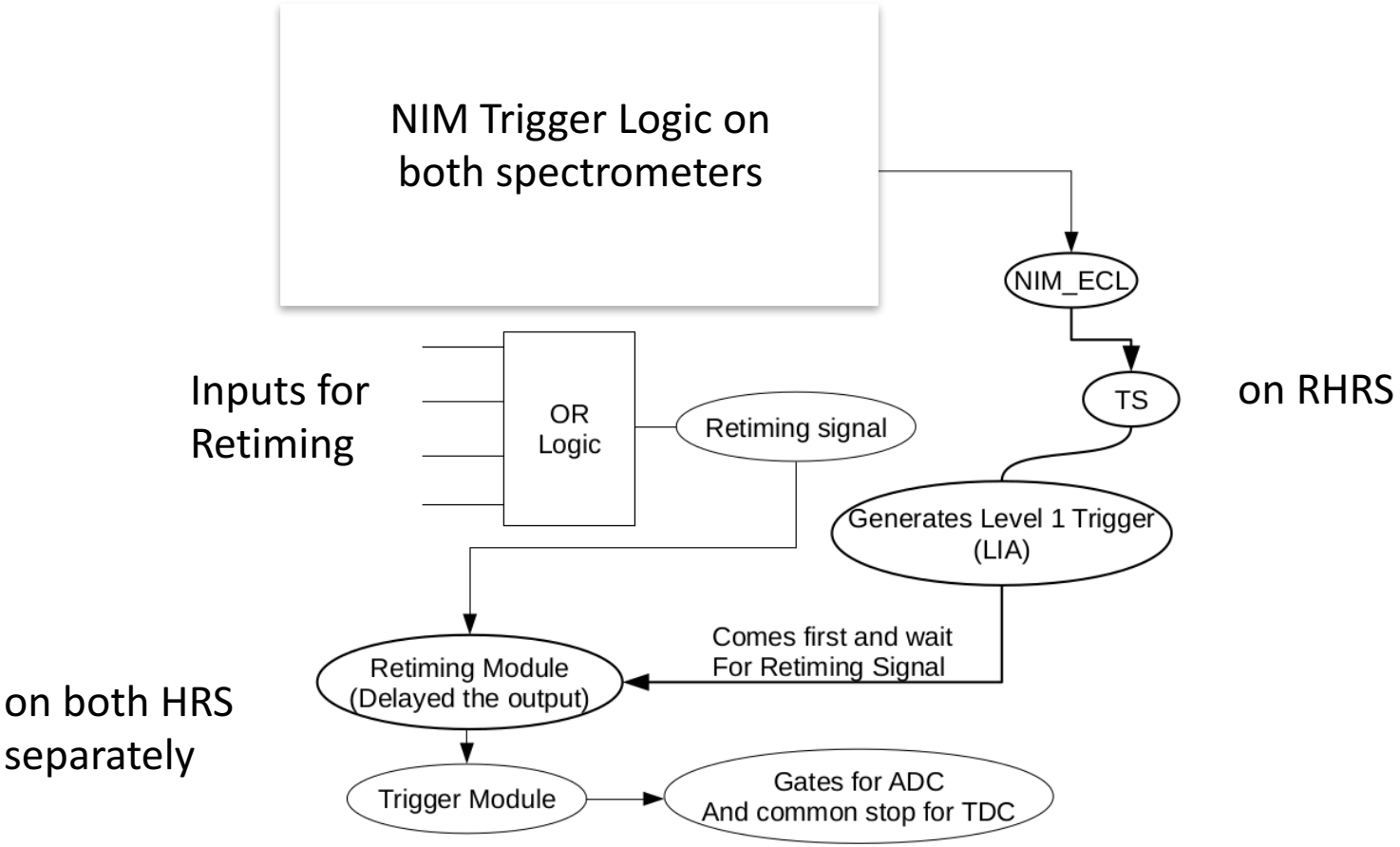
→ Delay of all trigger with respect to T1 to get order T1 – T3 – T2 – T5 – T4 – T6
→ Trigger Supervisor (TS) minimum time difference 10 ns
→ T3 – T1 = 10 ns, T2 – T3 = 15 ns, T5 – T2 = 15 ns, rest same
→ T6 – T1 = 70 ns (Note: By mistake the differences to T5 and T6 were smaller than wanted)

Delay: Delay generator

Coincidence Schematics (continued)



Delay: Delay generator


NIM Trigger Logic on
both spectrometers
NIM_ECL
TS
on RHRS
Inputs for
Retiming
OR
Logic
Retiming signal
Generates Level 1 Trigger
(LIA)
Comes first and wait
For Retiming Signal
Retiming Module
(Delayed the output)
on both HRS
separately
Trigger Module
Gates for ADC
And common stop for TDC

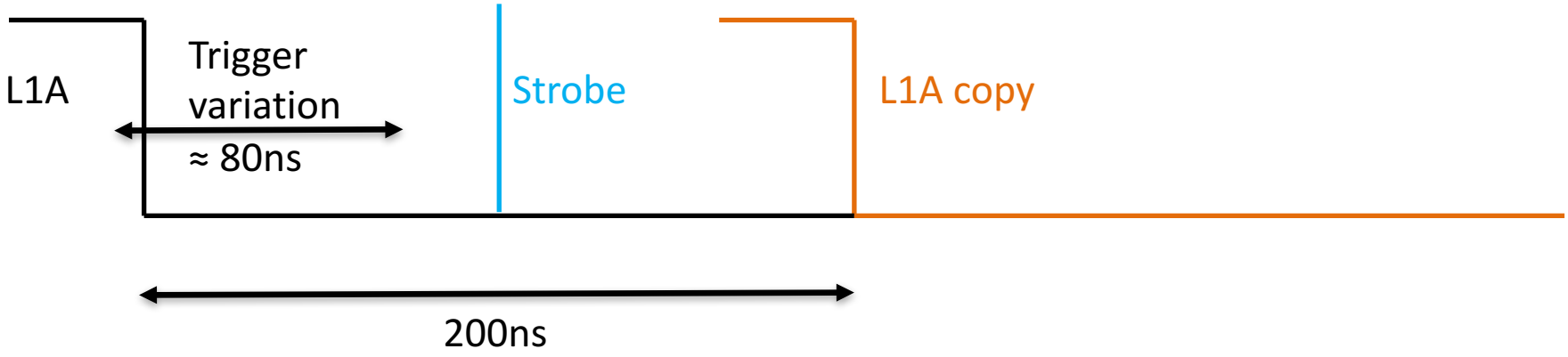
Retiming / Strobe Signal

- Why?
  - Common stop of TDC and ADC gate identical for same events i.e. one peak TDC spectrum
  - Can not be achieved when TDC stop results from L1A signal since it depends on the trigger delays
  - Use independent signal in detector for common stop and ADC
  - Ensure that common stop is existing even for events without a “real“ signal i.e. triggered by clock or only on one arm

Retiming / Strobe Signal continued

- How?
  - Use detector information to get common stop
  - Only one Strobe per event and spectrometer (RT module)
  - LHRS strobe: S0||S2 (S2 before S0)
  - RHRS strobe: T1 || T2 || T3 || T4 (could be improved)
  - Coincidence with L1A accept (RT module)
  - After 200 ns delayed copy of L1A for coincidence (according to DAQ manual)

Retiming / Strobe Signal continued



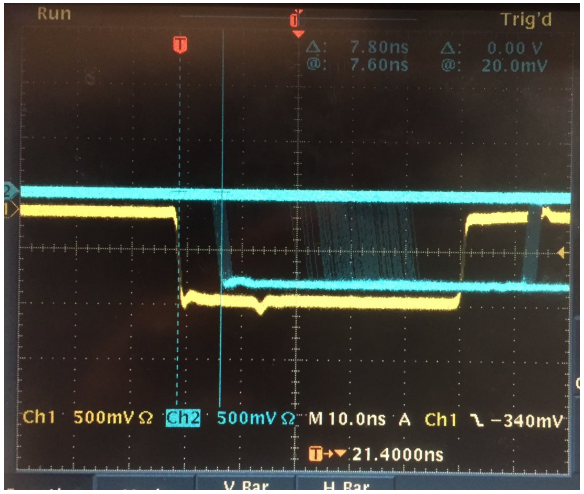
- Strobe between 100 ns to 200 ns after earliest trigger (T1)
- Random accidentals vary more but this gives only flat background → does not matter
- Common Stop for TDCs and ADC gate signal is derived from the upper coincidence signal

LHRS Strobe

S0||S2 = Strobe

S0 (blue)
S2 (yellow)

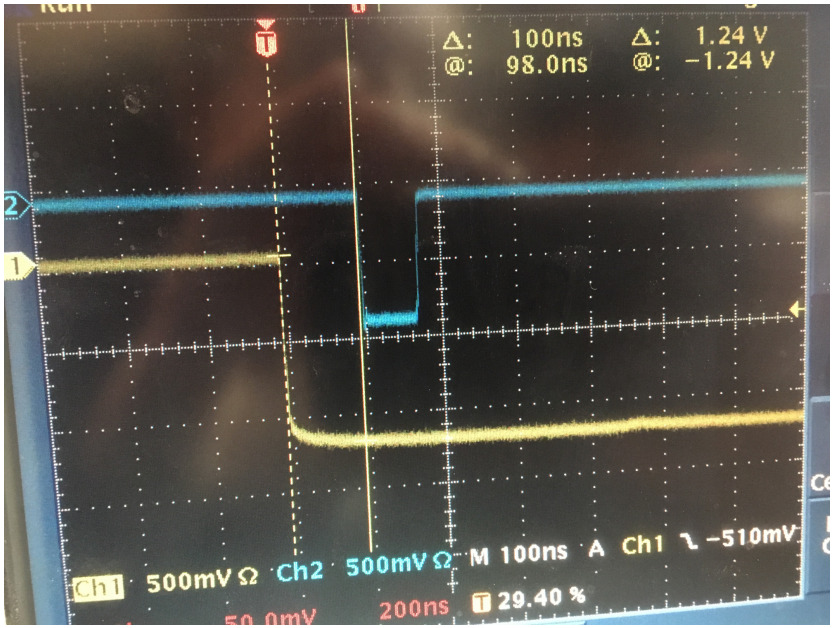
S2 defines time of strobe
Strobe is sent to delay generator for coincidence with L1A



L1A and Strobe Timing
Strobe (blue)
L1A (yellow), T3 trigger

Strobe 100ns after L1A (changed several times later)

Strobe (before delay) is sent to RHRS (ch 5) into TDC & scaler to get coincidence retiming → ideally L-strobe stopped by R-strobe



RHRS Strobe

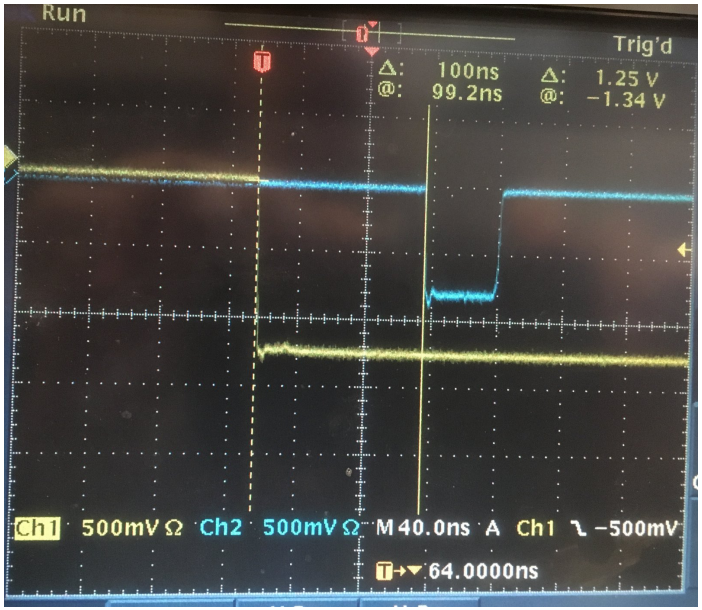
T1||T2||T3||T4 = Strobe

No picture available

L1A and Strobe Timing

Strobe (blue)
L1A (yellow), T4 trigger

Strobe 100ns after L1A (changed later)

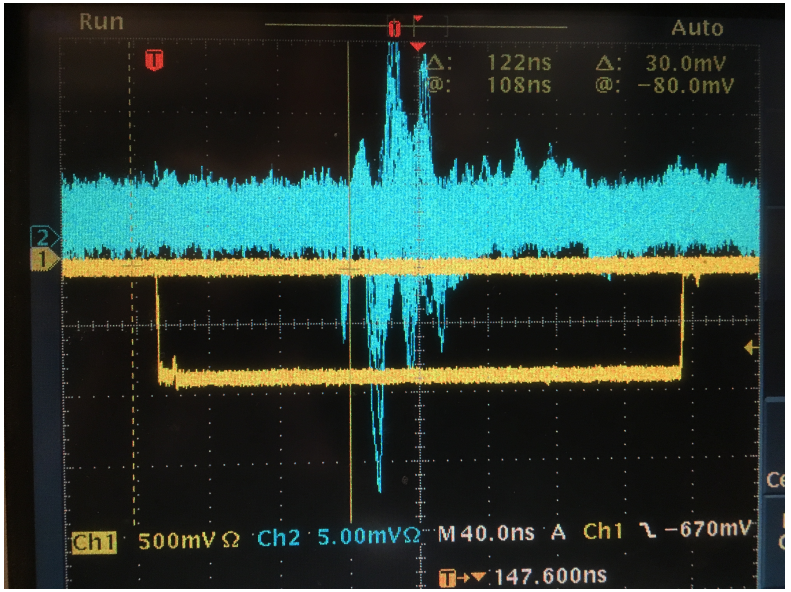


ADC Gates

LHRS Gate

S0 PMT signal (blue)
ADC gate (yellow)

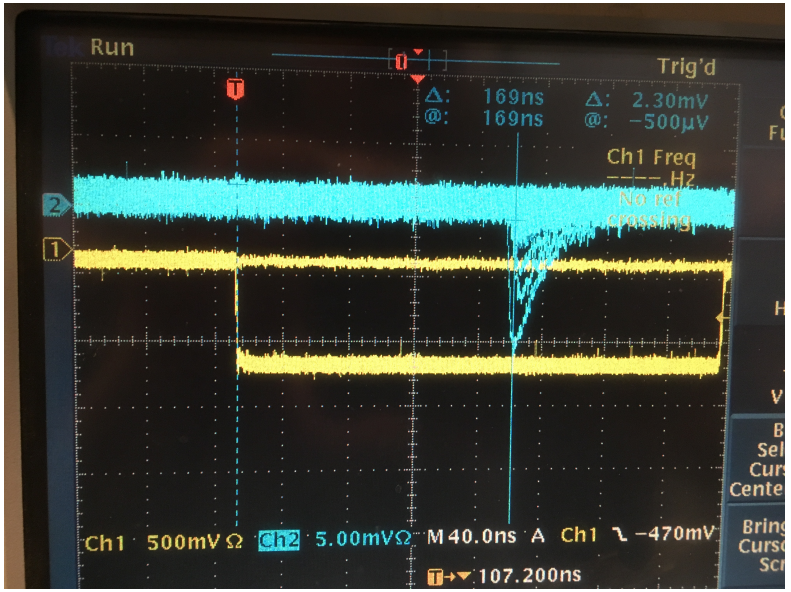
Broad ADC gate (>300ns)
Most of the signal is cross talk probably induced by EDTM (was better after we switched it off)



RHRS Gate

S0 PMT signal (blue)
ADC gate (yellow)

Change of ADC gate width to 400ns on **both arms** on 02/24/17



Outlook

- Overview over modifications through beam time
- Mistakes and what to avoid
- Further improvements for next beam times