(e,e‘K) Trigger Setup

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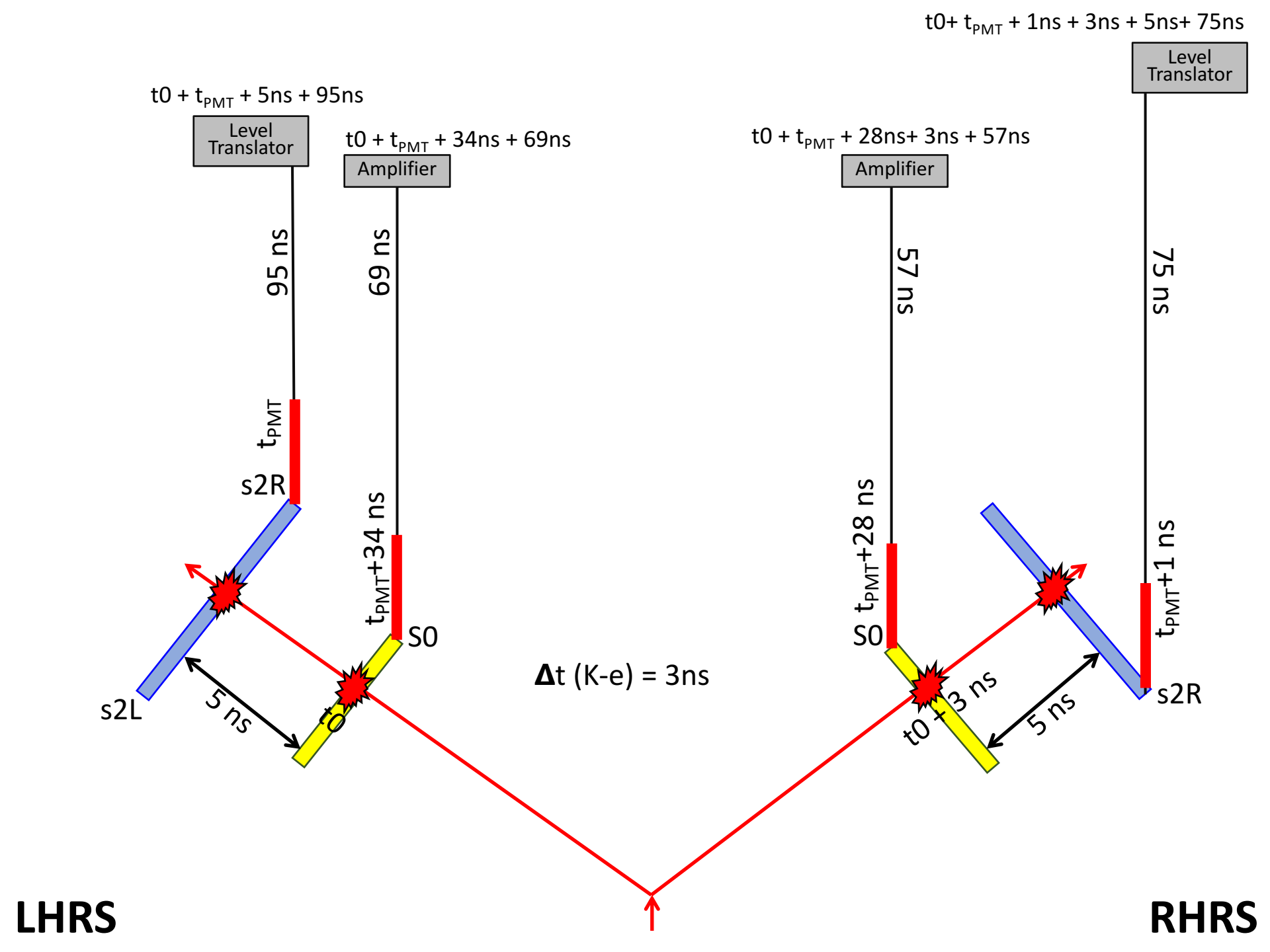
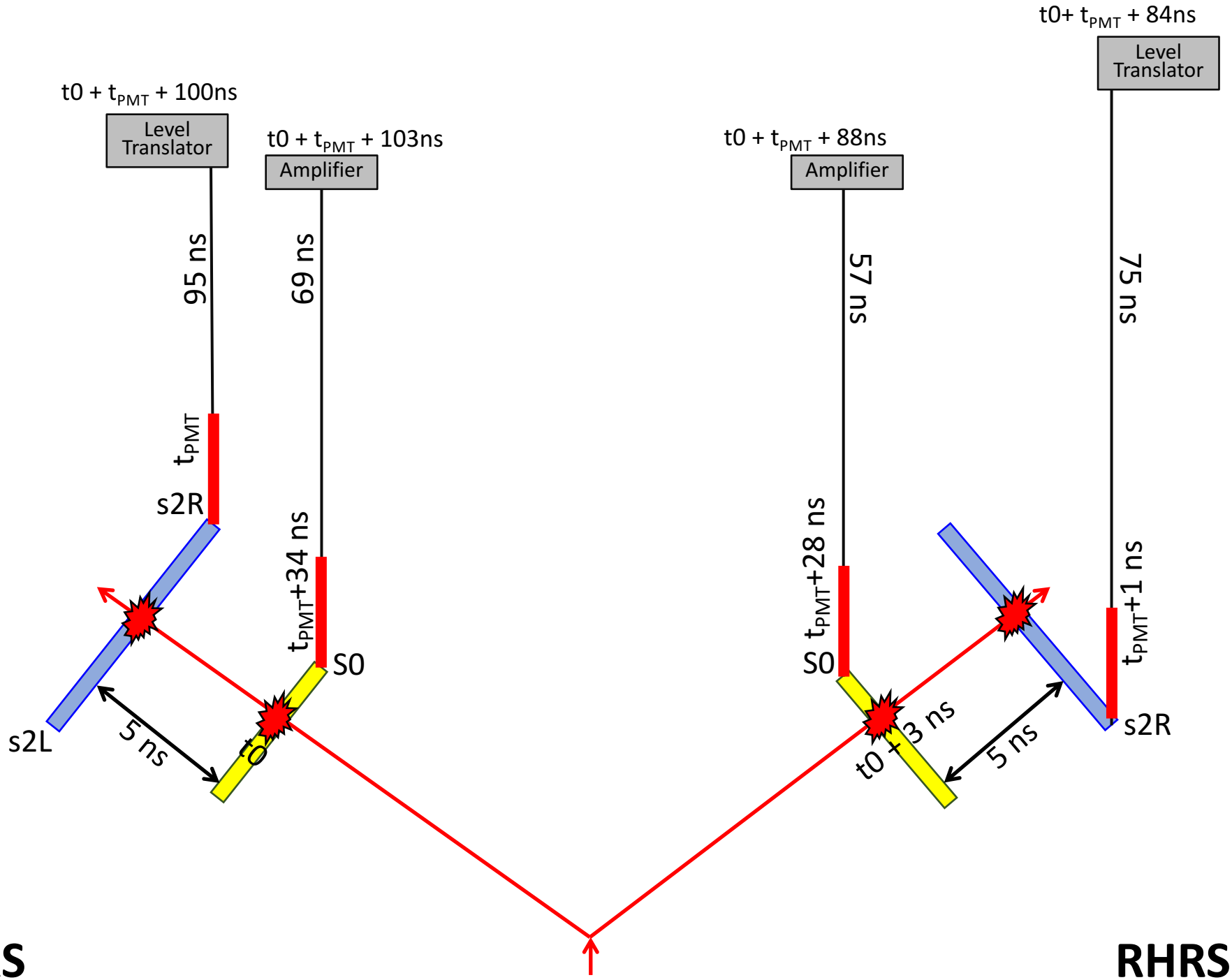
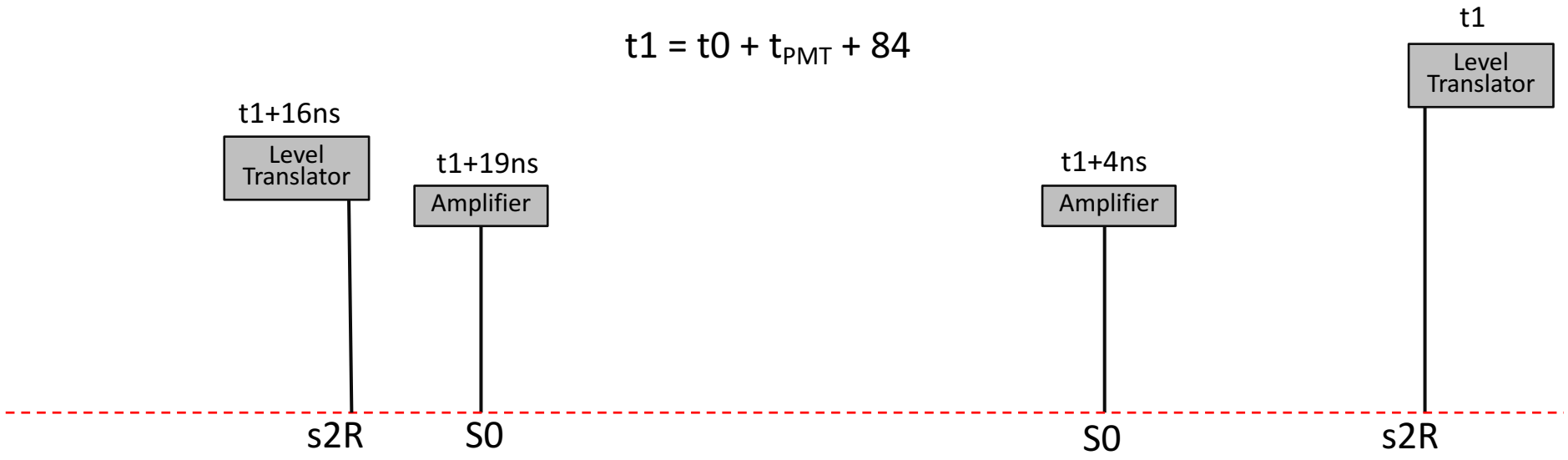
Considerations

- Main Trigger C1 = $(S0 \,\&\, S2)_L \,\&\, (S0 \,\&\, S2)_R$
- C2 = $(S0 \,\&\, S2\&GC)_L \,\&\, (S0 \,\&\, S2)_R$ as input but prescale=0
- Coincidence trigger window 150ns and T1/T2 40ns after $(S0 \,\&\, S2)_R$
- Kaons about 3ns later than Electrons on S0 (Protons ~10ns and Pions about ~0.2ns)
- Single Arm Triggers T1 = $(S0 \,\&\, S2)_L$, T3 = $(S0||S2) \,\&\, GC_L$ and T4 = $(S0 \,\&\, S2)_R$ prescaled
- Trigger time order: C1 < (C2) < T1 < T4 < T3 with Δt = 10ns between each input

FAKE COINCIDENCE SETUP

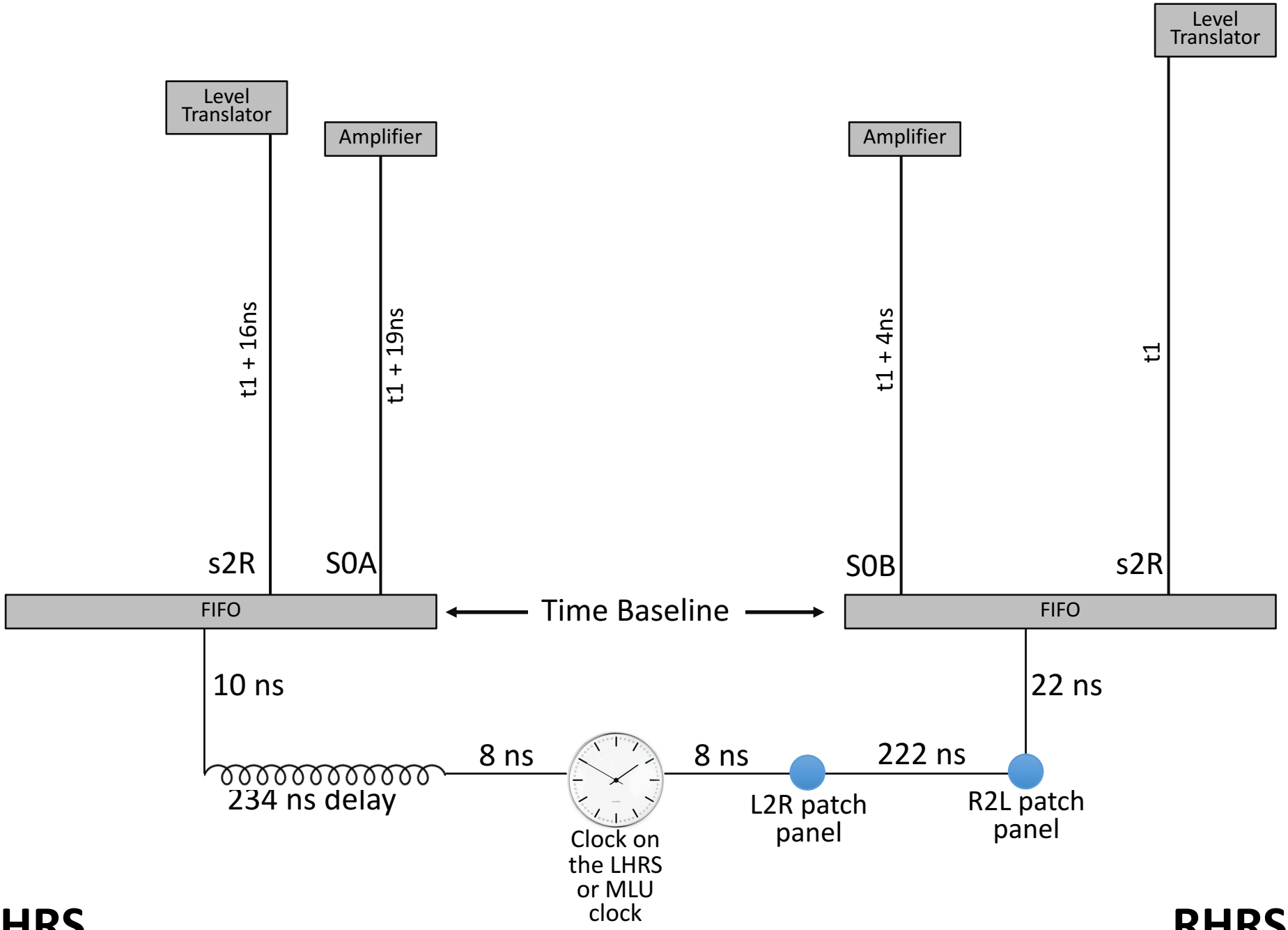

t0 + tPMT + 5ns + 95ns
Level Translator
95 ns
tPMT
s2R
s2L
5 ns
t0 + tPMT + 34ns + 69ns
Amplifier
69 ns
tPMT+34 ns
S0
t0
Δt (K-e) = 3ns
t0+ tPMT + 1ns + 3ns + 5ns+ 75ns
Level Translator
75 ns
tPMT+1 ns
s2R
5 ns
t0 + 3 ns
t0 + tPMT + 28ns+ 3ns + 57ns
Amplifier
57 ns
tPMT+28 ns
S0
LHRS
RHRS

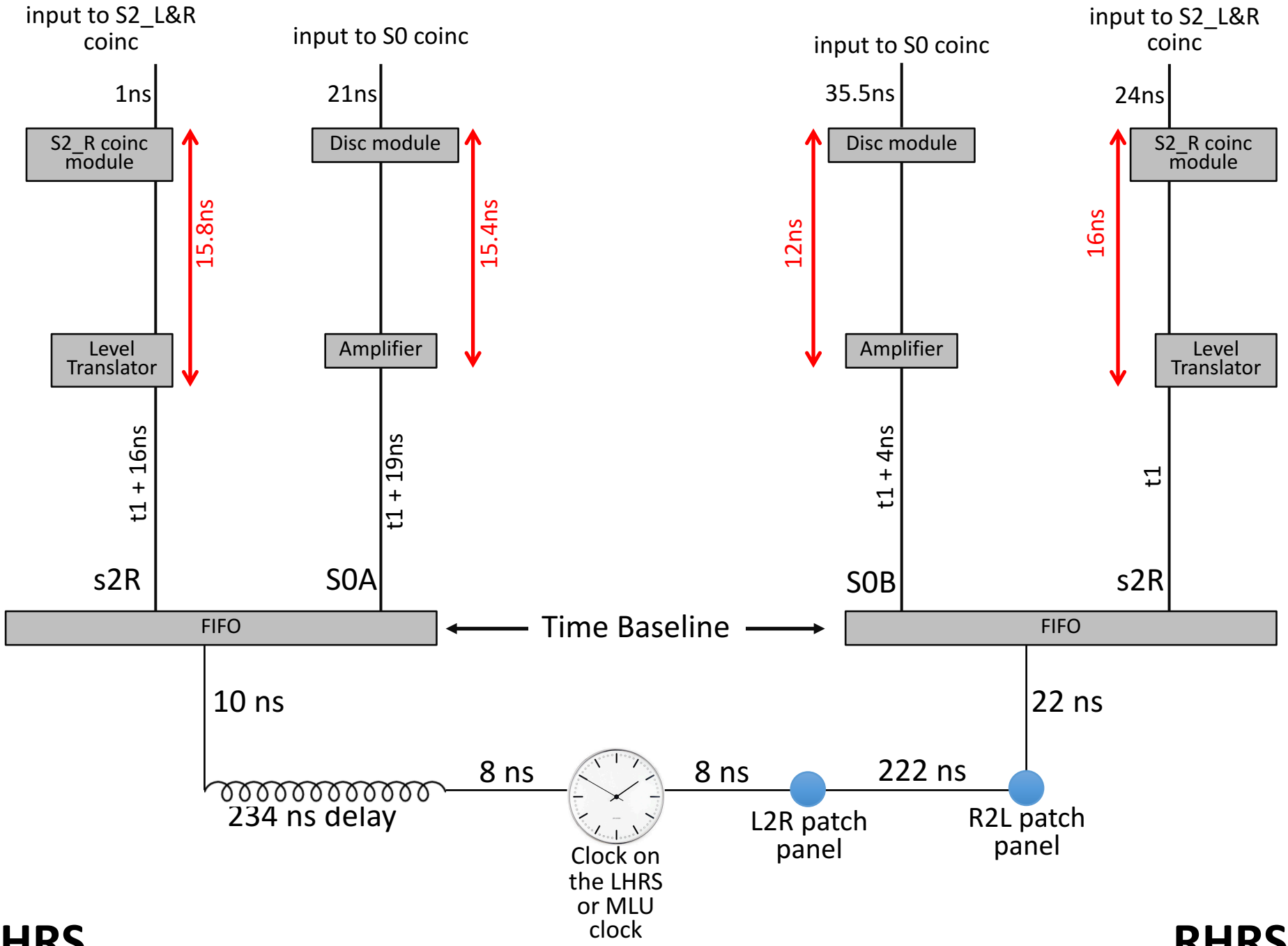

t0 + tPMT + 100ns
Level Translator
95 ns
tPMT
s2R
s2L
5 ns
t0 + tPMT + 103ns
Amplifier
69 ns
tPMT+34 ns
S0
t0
t0+ tPMT + 84ns
Level Translator
75 ns
tPMT+1 ns
s2R
t0 + tPMT + 88ns
Amplifier
57 ns
tPMT+28 ns
S0
t0 + 3 ns
5 ns
LHRS
RHRS

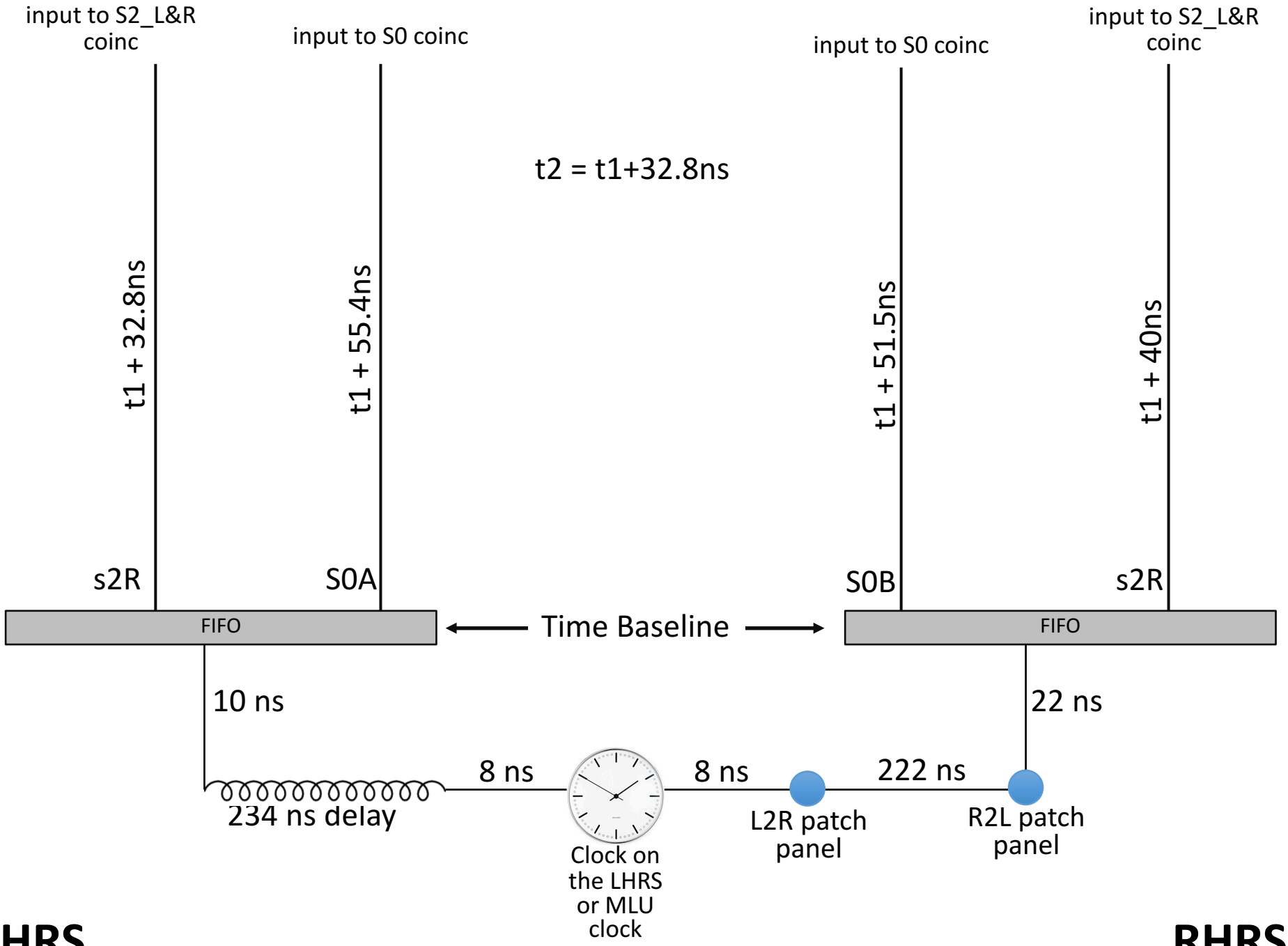

$t1 = t0 + t_{PMT} + 84$
t1
Level Translator
t1+16ns
Level Translator
t1+19ns
Amplifier
t1+4ns
Amplifier
s2R
S0
S0
s2R

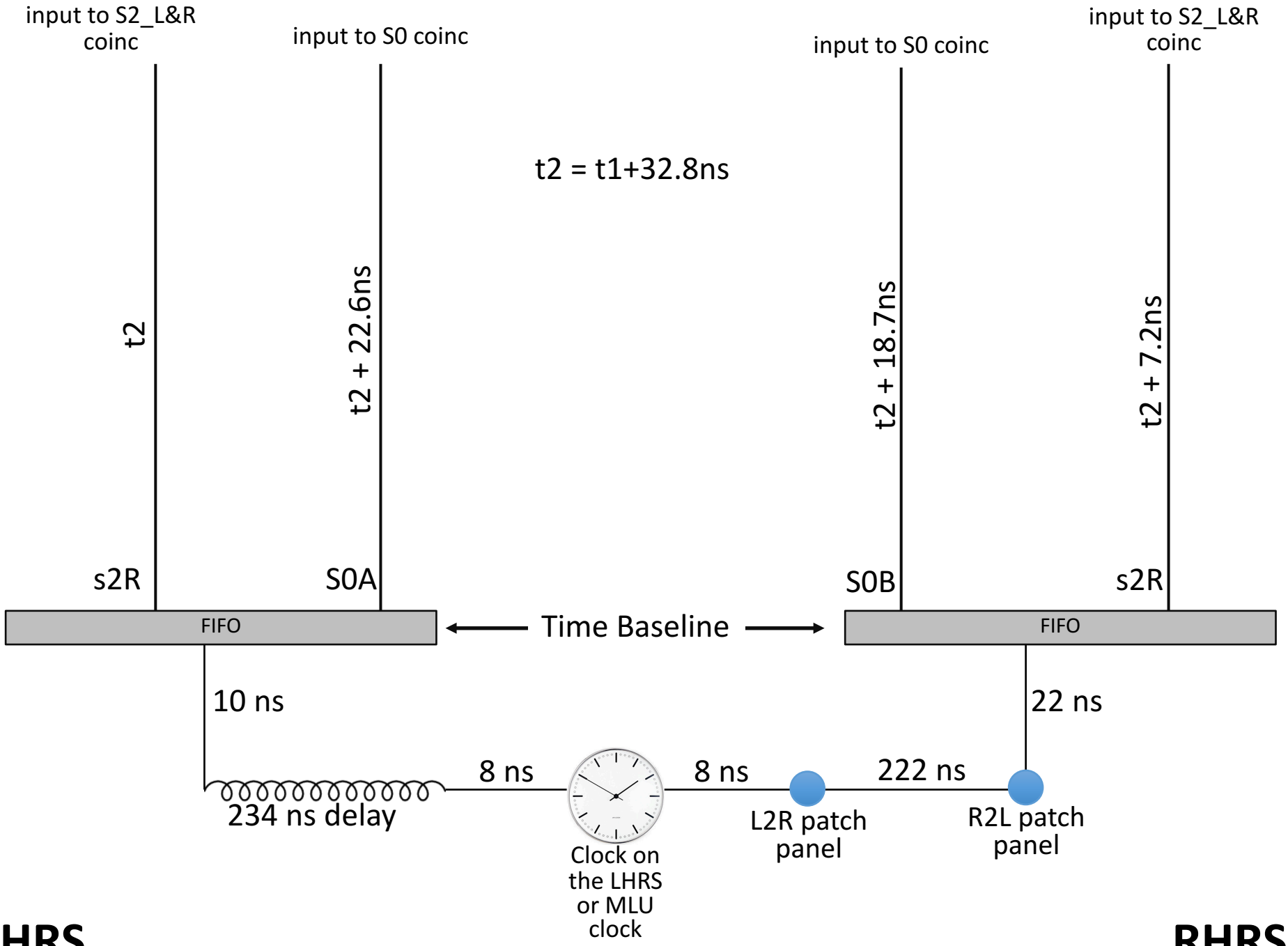
LHRS

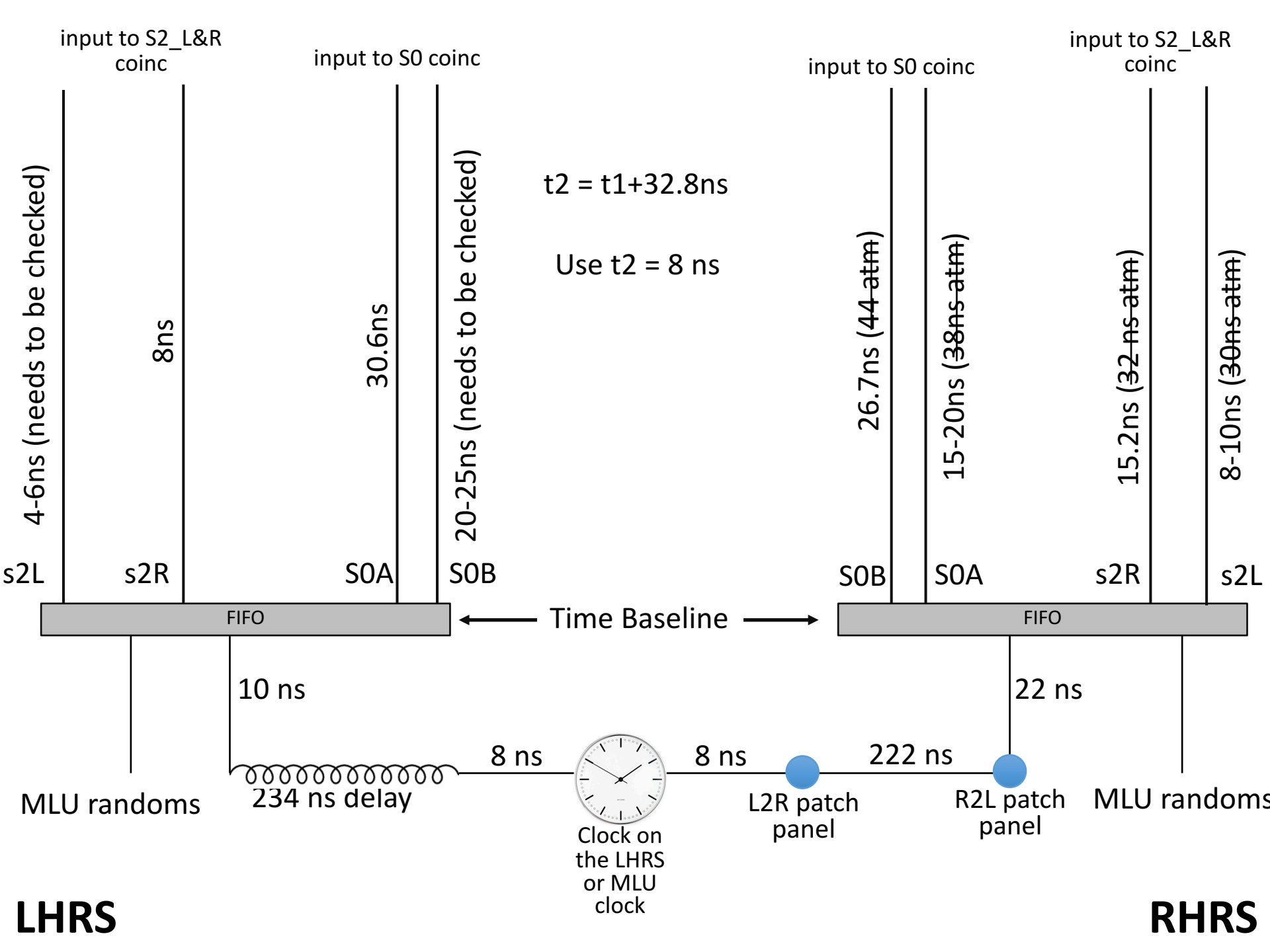
RHRS


Level Translator
Amplifier
Amplifier
Level Translator
t1 + 16ns
t1 + 19ns
t1 + 4ns
t1
s2R
S0A
S0B
s2R
FIFO
Time Baseline
FIFO
10 ns
22 ns
8 ns
8 ns
222 ns
234 ns delay
Clock on the LHRS or MLU clock
L2R patch panel
R2L patch panel
LHRS
RHRS

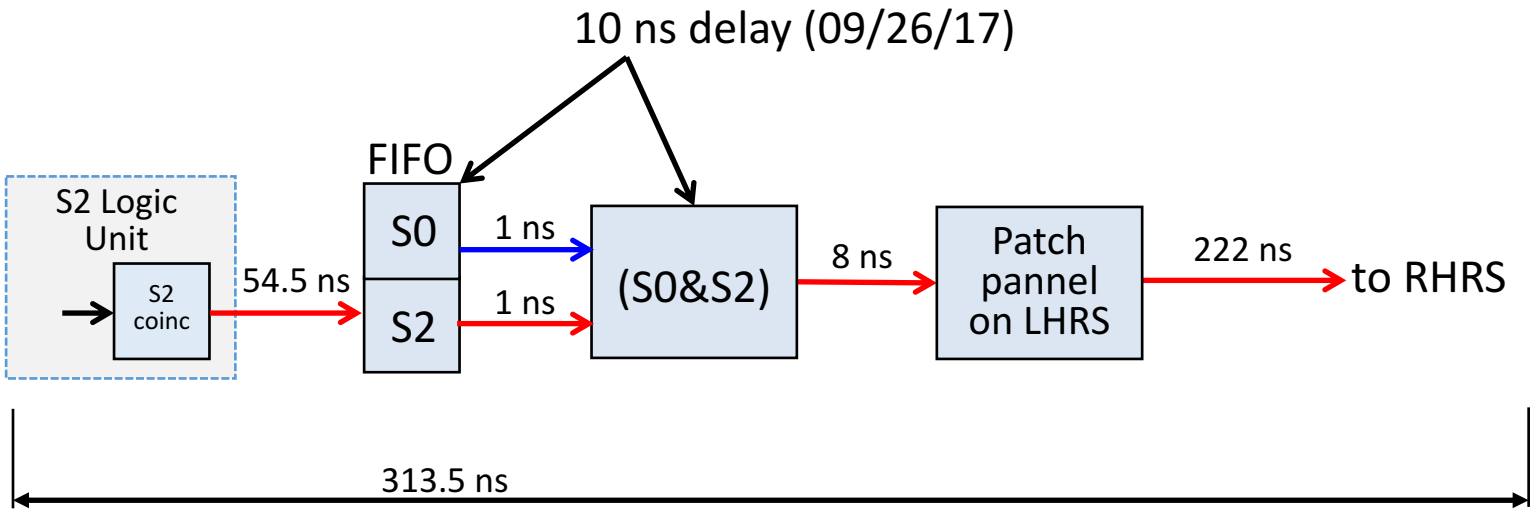

input to S2_L&R coinc
1ns
S2_R coinc module
15.8ns
Level Translator
t1 + 16ns
s2R
input to S0 coinc
21ns
Disc module
15.4ns
Amplifier
t1 + 19ns
S0A
FIFO
Time Baseline
input to S0 coinc
35.5ns
Disc module
12ns
Amplifier
t1 + 4ns
S0B
FIFO
input to S2_L&R coinc
24ns
S2_R coinc module
16ns
Level Translator
t1
s2R
10 ns
8 ns
234 ns delay
Clock on the LHRS or MLU clock
8 ns
L2R patch panel
222 ns
R2L patch panel
22 ns
LHRS
RHRS


input to S2_L&R coinc
input to S0 coinc
input to S0 coinc
input to S2_L&R coinc
t2 = t1+32.8ns
t1 + 32.8ns
t1 + 55.4ns
t1 + 51.5ns
t1 + 40ns
s2R
S0A
S0B
s2R
FIFO
Time Baseline
FIFO
10 ns
22 ns
8 ns
8 ns
222 ns
234 ns delay
Clock on the LHRS or MLU clock
L2R patch panel
R2L patch panel
LHRS
RHRS

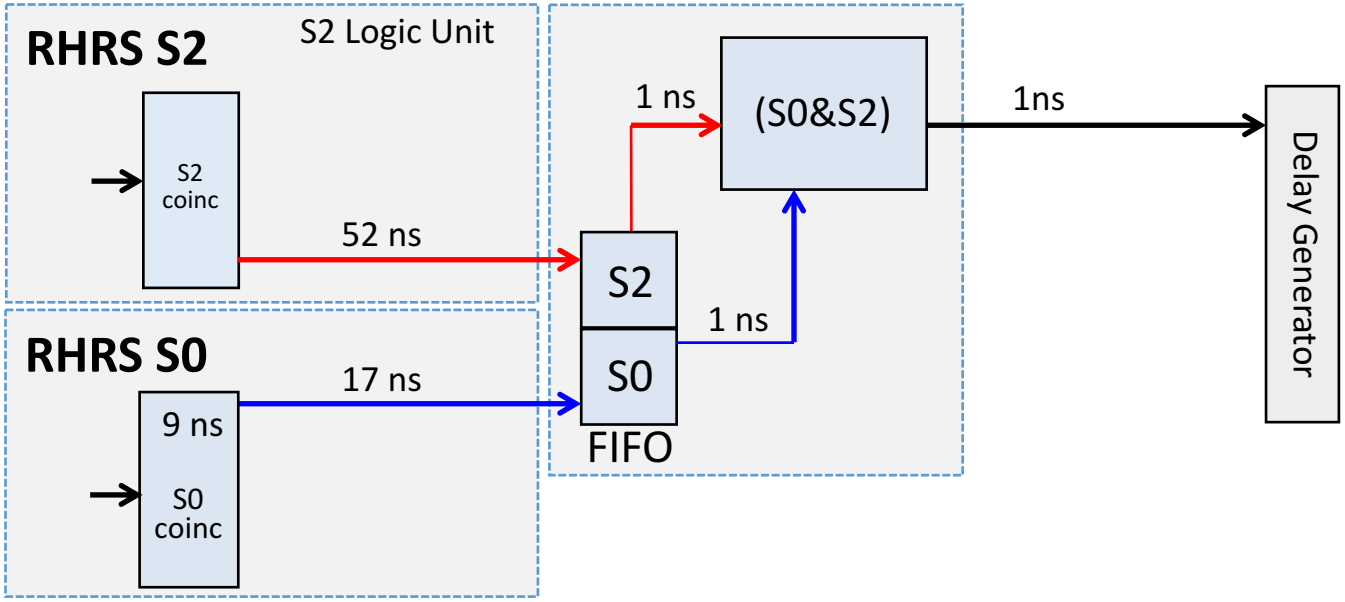

input to S2_L&R coinc
input to S0 coinc
input to S0 coinc
input to S2_L&R coinc
t2 = t1+32.8ns
t2
t2 + 22.6ns
t2 + 18.7ns
t2 + 7.2ns
s2R
S0A
S0B
s2R
FIFO
Time Baseline
FIFO
10 ns
22 ns
8 ns
8 ns
222 ns
234 ns delay
Clock on the LHRS or MLU clock
L2R patch panel
R2L patch panel
LHRS
RHRS


input to S2_L&R coinc
input to S0 coinc
input to S0 coinc
input to S2_L&R coinc
4-6ns (needs to be checked)
8ns
30.6ns
20-25ns (needs to be checked)
t2 = t1+32.8ns
Use t2 = 8 ns
26.7ns (44 atm)
15-20ns (38ns atm)
15.2ns (32 ns atm)
8-10ns (30ns atm)
s2L
s2R
S0A
S0B
S0B
S0A
s2R
s2L
FIFO
Time Baseline
FIFO
10 ns
22 ns
8 ns
8 ns
222 ns
MLU randoms
234 ns delay
Clock on the LHRS or MLU clock
L2R patch panel
R2L patch panel
MLU randoms
LHRS
RHRS

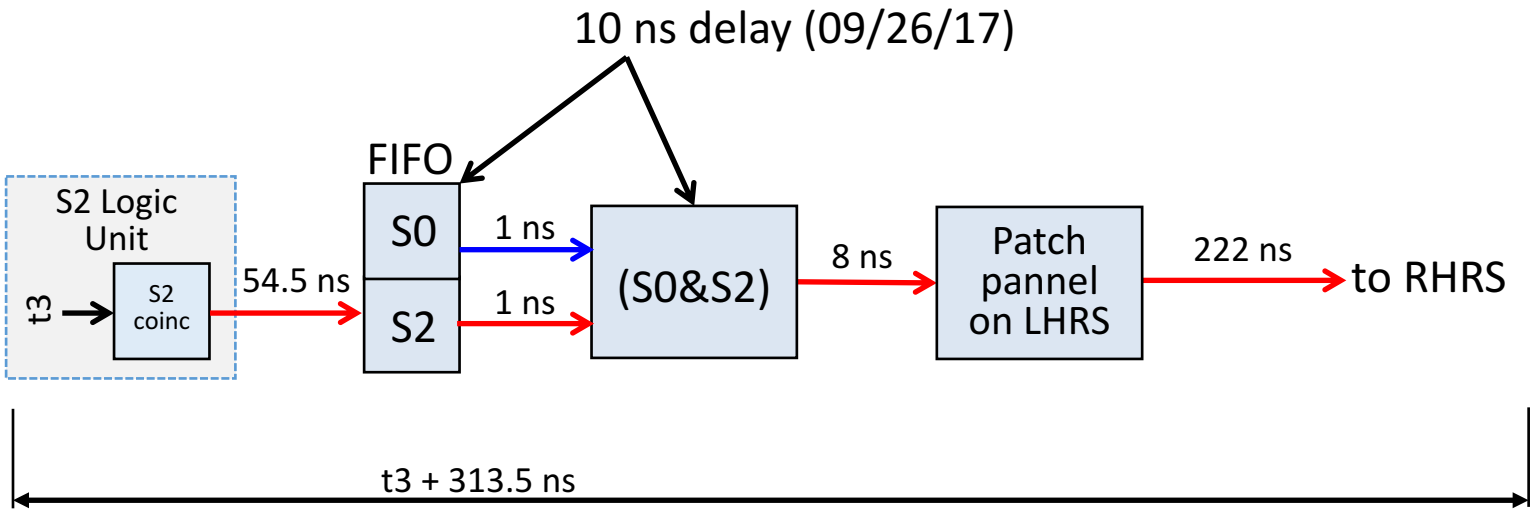
LHRS


10 ns delay (09/26/17)
FIFO
S2 Logic Unit
S2 coinc
54.5 ns
S0
S2
1 ns
1 ns
(S0&S2)
8 ns
Patch pannel on LHRS
222 ns
to RHRS
313.5 ns

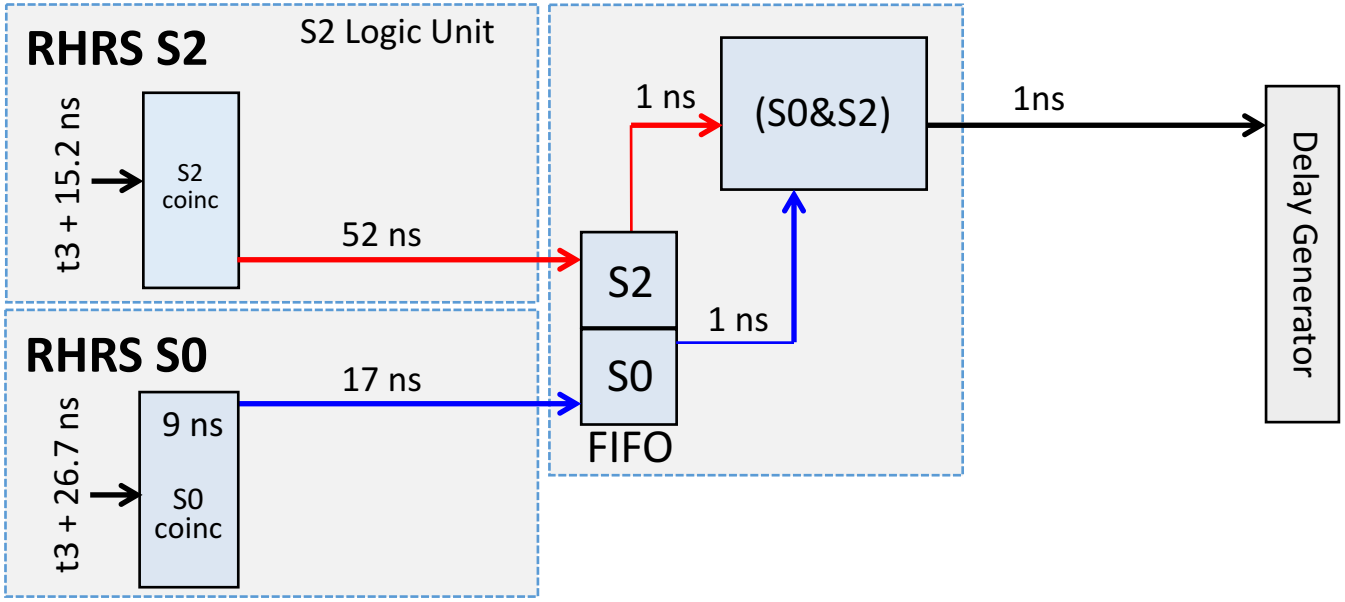
RHRS

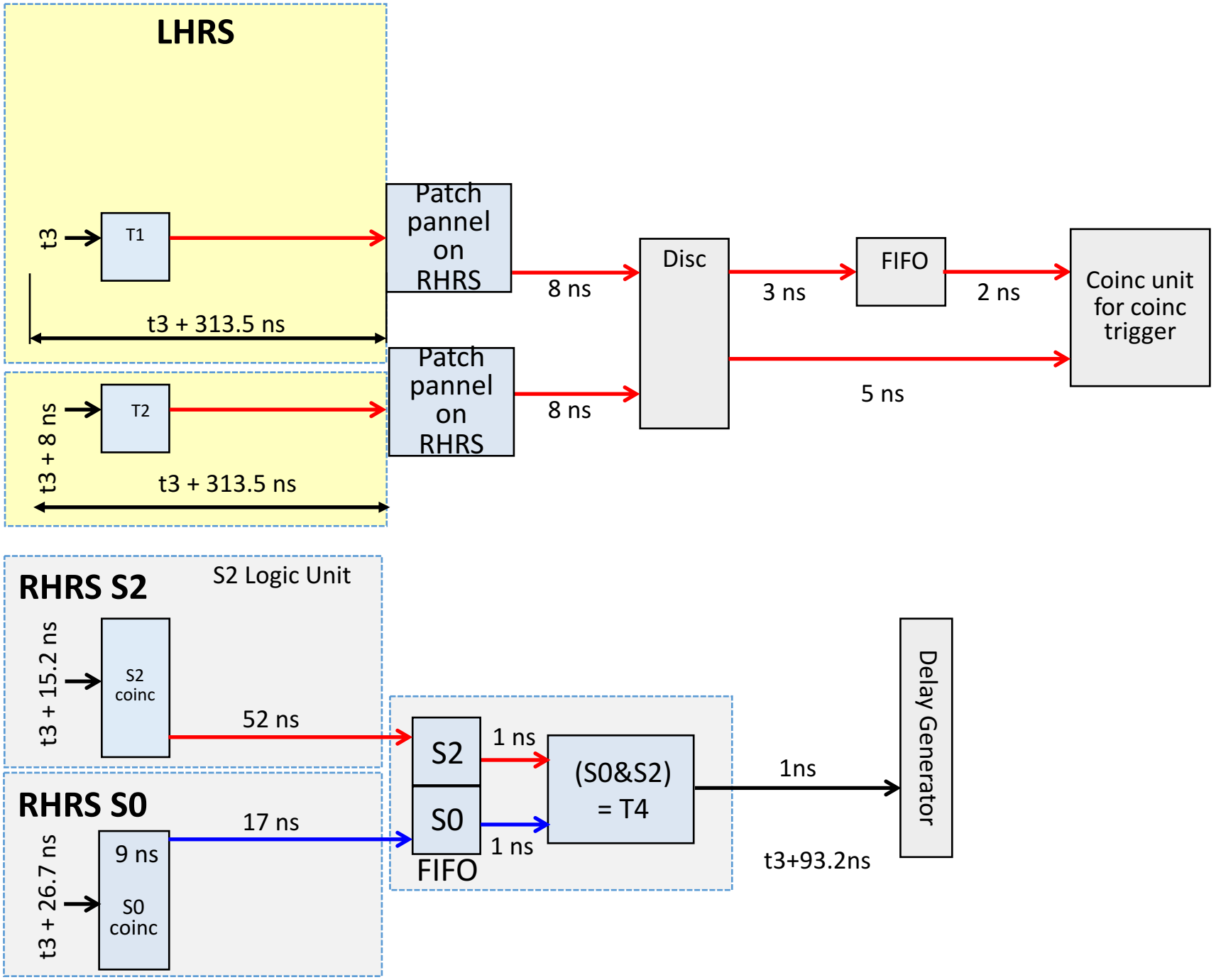

RHRS S2
S2 Logic Unit
S2 coinc
52 ns
RHRS S0
17 ns
9 ns
S0 coinc
1 ns
(S0&S2)
1ns
S2
1 ns
S0
FIFO
Delay Generator

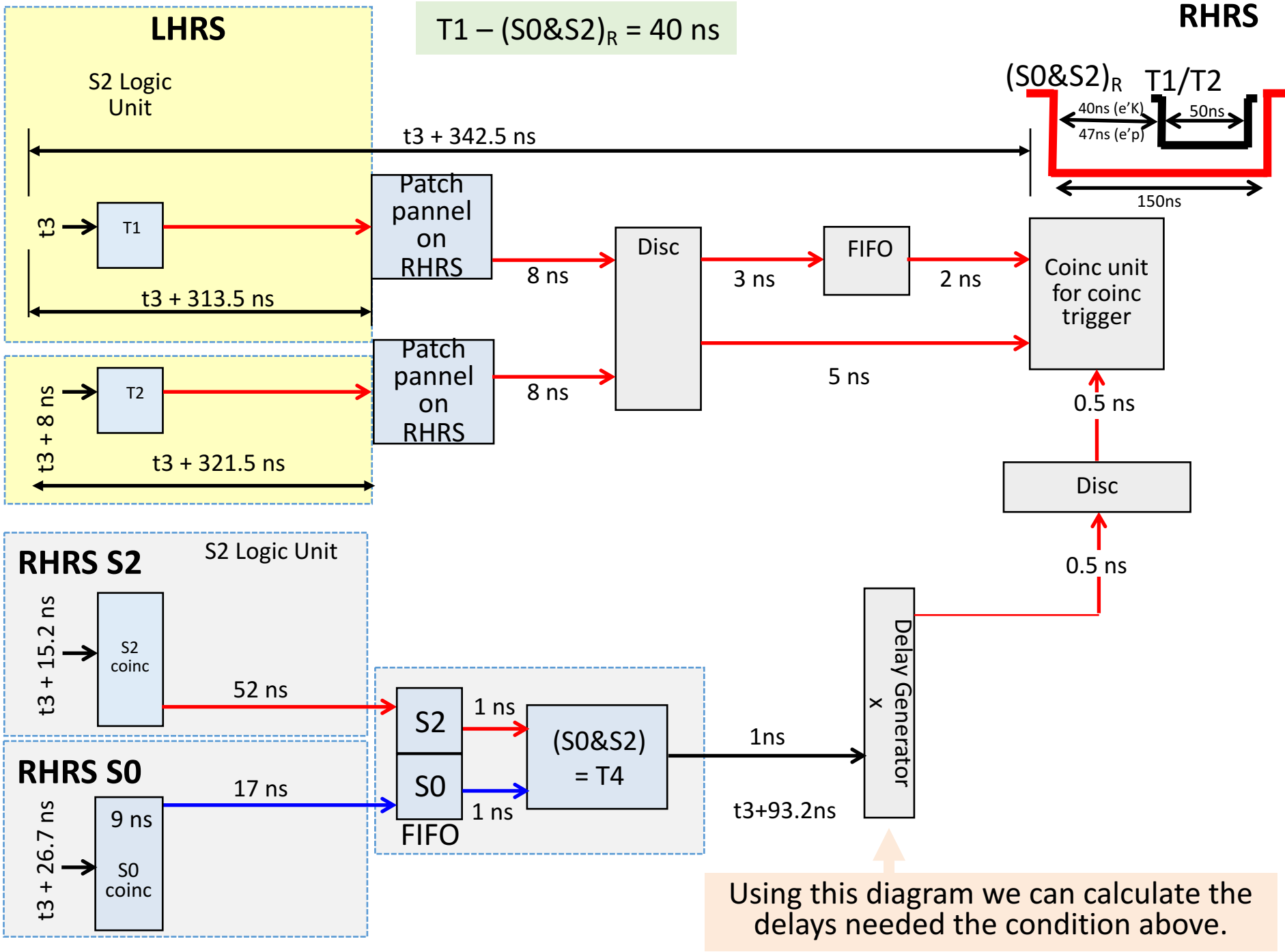
LHRS


10 ns delay (09/26/17)
FIFO
S2 Logic Unit
t3
S2 coinc
54.5 ns
S0
S2
1 ns
1 ns
(S0&S2)
8 ns
Patch pannel on LHRS
222 ns
to RHRS
t3 + 313.5 ns

RHRS


RHRS S2
S2 Logic Unit
t3 + 15.2 ns
S2 coinc
52 ns
RHRS S0
t3 + 26.7 ns
9 ns
S0 coinc
17 ns
1 ns
(S0&S2)
1ns
S2
S0
1 ns
FIFO
Delay Generator


RHRS
LHRS
t3
T1
t3 + 313.5 ns
Patch pannel on RHRS
8 ns
Disc
3 ns
FIFO
2 ns
Coinc unit for coinc trigger
5 ns
t3 + 8 ns
T2
t3 + 313.5 ns
Patch pannel on RHRS
8 ns
RHRS S2
S2 Logic Unit
t3 + 15.2 ns
S2 coinc
52 ns
RHRS S0
t3 + 26.7 ns
9 ns
S0 coinc
17 ns
S2
S0
FIFO
1 ns
1 ns
(S0&S2) = T4
1ns
t3+93.2ns
Delay Generator


LHRS
S2 Logic Unit
t3
T1
t3 + 313.5 ns
t3 + 342.5 ns
Patch pannel on RHRS
8 ns
Disc
3 ns
FIFO
2 ns
Coinc unit for coinc trigger
T2
t3 + 8 ns
t3 + 321.5 ns
Patch pannel on RHRS
8 ns
5 ns
0.5 ns
Disc
0.5 ns
RHRS
(S0&S2)R
T1/T2
40ns (e'K)
47ns (e'p)
50ns
150ns
T1 – (S0&S2)R = 40 ns
RHRS S2
S2 Logic Unit
t3 + 15.2 ns
S2 coinc
52 ns
RHRS S0
t3 + 26.7 ns
9 ns
S0 coinc
17 ns
S2
S0
1 ns
1 ns
FIFO
(S0&S2) = T4
1ns
t3+93.2ns
Delay Generator x
Using this diagram we can calculate the delays needed the condition above.

Prediction for the delays on RHRS for coinc trigger

C1:
C2

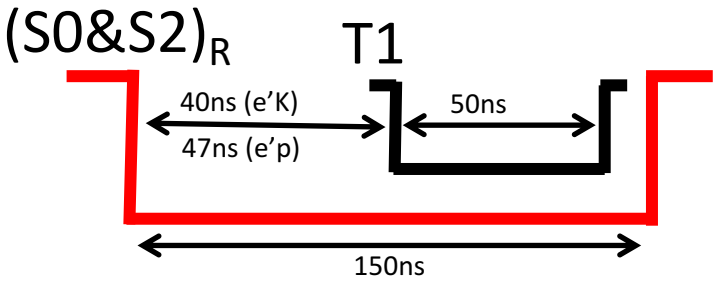
Need to set delay in RHRS delay generator for S0&S2 (RHRS) to:

$$t3 + 342.5 - (t3 + 93.2 + x + 0.5 + 8 + 0.5)\ ns = 40\ ns$$

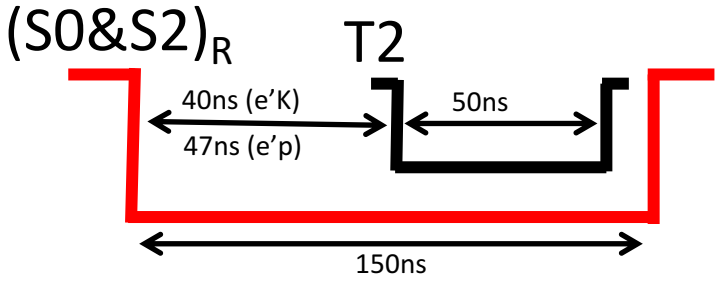
$$x = 200.3\ ns \approx 200\ ns$$

Coincidence triggers

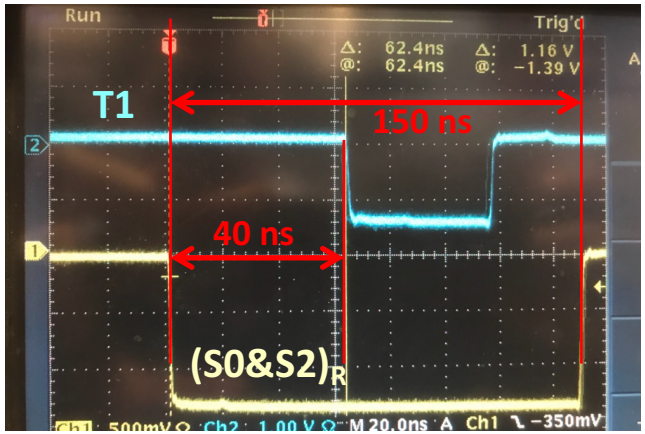
C1:

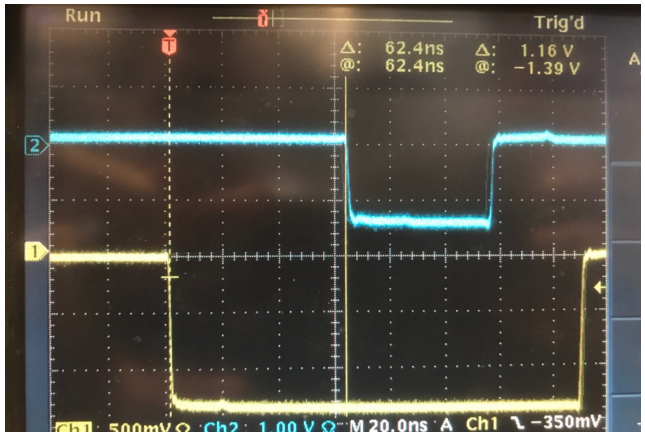


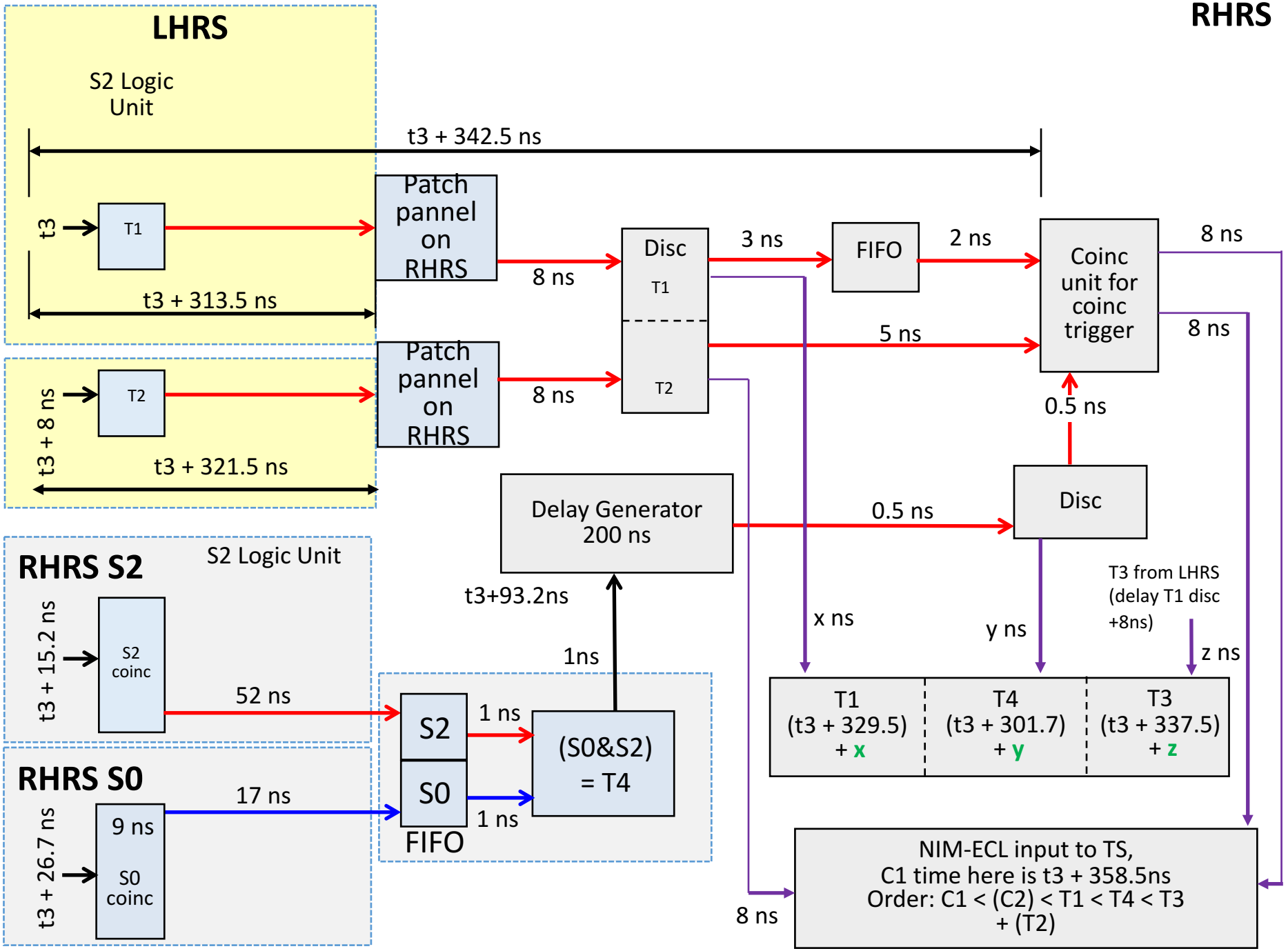
C2:



Picture from (e,e'p)






LHRS
RHRS
S2 Logic Unit
t3 + 342.5 ns
t3
T1
t3 + 313.5 ns
Patch pannel on RHRS
8 ns
Disc
T1
T2
3 ns
FIFO
2 ns
Coinc unit for coinc trigger
8 ns
8 ns
5 ns
t3 + 8 ns
T2
t3 + 321.5 ns
Patch pannel on RHRS
8 ns
0.5 ns
Delay Generator 200 ns
0.5 ns
Disc
RHRS S2
S2 Logic Unit
t3 + 15.2 ns
S2 coinc
52 ns
t3+93.2ns
1ns
T3 from LHRS (delay T1 disc +8ns)
x ns
y ns
z ns
S2
S0
1 ns
1 ns
FIFO
(S0&S2) = T4
T1 (t3 + 329.5) + x
T4 (t3 + 301.7) + y
T3 (t3 + 337.5) + z
RHRS S0
17 ns
t3 + 26.7 ns
9 ns
S0 coinc
8 ns
NIM-ECL input to TS,
C1 time here is t3 + 358.5ns
Order: C1 < (C2) < T1 < T4 < T3 + (T2)

Calculated Trigger Inputs Delays

C1-T1 = -10ns:

$$t3 + 358.5 - (t3 + 329.5 + x)\ ns = -10\ ns$$
$$x = 39\ ns \approx 40\ ns$$

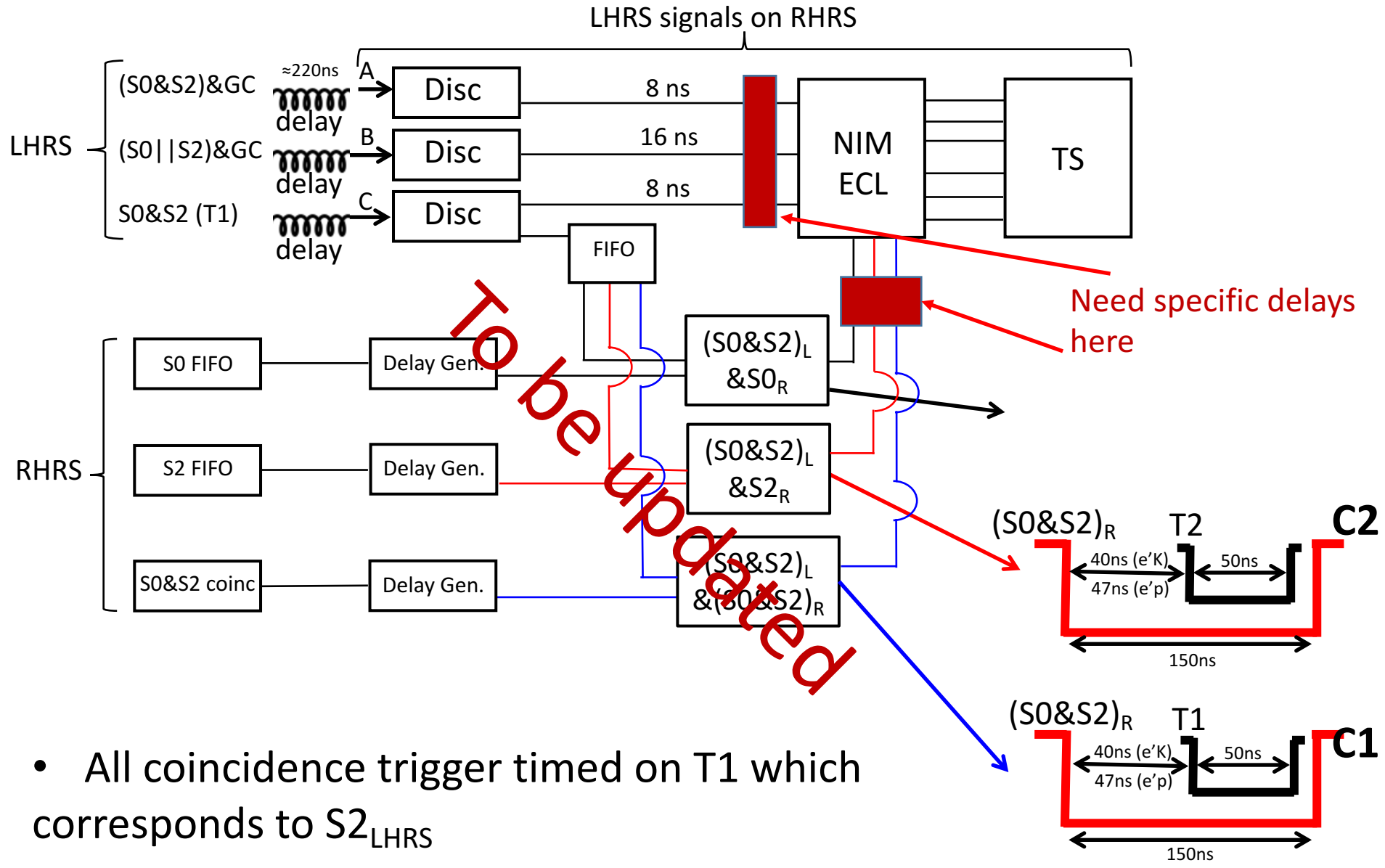
C1-T4 = -20ns:

$$t3 + 358.5 - (t3 + 301.7 + y)\ ns = -20\ ns$$
$$y = 76.8\ ns \approx 77\ ns$$

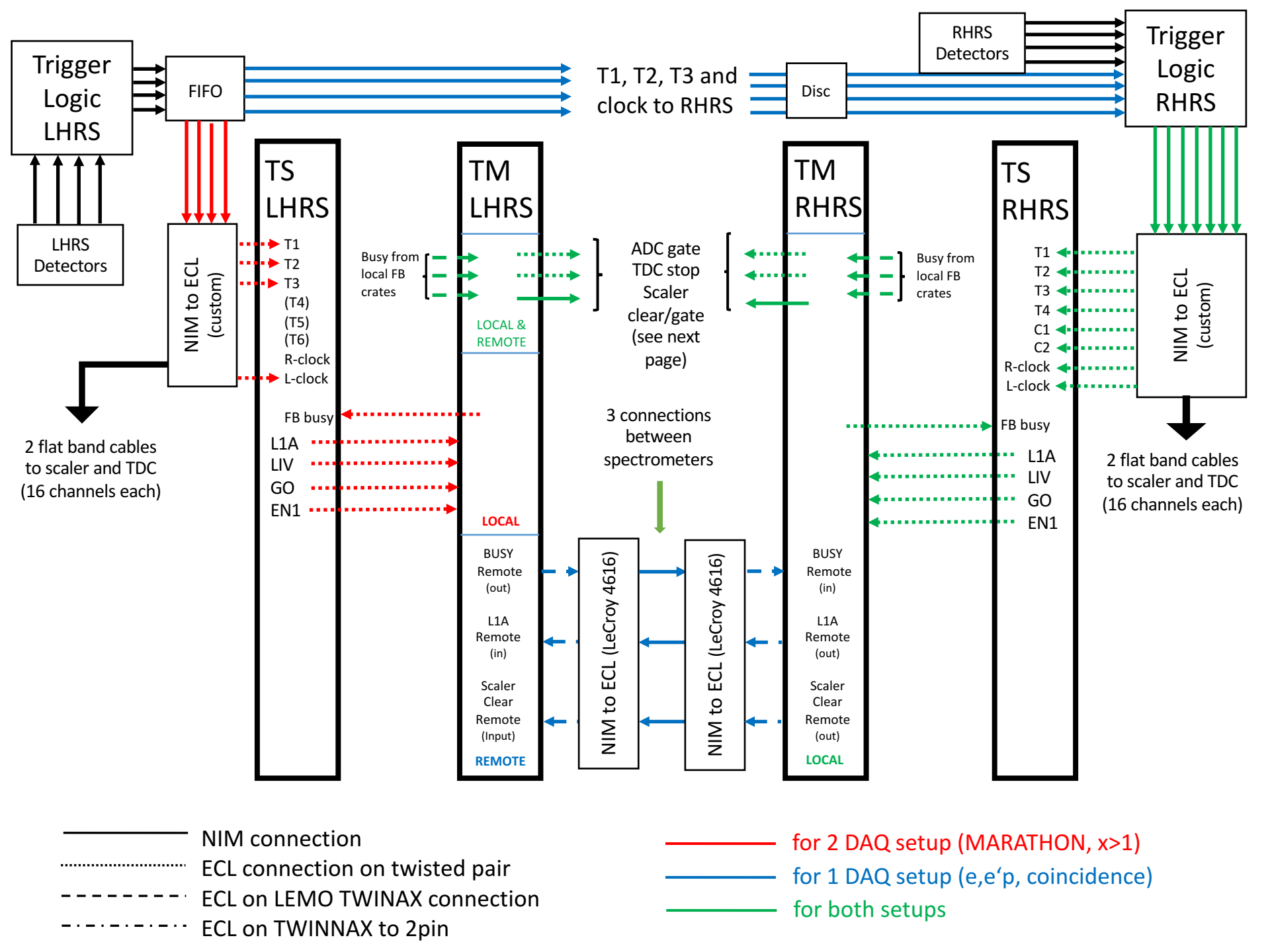
C1-T3 = -30ns:

$$t3 + 358.5 - (t3 + 337.5 + z)\ ns = -30\ ns$$
$$z = 51ns \approx 52\ ns$$

Coincidence triggers



- All coincidence trigger timed on T1 which corresponds to $S2_{LHRS}$


Trigger Logic LHRS
FIFO
T1, T2, T3 and clock to RHRS
Disc
RHRS Detectors
Trigger Logic RHRS
LHRS Detectors
NIM to ECL (custom)
TS LHRS
T1
T2
T3
(T4)
(T5)
(T6)
R-clock
L-clock
FB busy
L1A
LIV
GO
EN1
2 flat band cables to scaler and TDC (16 channels each)
TM LHRS
Busy from local FB crates
LOCAL & REMOTE
LOCAL
BUSY Remote (out)
L1A Remote (in)
Scaler Clear Remote (Input)
REMOTE
ADC gate
TDC stop
Scaler clear/gate
(see next page)
3 connections between spectrometers
NIM to ECL (LeCroy 4616)
NIM to ECL (LeCroy 4616)
TM RHRS
BUSY Remote (in)
L1A Remote (out)
Scaler Clear Remote (out)
LOCAL
Busy from local FB crates
TS RHRS
T1
T2
T3
T4
C1
C2
R-clock
L-clock
FB busy
L1A
LIV
GO
EN1
NIM to ECL (custom)
2 flat band cables to scaler and TDC (16 channels each)
NIM connection
ECL connection on twisted pair
ECL on LEMO TWINAX connection
ECL on TWINNAX to 2pin
for 2 DAQ setup (MARATHON, x>1)
for 1 DAQ setup (e,e'p, coincidence)
for both setups

Signals Exchange LHRS and RHRS

Fast cables (black, 222ns):

1. T1
2. T2
3. T3
4. L1A Remote
5. LHRS clock
6. Retiming signal , $(S0||S2)_{RHRS}$

Slower cables (grey, 240ns):

1. RHRS clock
2. Busy Remote
3. Scaler Gate/Clear Remote

Flatband RS485 connection TS to LHRS Fastbus and VME crates

+ add second RS485 connection for slow scaler readout on LHRS
+ add interconnection line for random pulser / accidental test

Setup Changes

Hardware changes:

- LHRS: Switch RS485 cable to establish communication between RHRS Trigger Supervisor (TS) and LHRS crates.
- RHRS: Plug coincidence trigger into NIM-ECL converter that then goes to TS.
- RHRS: Adjust trigger input delays in NIM-ECL converter to TS.
- RHRS only (fall 2018): Adjust ADC Gate for Fastbus.
- Connect another RS485 cable to establish LHRS scaler readout to RHRS TS

Software changes:

- **LHRS: Change boot code of Fastbus and TS crate.**
- **Change CODA control configuration.**
- **Replay script for coincidence.**
- **CODA start/end run scripts.**
- Adjust FADC latency (ADC gate for FADCs) (has to be done after we start taking data).
- Modify scaler GUI.
- Modification of scaler readout (LHRS slow scaler started in RHRS start script).
- Change datamon (software for live dead time monitoring).

Things to do for DAQ change (counting house)

- ❑ Restart Fastbus crates and stop auto boot
- ❑ Use changeboot scripts (changeboot_coincidence or changeboot_single) to adjust bootcode

- ❑ Startcoda with “startcoda 1” on adaq2 to start the coincidence connections
- ❑ Change FADC settings to mode 10 and threshold on
- ❑ Load RHRS_Twoarm config (or what we are using for nnL)
- ❑ See if CODA will download, config and start
- ❑ Take data

- ❑ Check if scalers on both arms are working
- ❑ Check if LHRS slow scaler are started in the RHRS start script

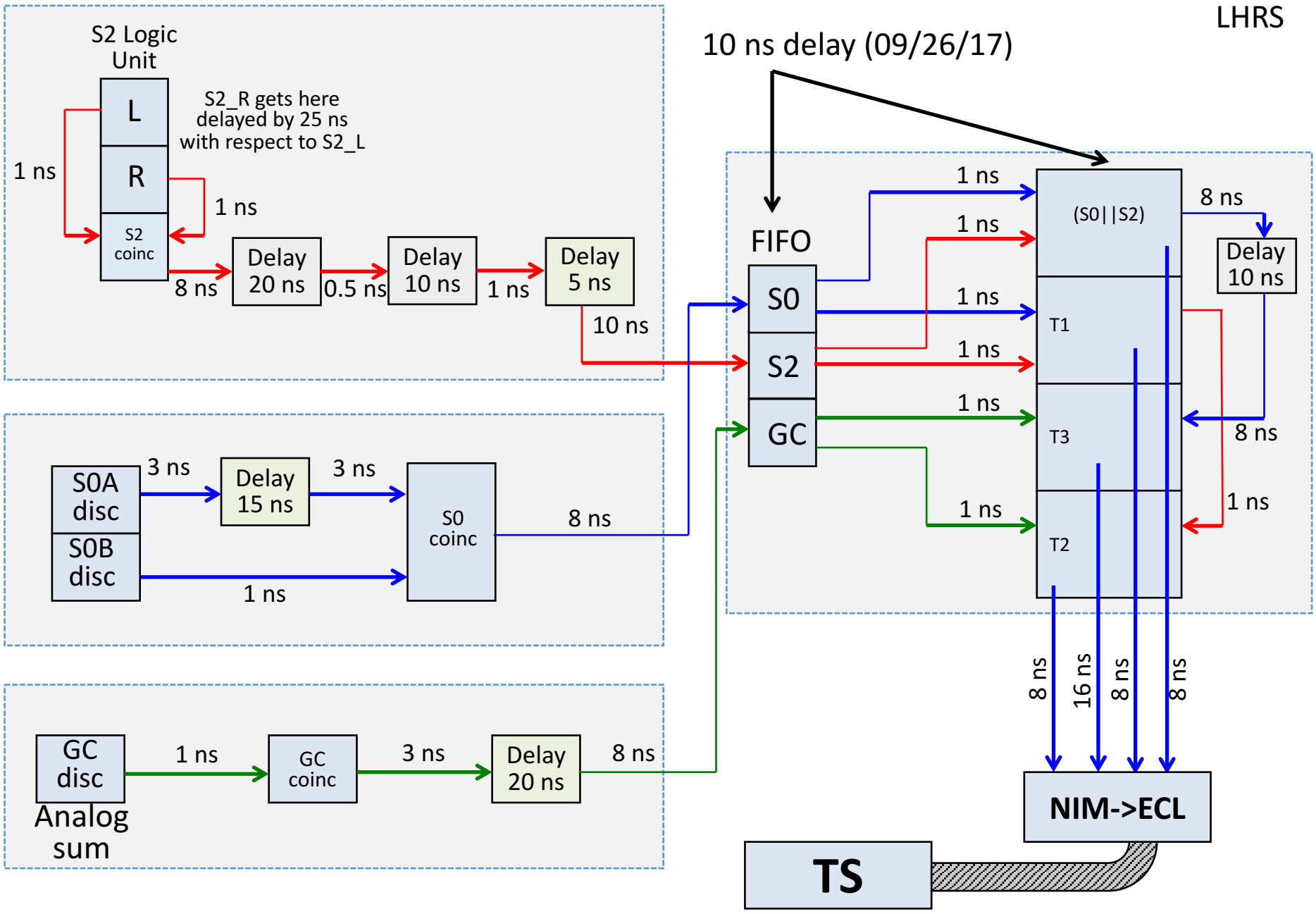
- ❑ Check FADC delays

Things to do for DAQ change (in the Hall)

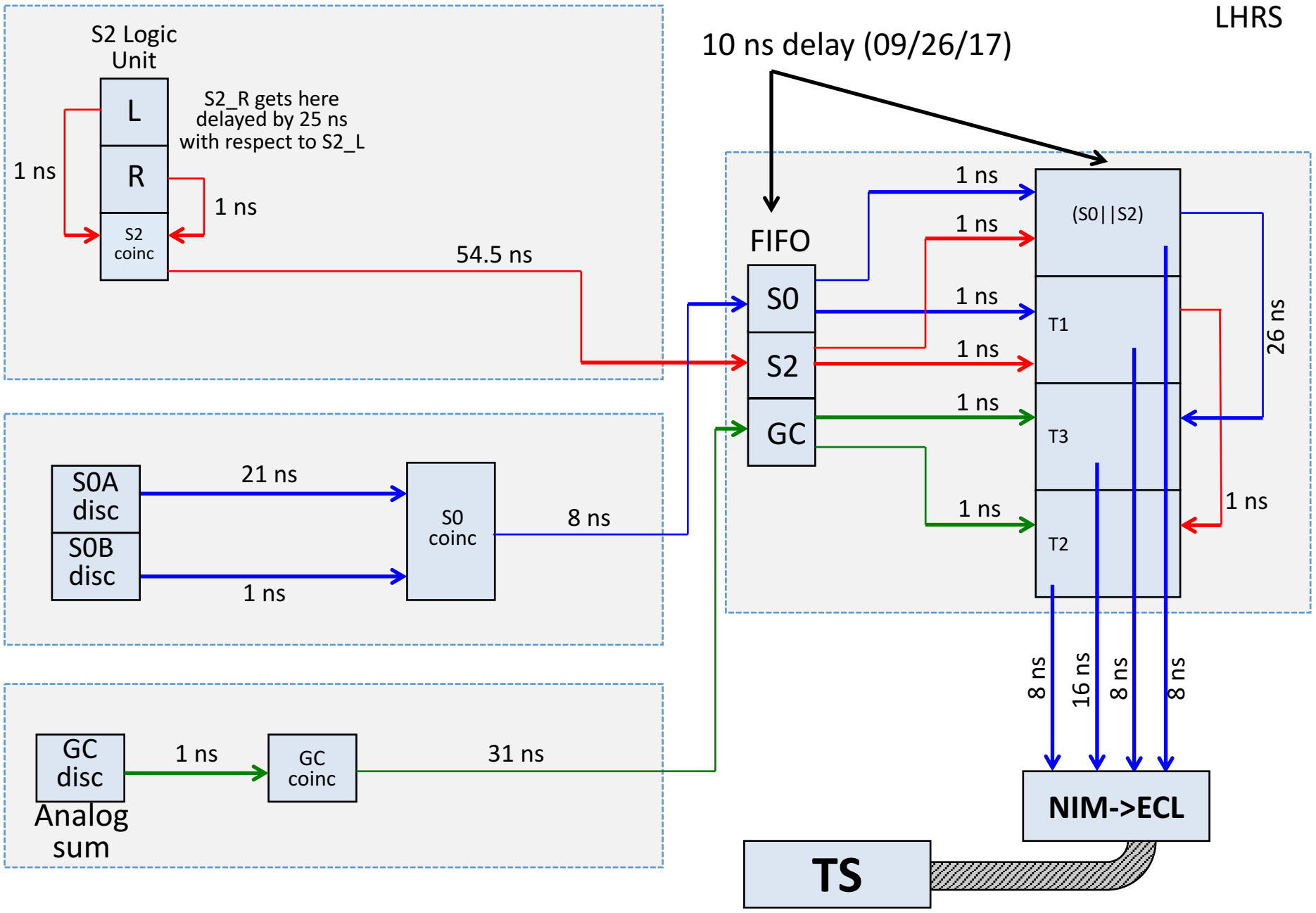
- ❑ LHRS: Move communication cable for branch
- ❑ LHRS: for F1TDC need L1A_remote input instead of L1A (best case same cable length)
- ❑ LHRS: Change L1A reference to L1A_remote FADC
- ❑ LHRS: Set up mixing of fake clock and accidentals, for C2 setup put T2 logic temporarily in OR mode)
- ❑ LHRS: Check F1TDC Trigger signal and polarity
- ❑ RHRS: Setup coincidence trigger delays with fake clock RHRS: Setup trigger delay inputs, inputs will be (T1-T3,T4,C1,C2,R and L clock)
- ❑ RHRS: S0&S2RHRS delayed output for C1 coincidence delay by 77ns more (from disc for width) and feed into TS channel 4 (currently T4). This allows for correct ADC gate adjustment for singles and delay with respect to C1 and T1
- ❑ C1, C2, T1, and T4 on Textronix 4channel scope, bring maybe 2-chan scope from LHRS to RHRS
- ❑ RHRS: Check F1TDC Trigger signal delay
- ❑ Fix problems (T6 check, more NIM modules)
- ❑ If CODA is running:
  - ❑ RHRS ADC gate adjustment with T4 and S0/GC for PS/SH
- ❑ Take Fake coincidence data
  - ❑ Only random clock trigger
  - ❑ Add accidentals with different rates on both arms
- ❑ Take cosmics data LHRS only and RHRS only with coincidence DAQ. Check F1 signals

LHRS

T1 = (S0&S2), T2 = (S0&S2)&GC, T3 = (S0||S2)&GC

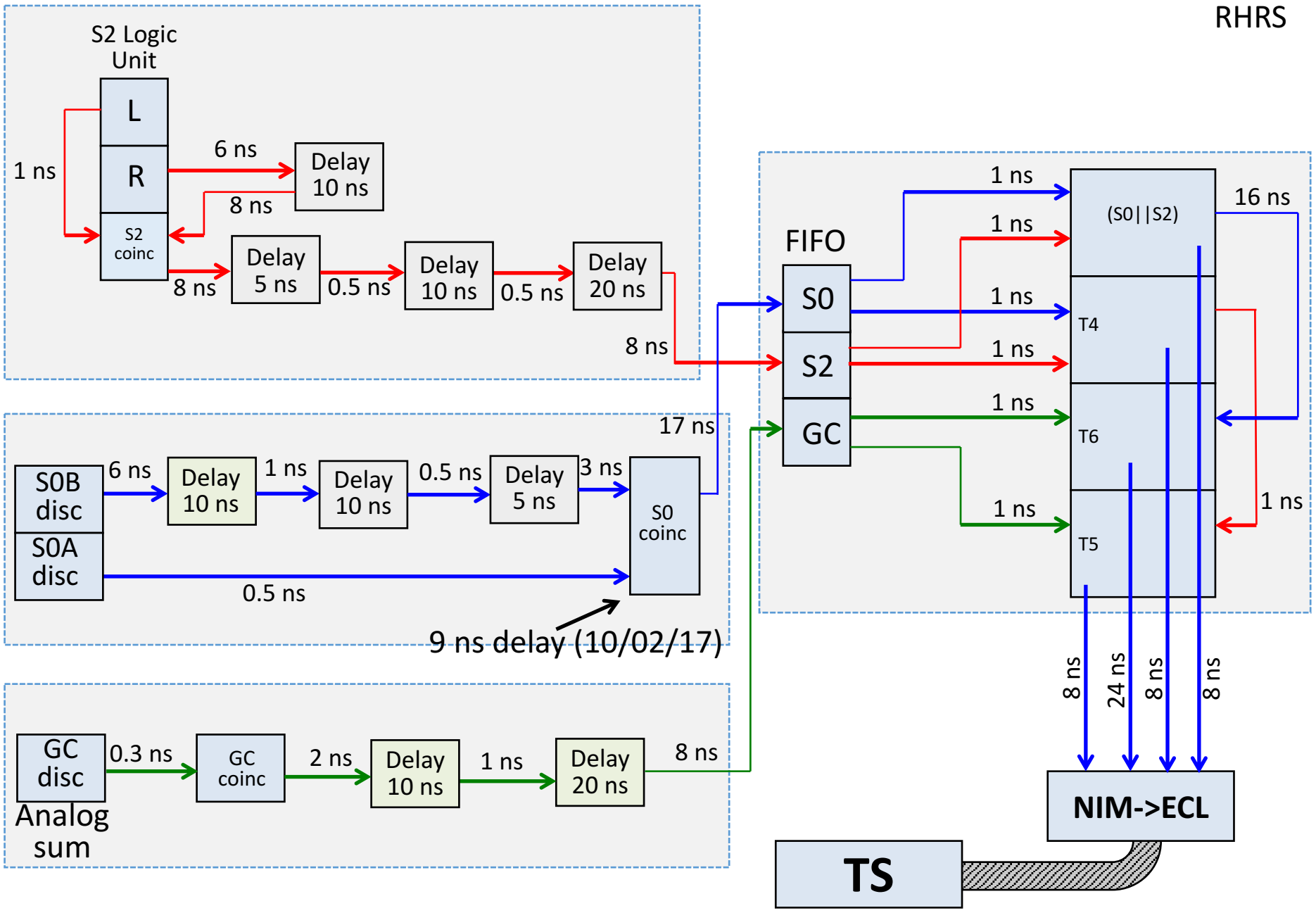


T1 = (S0&S2), T2 = (S0&S2)&GC, T3 = (S0||S2)&GC



RHRS

T4 = (S0&S2), T5 = (S0&S2)&GC, T6 = (S0||S2)&GC



T4 = (S0&S2), T5 = (S0&S2)&GC, T6 = (S0||S2)&GC